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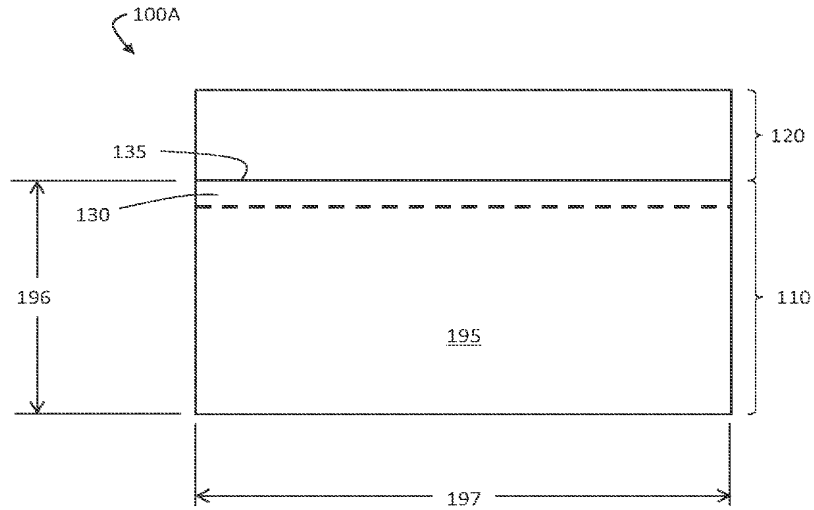


FIG. 1A

(57) **Abstract:** Material structures comprising III-nitride material regions (120) (e.g., gallium nitride material regions) are described herein. The material structures also comprise substrates (110) having relatively high electrical conductivities to reduce the degree to which thermal runaway occurs, which can enhance device performance including at elevated flange temperatures. Some embodiments include one or more features that reduce the degree of capacitive coupling exhibited during operation. For example, in some embodiments, relatively thick III-nitride material regions and/or relatively small ohmic contacts are employed.



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### **III-NITRIDE MATERIAL SEMICONDUCTOR STRUCTURES ON CONDUCTIVE SUBSTRATES**

#### **TECHNICAL FIELD**

5           III-nitride materials are generally described, including gallium nitride materials and associated material structures.

#### **BACKGROUND**

10           III-nitride materials include gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN) and their respective alloys (e.g., AlGaN, InGaN, AlInGaN and AlInN). In particular, gallium nitride materials include gallium nitride (GaN) and its alloys such as aluminum gallium nitride (AlGaN), indium gallium nitride (InGaN), and aluminum indium gallium nitride (AlInGaN). These materials are semiconductor compounds that have a relatively wide, direct bandgap which permits highly energetic  
15           electronic transitions to occur. Such electronic transitions can result in gallium nitride materials having a number of attractive properties including the ability to efficiently emit blue light, the ability to transmit signals at high frequency, and others.

          In many applications, III-nitride materials are typically grown heteroepitaxially on a substrate. However, property differences between III-nitride materials (e.g., gallium  
20           nitride materials) and many substrate materials can present challenges. For example, gallium nitride materials (e.g., GaN) have a different thermal expansion coefficient (i.e., thermal expansion rate) and lattice constant than many substrate materials and, in particular, silicon. These differences may lead to formation of cracks and/or other types of defects in gallium nitride material layers that are grown heteroepitaxially on silicon.  
25           In some methods, a transition layer is used to mitigate the effects of these differences in order to grow high quality gallium nitride material and device structures on silicon. However, these differences (and others) have limited the performance and commercialization of structures and devices that include gallium nitride material formed on silicon substrates.

30           III-nitride materials (e.g., gallium nitride materials) are being investigated in high frequency (e.g., radio frequency (RF)) device and power management applications. The use of III-nitride materials for certain applications can present challenges. Accordingly, improved devices and methods are desirable.

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## SUMMARY

III-nitride materials are generally described herein, including material structures comprising III-nitride material regions (e.g., gallium nitride material regions). In certain cases, the material structures also comprise substrates having relatively high electrical conductivities. Certain embodiments include one or more features that reduce the degree to which thermal runaway occurs, which can enhance device performance including at elevated flange temperatures. For example, in accordance with certain embodiments, III-nitride materials grown on substrates with relatively high electrical conductivities are described herein. The use of an electronically conductive substrate can reduce the amount of resistive heating that is present during device operation, which can reduce thermal runaway. Some embodiments include one or more features that reduce the degree of capacitive coupling exhibited during operation. For example, in some embodiments, relatively thick III-nitride material regions and/or relatively small ohmic contacts are employed. In some embodiments, the resulting semiconductor devices are capable of high efficiencies at elevated temperature and/or during operation at relatively high frequencies (e.g., RF frequencies).

The subject matter of the present invention involves, in some cases, interrelated products, alternative solutions to a particular problem, and/or a plurality of different uses of one or more systems and/or articles.

Some embodiments relate to a semiconductor structure for an integrated circuit component, comprising a substrate, at least a portion of which is made of bulk silicon having an electronic resistivity of less than  $0.10 \Omega\text{-cm}$  when the silicon is at  $25^\circ\text{C}$  and a III-nitride material region located over the substrate.

Some embodiments relate to a semiconductor structure for an integrated circuit component, comprising a substrate, at least a portion of which comprises silicon having an electronic resistivity of less than  $0.10 \Omega\text{-cm}$  when the silicon is at  $25^\circ\text{C}$  and a III-nitride material region located over the substrate, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.

Some embodiments relate to a semiconductor device, comprising a substrate, at least a portion of which is made of bulk silicon; a III-nitride material region having a thickness of at least 2.0 micrometers located over the substrate; a source electrode over the III-nitride material region, the source electrode defining a source electrode interfacial

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area with the III-nitride material region; a drain electrode over the III-nitride material region, the drain electrode defining a drain electrode interfacial area with the III-nitride material region; and a gate electrode over the III-nitride material region, the gate electrode defining a gate electrode interfacial area with the III-nitride material region;

5 wherein: the source electrode, and the drain electrode, and the gate electrode define an active area, and the sum of the source electrode interfacial area, the drain electrode interfacial area, and the gate electrode interfacial area is less than 30% of the active area.

Some embodiments relate to a semiconductor device, comprising: a substrate, at least a portion of which is made of bulk silicon; a III-nitride material region having a

10 thickness of at least 2.0 micrometers located over the substrate; at least one cathode electrode over the III-nitride material region, the at least one cathode electrode defining a cathode electrode interfacial area with the III-nitride material region; and an anode electrode over the III-nitride material region, the anode electrode defining an anode electrode interfacial area with the III-nitride material region; wherein: the at least one

15 cathode electrode and the anode electrode define an active area, and the sum of the cathode electrode interfacial area and the anode electrode interfacial area is less than 30% of the active area.

Some embodiments relate to a semiconductor device, comprising: a substrate, at least a portion of which comprises silicon; a III-nitride material region having a thickness

20 of at least 2.0 micrometers located over the substrate; an ohmic contact over the III-nitride material region, the ohmic contact defining an ohmic contact interfacial area with the III-nitride material region; and a gate electrode over the III-nitride material region, the gate electrode defining a gate electrode interfacial area with the III-nitride material region, wherein the ohmic contact interfacial area is less than 50 times the gate electrode

25 interfacial area.

Some embodiments relate to a semiconductor device comprising: a substrate, at least a portion of which comprises silicon; a III-nitride material region having a thickness of at least 2.0 micrometers located over the substrate; an integrated circuit component formed, at least in part, in the III-nitride material region; and at least one ohmic contact

30 over the III-nitride material region, wherein: the at least one ohmic contact defines, at least in part, an active area of the integrated circuit component, and an active-area capacitance ratio for the integrated circuit component is no greater than 0.4 pF/mm.

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Some embodiments relate to a semiconductor device, comprising: a substrate, at least a portion of which comprises silicon; and a III-nitride material region located over the substrate, wherein: the semiconductor device is configured such that at 25°C, the device is capable of a power added efficiency of at least 50%, and the semiconductor  
5 device is configured such that: when the substrate is increased in temperature from 25°C to 105 °C, the device exhibits a drop in power added efficiency of less than 5%, and/or when the substrate is increased in temperature from 25°C to 125 °C, the device exhibits a drop in power added efficiency of less than 10%.

Some embodiments relate to a semiconductor structure, comprising: a substrate,  
10 at least a portion of which is electronically conductive, the substrate having a thickness of less than 150 micrometers; a III-nitride material region located over the substrate; and an electronically conductive material located over the III-nitride material region, wherein: the electronically conductive material is electrically coupled to the electronically conductive portion of the substrate through the thickness of the III-nitride  
15 material region.

Some embodiments relate to a semiconductor device, comprising: a substrate comprising silicon; a III-nitride material region located over the substrate; at least one ohmic contact located over the substrate and the III-nitride material region and defining an ohmic contact interfacial area with the III-nitride material region; a dielectric region  
20 located over the substrate and over the III-nitride material region; and at least one contact pad located over the substrate, over the III-nitride material region, and over the dielectric region, the at least one contact pad defining a contact pad area, wherein the ratio of the ohmic contact area to the contact pad area is less than 28%.

Some embodiments relate to a structure comprising: a substrate comprising  
25 silicon and having a bulk resistivity less than 0.10  $\Omega$ -cm; a III-nitride material region located over the substrate; and an integrated circuit component formed, at least in part, in the III-nitride material region and wherein the integrated circuit component has a ratio of an active-area of the device, measured in square microns, to a gate or anode peripheral length, measured in microns, that is no greater than 200.

Some embodiments relate to a structure, comprising: a substrate comprising  
30 silicon and having a bulk resistivity less than 0.10  $\Omega$ -cm; a III-nitride material region located over the substrate; and an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one ohmic contact of a first type,

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wherein the integrated circuit component has a ratio of an ohmic contact interfacial area, measured in square microns, for the first type of ohmic contact to a gate or anode peripheral length, measured in microns, that is no greater than 30.

Some embodiments relate to a structure, comprising: a substrate comprising  
5 silicon and having a bulk resistivity less than  $0.10 \Omega\text{-cm}$ ; a III-nitride material region located over the substrate; and an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one gate or anode contact pad, wherein the integrated circuit component has a ratio of a contact-pad area, measured in square  
10 microns, for the at least one gate or anode contact pad to a gate or anode peripheral length, measured in microns, that is no greater than 20.

Some embodiments relate to a structure, comprising: a substrate comprising  
silicon and having a bulk resistivity less than  $0.10 \Omega\text{-cm}$ ; a III-nitride material region located over the substrate; and an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one drain, source, or cathode contact  
15 pad, wherein the integrated circuit component has a ratio of a contact-pad area, measured in square microns, for the at least one drain, source, or cathode contact pad to a gate or anode peripheral length, measured in microns, that is no greater than 50.

Some embodiments relate to a structure, comprising: a substrate comprising  
silicon and having a bulk resistivity less than  $0.10 \Omega\text{-cm}$ ; a III-nitride material region  
20 located over the substrate; and an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one ohmic contact of a first type, wherein the integrated circuit component has a ratio of an ohmic contact capacitance, in picofarads, calculated based on an area of the at least one ohmic contact, for the first type of ohmic contact to a gate or anode peripheral length, measured in millimeters, that is no  
25 greater than 2.5.

Some embodiments relate to a structure, comprising: a substrate comprising  
silicon and having a bulk resistivity less than  $0.10 \Omega\text{-cm}$ ; a III-nitride material region located over the substrate; and an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one gate or anode contact pad, wherein  
30 the integrated circuit component has a ratio of a contact pad capacitance, in picofarads, calculated based on an area of the at least one gate or anode contact pad, to a gate or anode peripheral length, measured in millimeters, that is no greater than 1.0.

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Some embodiments relate to a structure, comprising: a substrate comprising silicon and having a bulk resistivity less than  $0.10 \Omega\text{-cm}$ ; a III-nitride material region located over the substrate; and an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one source, drain, or cathode contact pad, wherein the integrated circuit component has a ratio of a contact pad capacitance, in picofarads, calculated based on an area for the at least one source, drain, or cathode contact pad, to a gate or anode peripheral length, measured in millimeters, that is no greater than 1.5.

Other advantages and novel features of the present invention will become apparent from the following detailed description of various non-limiting embodiments of the invention when considered in conjunction with the accompanying figures. In cases where the present specification and a document incorporated by reference include conflicting and/or inconsistent disclosure, the present specification shall control.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

Non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying figures, which are schematic and are not intended to be drawn to scale. In the figures, each identical or nearly identical component illustrated is typically represented by a single numeral. For purposes of clarity, not every component is labeled in every figure, nor is every component of each embodiment of the invention shown where illustration is not necessary to allow those of ordinary skill in the art to understand the invention. In the figures:

FIG. 1A is a cross-sectional schematic illustration of a semiconductor structure, according to certain embodiments;

FIG. 1B is a cross-sectional schematic illustration of a multi-layered III-nitride material region, according to some embodiments;

FIG. 1C is a cross-sectional schematic illustration of a multi-layered III-nitride material device region, according to certain embodiments;

FIG. 2A is, according to some embodiments, a cross-sectional schematic illustration of a device comprising a semiconductor structure;

FIG. 2B is a cross-sectional schematic illustration of a semiconductor device comprising an electronically conductive substrate, according to some embodiments;



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FIG. 2C is, in accordance with certain embodiments, a side-view schematic illustration of a semiconductor device having ohmic contacts on top of the III-nitride material region;

5 FIG. 2D is a top-view schematic illustration of the semiconductor device illustrated in FIG. 2A;

FIG. 3A is a top, perspective-view schematic illustration of a plurality of contact pairs, according to certain embodiments;

FIG. 3B is a top, perspective-view schematic illustration of a plurality of contact pairs, interfacial area, and active areas, according to certain embodiments;

10 FIG. 3C is a top, perspective-view schematic illustration of a plurality of gate, source, and drain electrodes, according to certain embodiments;

FIG. 3D is a top, perspective-view schematic illustration including gate contact pads, according to some embodiments;

15 FIG. 3E is a top, perspective-view schematic illustration including a drain contact pad, according to certain embodiments;

FIG. 3F is a top, perspective-view schematic illustration of a set of embodiments including a first type of source contact pad, according to some embodiments;

FIG. 3G is a top, perspective-view schematic illustration of contact pads and electrodes of a semiconductor device, according to certain embodiments;

20 FIG. 3H is a top, perspective-view schematic illustration of a portion of the structure shown in FIG. 3G, according to certain embodiments;

FIG. 4 is a cross-sectional schematic illustration of a device comprising a semiconductor structure that includes an electronically conductive material coupled to an electronically conductive substrate, according to certain embodiments;

25 FIG 5A is a plot showing measured efficiency of a semiconductor device as a function of substrate temperature for highly resistive silicon substrates and conductive silicon substrates, according to some embodiments;

30 FIG 5B is a plot showing measured output power of a semiconductor device as a function of substrate temperature for highly resistive silicon substrates and conductive silicon substrates, in some embodiments;

FIG. 6 is a plot of the dissipated power in a silicon substrate vs. the resistivity of a silicon substrate, according to certain embodiments;

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FIG. 7 is a plot of the dissipated power in a silicon substrate vs. the lattice temperature of a silicon substrate, in certain embodiments; and

FIG. 8 is a plot of the intrinsic capacitance vs. the III-nitride material thickness, according to some embodiments.

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### DETAILED DESCRIPTION

III-nitride materials are generally described herein, including material structures comprising III-nitride material regions and substrates (e.g., silicon-containing substrates). Certain embodiments are related to gallium nitride materials, and material structures comprising gallium nitride material regions and silicon-containing substrates.

10 It has been discovered, in accordance with certain embodiments, that in certain cases, operation of semiconductor devices including III-nitride material regions over substrates generates heat, which decreases the electrical resistance of the substrate. The decrease in electrical resistance can lead to an increase in current transported across the substrate, which can lead to additional resistive heating. In this way, a positive feedback effect (in which further heating leads to further reductions in electrical conductivity and additional further heating) can be present that can degrade product performance characteristics, such as output power and efficiency of devices formed from such semiconductor structures. Certain of the embodiments described herein are related to structures and methods of operation that reduce this positive feedback effect, which in certain cases, enhances device performance.

20 Certain embodiments are related to semiconductor structures comprising substrates having relatively high electronic conductivities. For example, in accordance with certain embodiments, the structures include substrates comprising silicon having a relatively high electronic conductivity. In certain embodiments, electronically conductive substrates can reduce issues arising from increased thermal resistance within the semiconductor structure. For example, without wishing to be bound by any particular theory, it is believed that the use of substrates having regions with relatively high electronic conductivity reduces the amount of heat that is generated via resistive heating during operation of the device. It is further believed that the reduction in the amount of heat generated by the device leads to enhanced device performance (e.g., an increase in power output and/or device efficiency).

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According to some embodiments, the semiconductor structures comprise relatively thick III-nitride layers. In certain embodiments, use of a relatively thick III-nitride layer (e.g., a relatively thick epitaxial GaN layer) reduces capacitive coupling between electrically conductive components of the semiconductor structure (e.g.,  
5 conductive metal structures, such as electrodes, of transistors) and the substrate (e.g., a silicon-containing substrate which can be electronically conductive). The reduction in capacitive coupling can reduce RF current displacement in the semiconductor structures, which can ultimately result in higher operating temperatures of the semiconductor structures, enhanced operating efficiency, and/or other performance improvements.

10 According to certain embodiments, the interfacial area between the III-nitride material surface and electronically conductive components in a semiconductor device is relatively small. This can be achieved, for example, by using small ohmic or Schottky contacts. In certain embodiments, reducing and/or minimizing the contact area between electrode structures (e.g., metal structures) and the III-nitride material surface results in  
15 the reduction of capacitive coupling between the electrode structures and the substrate (e.g., a silicon-containing substrate, which can be electronically conductive). Not wishing to be bound by any particular theory, the ohmic or Schottky contacts can, in certain cases, capacitively couple to the substrate, which can result in the loss of energy during operation of the semiconductor device. It is believed that when large ohmic or  
20 Schottky contacts are used, capacitive coupling increases, which can result in increased displacement current, resulting in dissipated power in the substrate. Conversely, as the contact area is decreased, capacitive coupling to the substrate and displacement current can be decreased, leading to enhanced performance.

According to some embodiments, a dielectric region is located over the substrate  
25 and over the III-nitride material region. In certain embodiments, the dielectric region provides a surface on which large contact pads are formed. According to some embodiments when large contact pads are present on the thick dielectric region, the thick dielectric region separates the large contact pads from the III-nitride material region and underlying substrate, resulting in reduced capacitive coupling to the substrate (e.g., a  
30 silicon-containing substrate, which can be electronically conductive). In certain embodiments, a large contact pad present on a thick dielectric region reduces unwanted capacitance associated with the contact pad.

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In certain embodiments, the semiconductor structures described herein comprise a backside ground that couples an electronically conductive material (e.g., a contact pad and/or an electrode) of a device to the electronically conductive substrate through the thickness of the III-nitride material region. According to certain embodiments, the electronically conductive material that is coupled to the electronically conductive substrate is coupled to the source electrode and/or drain electrode. In some embodiments, the electronically conductive material reduces the capacitance to the silicon-containing substrate (e.g., to ground) by providing an alternate source of grounding.

Some embodiments described herein are related to semiconductor structures and devices with improved performance. For example, in accordance with certain embodiments, the semiconductor structures exhibit increased efficiency at elevated temperatures. Furthermore, in certain embodiments, the semiconductor structures have small drops in efficiency upon increasing operating temperatures of the semiconductor structures.

Certain embodiments are related to inventive semiconductor structures. Certain inventive semiconductor structures described herein can comprise a substrate and a III-nitride material region located over the substrate (e.g., at least one region comprising III-nitride material formed over a surface region of the substrate). In some cases, a substrate can have one or more semiconductor layers and may further include one or more thin-film dielectric layers. A substrate may be made of bulk silicon or may comprise silicon in various embodiments. In some implementations, the III-nitride material region can include one or more thin-film dielectric layers.

FIG. 1A is a cross-sectional schematic illustration of a semiconductor structure 100A, according to certain embodiments. Semiconductor structure 100A comprises substrate 110 and a III-nitride material region 120 located over surface 135 of substrate 110 (and, thus, over surface region 130 of substrate 110). According to certain embodiments, surface 135 of substrate 110 can be a silicon surface. For example, surface 135 may correspond to a surface of a silicon wafer, in some embodiments. In certain embodiments, the top surface (e.g., surface 135 in the figures) may correspond to a silicon surface of a composite substrate (e.g., comprising a silicon layer and one or more additional underlying layers). For example, in some embodiments, surface 135

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may correspond to a surface of a silicon portion of a silicon-on-insulator substrate, surface 135 may correspond to a surface of a silicon-on-sapphire substrate.

According to certain embodiments and as described above, the semiconductor structures described herein comprise a substrate. In certain embodiments, the substrate  
5 comprise silicon (i.e., a substrate containing the element silicon in any form). Some embodiments are related to substrates at least a portion of which is made of silicon. Certain embodiments are related to substrates at least a portion of which (or all of which) is made of bulk silicon. As used herein, bulk silicon refers to doped or undoped elemental Si in any form. Substrates that contain bulk silicon can include, for example,  
10 at least a layer of doped or undoped silicon, as opposed to silicon oxides, silicon carbides, silicon nitrides, etc. Examples of substrates comprising silicon that can be used in various embodiments include, but are not limited to, bulk silicon wafers, silicon-on-insulator substrates, and substrates made of or comprising alloys of silicon (e.g., silicon germanium and silicon carbide substrates). In some embodiments, the substrate  
15 comprises a silicon substrate. As used herein, a silicon substrate refers to any substrate that includes a silicon surface. Examples of suitable silicon substrates include substrates that are composed entirely of silicon (e.g., bulk silicon wafers), silicon-on-insulator (SOI) substrates, and silicon-on-sapphire (SOS) substrates. Suitable silicon substrates also include composite substrates that have a silicon wafer bonded to another material  
20 such as diamond or other crystallographic forms of carbon, aluminum nitride (AlN), silicon carbide (SiC), or other crystalline or polycrystalline materials. Silicon substrates having different crystallographic orientations may be used, though single crystal silicon substrates may be preferred in certain, but not necessarily all, embodiments. In some  
25 embodiments, silicon (111) substrates are used. In certain embodiments, silicon (100) or (110) substrates are used. As used herein, a silicon carbide substrate refers to any substrate that includes a silicon carbide surface. Examples of suitable silicon carbide substrates include substrates that are composed entirely of silicon carbide (e.g., bulk silicon carbide wafers), silicon carbide composite wafers (e.g., wafers comprising a silicon carbide layer and a second layer of a material that is not silicon carbide), and the  
30 like.

In certain embodiments, at least a portion of the substrates described herein are electronically conductive. In some embodiments, the substrate comprises at least one layer that is electronically conductive. For example, in certain embodiments in which

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silicon substrates are used, the silicon substrate (or at least the silicon portion of the substrate for substrates that include a silicon portion formed on another material) is electronically conductive. As used herein, a material (e.g., a region, a layer, a substrate, etc.) is considered to be electronically conductive when it has an electronic resistivity of less than  $0.10 \Omega \cdot \text{cm}$  when at  $25^\circ \text{C}$ . In certain embodiments, the region of the substrate underneath an active region of the semiconductor structure has a resistivity of about  $0.01 \Omega \cdot \text{cm}$  to about  $0.10 \Omega \cdot \text{cm}$ . For example, electronically conductive materials (e.g., regions, layers, substrates) have electronic resistivities of less than  $0.10 \Omega \cdot \text{cm}$  in some embodiments, less than  $0.05 \Omega \cdot \text{cm}$  in some embodiments, less than  $0.03 \Omega \cdot \text{cm}$  in some embodiments, less than  $0.01 \Omega \cdot \text{cm}$  in some embodiments, less than  $0.001 \Omega \cdot \text{cm}$  in some embodiments, less than  $0.0001 \Omega \cdot \text{cm}$  in some embodiments, less than  $0.00001 \Omega \cdot \text{cm}$  in some embodiments, or yet less than  $0.000001 \Omega \cdot \text{cm}$  in some embodiments, when the electronically conductive materials are at  $25^\circ \text{C}$ . According to certain embodiments, the electronic resistivity of the material (e.g., a layer, a substrate) when at  $25^\circ \text{C}$  is greater than  $0 \Omega \cdot \text{cm}$  in some embodiments, greater than  $1 \times 10^{-10} \Omega \cdot \text{cm}$  in some embodiments, greater than  $1 \times 10^{-9} \Omega \cdot \text{cm}$  in some embodiments, greater than  $1 \times 10^{-8} \Omega \cdot \text{cm}$  in some embodiments, greater than  $1 \times 10^{-6} \Omega \cdot \text{cm}$  in some embodiments, greater than  $1 \times 10^{-4} \Omega \cdot \text{cm}$  in some embodiments, greater than  $1 \times 10^{-2} \Omega \cdot \text{cm}$  in some embodiments, and yet greater than  $0.01 \Omega \cdot \text{cm}$  in some embodiments. Combinations of these ranges are also possible, (e.g., greater than  $1 \times 10^{-10} \Omega \cdot \text{cm}$  and less than  $0.10 \Omega \cdot \text{cm}$ ).

The electronic resistivity of a material (e.g., a region, a layer, a substrate, etc.) is measured laterally across the material (i.e., in a direction perpendicular to the thickness of the substrate). Those of ordinary skill in the art are capable of determining the electronic resistivity of a material. For example, the electronic resistivity of a material (e.g., a region, a layer, a substrate, etc.) can be determined by first making a resistance measurement across a known geometry (e.g., by placing two electrodes across the material). The resistivity of the material can then be determined as follows:

$$\rho = R \frac{A}{l} \quad (1)$$

where  $R$  is the measured electrical resistance,  $A$  is the cross-sectional area over which the resistance measurement was taken, and  $l$  is the length of the area over which the

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resistance measurement was taken. The conductivity of the region (also sometimes referred to as the “conductance”) is the inverse of the resistivity of the region.

In some embodiments, the substrate comprises at least one portion having a length of at least 1 micrometer, at least 10 micrometers, at least 100 micrometers, at least 5 1 mm, or at least 10 mm, wherein that portion also has an electronic resistivity of less than  $0.10 \Omega \cdot \text{cm}$  (or within any of the ranges outlined above) when at 25 °C.

Electronically conductive substrates (e.g., comprising silicon, such as silicon substrates or other substrates comprising silicon) may be particularly useful in some (but not necessarily all) structures that are used to form devices that operate at high 10 frequencies (e.g., RF devices). According to certain embodiments, the high conductivity can reduce so-called substrate losses which otherwise may arise and sacrifice performance. These substrate losses may render substrates with higher resistivities unsuitable in high frequency devices.

In certain embodiments, a substrate having one or more integrated circuit 15 components (such as devices and/or discrete components) may have various device layers, homojunctions, heterojunctions, or circuit layers embedded in the substrate, or formed on the front-side and/or back-side of the substrate. Such substrates may be semi-spec standard thickness, or thicker, or in some implementations thinner than semi-spec standards. In some cases, for example, an Si substrate may have a diameter of less than 20 one hundred millimeters (100 mm), while in other implementations, the substrate may have a diameter in a range from approximately 100 mm to approximately 150 mm. In certain embodiments, the substrate diameter may be in a range from approximately 150 mm to approximately 200 mm, or larger. In still other embodiments, the substrate may include a textured surface or may have a non-planar surface.

25 Embodiments include substrates of smaller size than a full wafer. The term “substrate” can also refer to a substrate having properties as described above and having a size of a chip, die, or discrete device. In certain implementations, a substrate of a chip, die, or discrete device is singulated from a larger wafer.

In some embodiments, the substrate may also have any of a variety of suitable 30 thicknesses. According to some embodiments, the substrate has a thickness of less than 150 micrometers. According to certain embodiments, the substrate has a thickness of less than 100 micrometers, less than 50 micrometers, or less. According to certain embodiments, the thickness of the substrate may be selected based on the final device

and heteroepitaxial specifications (e.g., wafer warp and bow), for example, as needed for successful high yielding semiconductor fabrication. In some embodiments, the thickness of the substrate may be semi-spec thicknesses typical of the wafer diameter used in high volume wafer silicon manufacturing.

5 As used herein, the term “III-nitride material” refers to any Group III element-nitride compound. Non-limiting examples of III-nitride materials include boron nitride (BN), aluminum nitride (AlN), gallium nitride (GaN), indium nitride (InN), and thallium nitride (TlN), as well as any alloys including Group III elements and Group V elements (e.g.,  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ ,  $\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{N}$ ,  $\text{In}_y\text{Ga}_{(1-y)}\text{N}$ ,  $\text{Al}_x\text{In}_{(1-x)}\text{N}$ ,  $\text{GaAs}_a\text{P}_b\text{N}_{(1-a-b)}$ ,  
10  $\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{As}_a\text{P}_b\text{N}_{(1-a-b)}$ , and the like). Typically, when present, arsenic and/or phosphorus are at low concentrations (e.g., less than 5 weight percent). III-nitride materials may be doped n-type or p-type, or may be intrinsic. III-nitride materials may have any polarity including but not limited to Ga-polar, N-polar, semi-polar, or non-polar crystal orientations. A III-nitride material may also include either the Wurtzite,  
15 Zincblende, or mixed polytypes, and may include monocrystalline, polycrystalline, or amorphous structures.

In some embodiments, the III-nitride material region comprises a gallium nitride material. As used herein, the phrase “gallium nitride material” refers to gallium nitride (GaN) and any of its alloys, such as aluminum gallium nitride ( $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ ), indium  
20 gallium nitride ( $\text{In}_y\text{Ga}_{(1-y)}\text{N}$ ), aluminum indium gallium nitride ( $\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{N}$ ), gallium arsenide phosphide nitride ( $\text{GaAs}_a\text{P}_b\text{N}_{(1-a-b)}$ ), aluminum indium gallium arsenide phosphide nitride ( $\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{As}_a\text{P}_b\text{N}_{(1-a-b)}$ ), amongst others. In certain embodiments, the III-nitride material region comprises GaN. According to some  
25 embodiments, the III-nitride material region is an epitaxial III-nitride material region. In certain embodiments, the III-nitride material region comprises a heterojunction, a two-dimensional electron gas (2DEG) region, and/or two-dimensional hole gas (2DHG). In some embodiments, the III-Nitride material region comprises doped homojunctions and/or doped heterojunctions.

Typically, when present, arsenic and/or phosphorus are at low concentrations  
30 (i.e., less than 5 weight percent). In certain embodiments, the gallium nitride material has a high concentration of gallium and includes little or no amounts of aluminum and/or indium. In high gallium concentration embodiments, the sum of  $(x+y)$  may be less than 0.4, less than 0.2, less than 0.1, or even less. In some cases, it is preferable for the



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gallium nitride material layer to have a composition of GaN (i.e.,  $x+y=0$ ). Gallium nitride materials may be doped n-type or p-type, or may be intrinsic.

According to some embodiments, the thickness of the III-nitride material device region (e.g., which may comprise at least one gallium nitride material layer) and the number of different layers within the III-nitride material device region are dictated, at least in part, on the application in which the semiconductor structure is used. In some embodiments, the III-nitride material region is thick. According to certain embodiments, at a minimum, the total thickness of the III-nitride material region (or any individual layer within the III-nitride material device region) is sufficient to permit formation of the desired semiconductor structure or device. Certain embodiments are related to a III-nitride material region having a thickness of at least 2.0 micrometers located over the substrate. In some embodiments, the thickness of the III-nitride material device region is greater than 2.0 micrometers, or greater than 3.0 micrometers, or greater than 4.0 micrometers, greater than 5.0 micrometers, greater than 6.0 micrometers, greater than 7.0 micrometers, greater than 8.0 micrometers, or greater than 9.0 micrometers. According to certain embodiments, the thickness the III-nitride material device region is less than 10.0 micrometers, less than 9.0 micrometers, less than 8.0 micrometers, less than 7.0 micrometers, less than 6.0 micrometers, less than 5.0 micrometers, less than 4.0 micrometers, less than 3.0 micrometers, or less than 2.0 micrometers. Combinations of these ranges are also possible (e.g., greater than 2.0 micrometers and less than 5.0 micrometers, greater than 3.0 micrometers and less than 4.0 micrometers). Some embodiments are related to a III-nitride material region having a thickness of 4.8 micrometers.

In some embodiments, the III-nitride material region is located over the substrate. When a structure (e.g., layer and/or device) is referred to as being “on,” “over,” or “overlying” another structure (e.g., layer or substrate), it is over at least a portion of that structure. In some cases, a structure that is referred to as being “on,” “over,” or “overlying” another structure is over the entirety of that structure. When a structure (e.g., layer and/or device) is referred to as being “on,” “over,” or “overlying” another structure (e.g., layer or substrate), it can be directly on the structure, or an intervening structure (e.g., a layer, air gap) also may be present. A structure that is “directly on” or “in direct contact with” another structure means that no intervening structure is present. It should also be understood that when a structure is referred to as being “on” or “over”

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another structure, it may cover the entire structure, or a portion of the structure. In addition, when a structure is referred to as being “on” or “over” another structure, it may be embedded within that structure.

According to some embodiments, the III-nitride material region comprises an optional III-nitride nucleation layer or intermediate layer. For example, referring to the exemplary embodiment of FIG. 1B, III-nitride material region 120 comprises III-nitride material transition layer 170. It should be understood that transition layer 170 is optional, and in other embodiments, III-nitride material region 120 does not include transition layer 170.

In FIG. 1B, transition layer 170 is formed directly on nucleation layer 155. In other embodiments, one or more materials may be positioned between transition layer 170 and nucleation layer 155.

The nucleation layer can, according to certain embodiments, prepare a surface of the substrate for growth of III-nitride material over the substrate. In certain cases, III-nitride material (e.g., gallium nitride materials and/or other III-nitride materials) can be difficult to grow heteroepitaxially directly on the substrate (and/or another region that is over a surface of the substrate), for example, because the III-nitride material one wishes to grow may have a lattice structure and/or a lattice constant which is significantly different than the substrate or other underlying region. According to certain embodiments, the nucleation layer forms an appropriate template to transition from the lattice of the substrate (or other underlying layer) to a template more suitable for III-nitride growth. In certain embodiments, the nucleation layer can accommodate the difference in the lattice constants of an overlying layer in the III-nitride material region (e.g., the III-nitride material region portion in direct contact with the nucleation layer) and the region underneath the nucleation layer (e.g., the substrate and/or another underlying region, which in some cases, may be in direct contact with the nucleation layer). In some embodiments, the nucleation layer can accommodate the difference in the thermal expansion coefficients of an overlying layer in the III-nitride material region (e.g., the III-nitride material region portion in direct contact with the nucleation layer) and the region underneath the nucleation layer (e.g., the substrate and/or another underlying region, which in some cases, may be in direct contact with the nucleation layer). According to certain embodiments, the nucleation layer can accommodate both the difference in lattice constants and the difference in thermal expansion coefficients of

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an overlying layer in the III-nitride material region and the region underneath the nucleation layer. In some embodiments, the nucleation layer may also act as a reaction barrier between the III-nitride material region and the silicon substrate. For example, in organometallic vapor phase epitaxy (OMVPE) growth environments (e.g., metal-organic chemical vapor deposition (MOVCD)), the introduction of gallium species in direct proximity to the silicon surface can result in the formation and accumulation of free gallium atoms and deleterious formation of SiN preventing proper initiation of GaN heteroepitaxy. This can be prevented by first forming an AlN heteroepitaxy nucleation layer which acts to seal the silicon surface and reacting with subsequent growth of GaN or gallium containing III-Nitride material layers.

According to certain embodiments, the nucleation layer comprises an aluminum nitride material. As used herein, the phrase “aluminum nitride material” refers to aluminum nitride (AlN) and any of its alloys, such as aluminum gallium nitride ( $\text{Al}_{(1-x)}\text{Ga}_{(x)}\text{N}$ ), aluminum indium nitride ( $\text{Al}_{(1-x)}\text{In}_{(x)}\text{N}$ ), aluminum indium gallium nitride ( $\text{Al}_{(1-x-y)}\text{In}_{(x)}\text{Ga}_{(y)}\text{N}$ ), aluminum indium gallium arsenide phosphide nitride ( $\text{Al}_{(1-x-y)}\text{In}_x\text{Ga}_y\text{As}_a\text{P}_b\text{N}_{(1-a-b)}$ ), amongst others. In certain embodiments, the aluminum nitride material has a high concentration of aluminum and includes little or no amounts of gallium and/or indium. In high aluminum concentration embodiments, the sum of  $(x+y)$  may be less than 0.4, less than 0.2, less than 0.1, or even less. In some cases, it is preferable for the aluminum nitride material to have a composition of AlN (i.e.,  $x+y=0$ ). Aluminum nitride materials may be doped n-type or p-type, or may be intrinsic. In certain embodiments, the use of an aluminum nitride material as the nucleation layer may be preferred in certain cases in which the III-nitride material is formed on the substrate without the use of a diffusion barrier region between the III-nitride material and the substrate.

According to certain embodiments, the nucleation layer may comprise one or more layers. When multiple nucleation layers are present, the nucleation layers may be made of the same material or different materials. In addition, in certain embodiments in which multiple nucleation layers are present, the nucleation layers may be formed using different semiconductor growth conditions. For example, in some embodiments, the nucleation layers may comprise two or more aluminum nitride material layers formed at different growth temperatures (e.g., one at a relatively low temperature and another at a relatively high temperature). In some embodiments, other growth conditions (e.g.,

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pressure, reactant flow rates, etc.) may be varied from the growth of one nucleation layer to another.

Suitable materials from which the III-nitride material nucleation layer may be formed include, but are not limited to, aluminum nitride materials (e.g., aluminum nitride, aluminum nitride alloys). The III-nitride material nucleation layer typically has a constant composition.

In some embodiments, the nucleation layer comprises a first aluminum nitride-based layer and a second aluminum nitride-based layer. The aluminum nitride-based nucleation layer can include aluminum nitride as well as other optional elements, such as silicon and/or oxygen. For example, in some embodiments, the aluminum nitride-based nucleation layer can be a thin (e.g., from about 10 Angstroms to about 20 Angstroms, or thinner) amorphous or non-crystalline (unordered) material comprising aluminum and nitrogen, and optionally silicon and/or oxygen. In some embodiments, the amorphous aluminum nitride-based layer may also act as a diffusion barrier region as discussed further below. In other embodiments, one or more separate diffusion barrier layers can be used in combination with the aluminum-nitride based layer.

In certain embodiments, a III-nitride material nucleation layer has a single crystal structure. It may be advantageous, in some but not necessarily all embodiments, for a III-nitride material nucleation layer to have a single crystal structure because such structures can facilitate formation of one or more single crystal layers (e.g., gallium nitride material layers) above the III-nitride material nucleation layer.

It should also be understood that a III-nitride material nucleation layer may not have a single crystal structure and may be amorphous or polycrystalline, though certain of the advantages associated with the single crystal nucleation layers may not be achieved in some such embodiments.

The III-nitride material nucleation layer may have a number of suitable thicknesses. For example, the III-nitride material nucleation layer may have a thickness of between about 10 nanometers and about 5 micrometers, though other thicknesses are also possible. In certain embodiments in which more than one nucleation layer is employed, the combined thickness of the nucleation layers may be between about 10 nanometers and about 5 micrometers, though other thicknesses are also possible.

According to certain embodiments, the III-nitride material region comprises an optional III-nitride transition layer. For example, referring to the exemplary embodiment

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of FIG. 1B, III-nitride material region 120 comprises III-nitride material transition layer 170. It should be understood that transition layer 170 is optional, and in other embodiments, III-nitride material region 120 does not include transition layer 170.

In FIG. 1B, transition layer 170 is formed directly on nucleation layer 155. In  
5 other embodiments, one or more materials may be positioned between transition layer 170 and nucleation layer 155.

In some embodiments, the III-nitride transition layer is compositionally graded. In some embodiments, the III-nitride material transition layer comprises a compositionally graded III-nitride material. Examples of such materials are described,  
10 for example, in U.S. Patent No. 6,649,287, issued November 18, 2003, and entitled “Gallium Nitride Materials and Methods,” which is incorporated herein by reference in its entirety for all purposes. Compositionally-graded transition layers have a composition that is varied across at least a portion of the layer (e.g., across at least a portion of the thickness of the layer). For example, according to certain embodiments in  
15 which the transition layer comprises a III-nitride material layer, the concentration of at least one of the elements (e.g., Ga, Al, In) of the III-nitride material is varied across at least a portion of the thickness of the transition layer. Compositionally-graded transition layers are particularly effective, according to certain embodiments, in reducing crack formation in gallium nitride material regions formed on the transition layer, for example,  
20 by lowering thermal stresses that result from differences in thermal expansion rates between the gallium nitride material and the substrate (e.g., silicon). Compositionally-graded transition layers may also contribute to reducing generation of screw dislocations in the III-nitride material layer(s)/region(s) (e.g., gallium nitride material layer(s)). In some cases, the compositionally-graded transition layers may also contribute to reducing  
25 mixed and edge dislocation densities.

The composition of a compositionally-graded III-nitride material layer can be graded, for example, discontinuously (e.g., step-wise) or continuously. The composition of the compositionally-graded layer can be graded across the entire thickness of the layer, or across only a portion of the thickness of the layer.

30 According to one set of embodiments, the transition layer is compositionally-graded and formed of an alloy of gallium nitride such as  $\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{N}$ ,  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ , and  $\text{In}_y\text{Ga}_{(1-y)}\text{N}$ . In some such embodiments, the concentration of at least one of the elements (e.g., Ga, Al, In) of the alloy is varied across at least a portion of the thickness

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of the transition layer. In certain embodiments in which the transition layer has an  $\text{Al}_x\text{In}_y\text{Ga}_{(1-y)}\text{N}$  composition,  $x$  and/or  $y$  may be varied. In certain embodiments in which the transition layer has a  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$  composition,  $x$  may be varied. In certain embodiments in which the transition layer has a  $\text{In}_y\text{Ga}_{(1-y)}\text{N}$  composition,  $y$  may be varied.

In certain embodiments, it is desirable for the transition layer to have a low gallium concentration at a back surface which is graded to a high gallium concentration at a front surface. It has been found that such transition layers can be particularly effective in relieving internal stresses within overlying gallium nitride material layers. For example, the transition layer may have a composition of  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ , where  $x$  is decreased from the back surface to the front surface of the transition layer (e.g.,  $x$  is decreased from a value of 1 at the back surface of the transition layer to a value of 0 at the front surface of the transition layer).

In some embodiments, the semiconductor structure includes an aluminum nitride nucleation layer and a compositionally-graded transition layer. In some embodiments, the compositionally-graded transition layer has a composition of  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ , where  $x$  is continuously graded from a value of 1 at the back surface of the transition layer to a value of 0 at the front surface of the transition layer. One discontinuous grade may include steps of  $\text{AlN}$ ,  $\text{Al}_{0.6}\text{Ga}_{0.4}\text{N}$ , and  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$  (step grades) proceeding in a direction toward the gallium nitride material layer. In another example of a discontinuously graded III-nitride material transition layer, there may be periodic layers and/or intervening layers inserted between one or more of the step layers making up the step grade. The periodic layers and/or intervening layers, for example, may be layers of aluminum nitride material (e.g.,  $\text{AlN}$  or  $\text{AlGaN}$ ) formed at the same or different (e.g., lower) temperatures than are used to form the step grade layers. Another example of periodic layers or intervening layers include silicon nitride and/or aluminum silicon nitride layers, which can act as masking layers to pin the vertical threading and screw dislocations which may extend from one layer to the next.

It should be understood that, in other cases, the transition layer may have a constant composition and may not be compositionally-graded. In some cases (e.g., in certain cases in which the substrate is not a silicon substrate), the transition layer may have a constant composition. Suitable compositions include, but are not limited to, aluminum nitride-based materials (e.g., aluminum nitride, aluminum nitride alloys) and

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gallium nitride materials. In these constant composition embodiments, the transition layer may be similar to the nucleation layer described above.

According to certain embodiments, the transition layer may be made of, at least in part, one or more superlattices. In some cases, a superlattice of a transition layer can be formed as a strained layer superlattices (SLS). In some cases, a superlattice of a transition layer can be formed as a multiple quantum wells (MQW). In some cases, a superlattice of a transition layer can be formed as a compositionally-graded superlattice or compositionally graded MQW. Embodiments also include transition layers that have any combination of the foregoing superlattice types. Any of the foregoing superlattice types may include carbon doping.

In some cases, a superlattice or combination of superlattices of the foregoing types can be present outside of a transition layer. In yet additional embodiments, a superlattice or combination of superlattices of the foregoing types can be present only and there may be no other transition layer.

In certain embodiments, the III-nitride material region comprises an optional III-nitride buffer layer. For example, referring to the exemplary embodiment of FIG. 1B, III-nitride material region 120 comprises III-nitride material buffer layer 180. It should be understood that buffer layer 180 is optional, and in other embodiments, III-nitride material region 120 does not include buffer layer 180.

The buffer layer can, according to certain embodiments, provide a surface for the growth of epitaxial III-nitride material above the buffer layer.

According to certain embodiments, the buffer layer comprises an aluminum gallium nitride material. In some such embodiments, the buffer layer comprises  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ . In certain embodiments in which the buffer layer comprises  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ ,  $x$  may be less than about 0.2, less than about 0.1, less than about 0.05, or less than about 0.01. In some embodiments, the buffer layer comprises GaN.

The buffer layer may be formed over the transition layer, for example, using any of a number of known growth techniques. For example, according to certain embodiments, the buffer layer may be formed over the transition layer using molecular-beam epitaxy (MBE) or metalorganic vapor phase epitaxy (MOVPE). In certain embodiments (including certain embodiments in which the desired epitaxial material structure will be used in the fabrication of devices such as field effect transistors (FETs), Schottky diodes, and/or High Electron Mobility Transistors (HEMTs)), it may be

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desirable to form a channel layer above the buffer layer. Typically, in some such embodiments, it would then be desirable for the buffer layer bandgap to be greater than or equal to the bandgap of the channel layer. For example, in certain transistor designs using back barriers, the channel layer may comprise gallium nitride while the buffer layer may comprise aluminum gallium nitride. In some such cases, the buffer layer may comprise a substantially uniform composition of AlGaN with a bandgap larger than the channel layer but smaller than the underlying transition layer alloy composition. In other examples, the buffer layer may itself be a compositionally graded layer which has a larger aluminum composition formed near the transition layer, and a smaller aluminum concentration formed near the channel layer.

In some embodiments, the composition of the channel layer and the buffer layer may be substantially the same. Although the intrinsic material properties of GaN materials can allow for the formation of high performance devices in theory, conventional growth environments of GaN nitride materials typically include impurity sources. For example, carbon impurities resulting from metalorganic precursors may be, in some cases, introduced into the GaN materials grown using MOCVD, also known more generically as organometallic vapor phase epitaxy (OMVPE). The presence of these impurities in the GaN growth environment can cause unintentional doping in or near critical device layers, for example the channel layer. In certain embodiments (e.g., including certain embodiments in which enhancing the standoff voltage is desired), it may be desirable to incorporate impurities into the buffer layer. For example, the addition of impurities such as carbon (C) and iron (Fe) into the buffer layers of gallium nitride based transistors may increase the vertical and lateral breakdown voltage capability and/or reduce the leakage levels of the device. However, addition of certain impurities within close proximity to the channel layer may result in dispersive device performance (e.g., exhibited by high levels of drain and gate lag). As such, in certain embodiments, it may be beneficial to form the buffer layer such that there is a substantially low impurity concentration throughout the thickness of the buffer layer. In certain other embodiments, there may be a graded (continuously or discontinuously) impurity level within the buffer layer, with a higher impurity concentration near the transition layer, and a lower impurity concentration formed nearer to the channel layer. In certain other embodiments, the transition layer(s) may also include one or more impurities. In some such embodiments, the concentration of impurities in the transition



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layer(s) may be higher than the concentration(s) of the impurities within the buffer layer and/or within the channel layer.

In certain embodiments, the III-nitride material region comprises an optional III-nitride device region. For example, referring to the exemplary embodiment of FIG. 1B, III-nitride material region 120 comprises III-nitride material device region 190. It should be understood that device region 190 is optional, and in other embodiments, III-nitride material region 120 does not include device region 190.

In some embodiments, the III-nitride material region includes at least one gallium nitride material layer. For example, in certain embodiments, the III-nitride material device region 190 comprises at least one gallium nitride material layer. Referring to FIG. 1B, for example, in some embodiments, III-nitride material device region 190 can include at least one gallium nitride material layer. As described further below, oftentimes, the structure includes more than one gallium nitride material layer which form, in part, the active region of a device.

As noted above, in some embodiments, the device region 190 comprises one or more III-nitride material layers. FIG. 1C is a cross-sectional schematic illustration of a III-nitride material device region 190, according to certain embodiments. In some embodiments, the III-nitride material device region comprises an optional back barrier layer. According to certain embodiments, when present, the optional back barrier layer is the layer of the III-nitride material region that is the closest to the underlying substrate. For example, in FIG. 1C, exemplary III-nitride material device region 190 comprises optional back barrier layer 190A, which as shown in FIG. 1C, is the closest of the layers within III-nitride material region to substrate 110. When used, the optional back barrier can create a double heterostructure (e.g., due to the bandgap off sets with the buffer layer, such as a GaN buffer layer). This may be desirable, in certain cases, in devices which operate under higher drain bias as they can prevent injection of electrons from the channel layer into the buffer layer, thereby reducing drain leakage and punch through of the device. Additionally, in some cases, the buffer layer may contain higher levels of impurities, intentionally (e.g., iron and carbon used to increase breakdown voltage) or unintentionally (e.g., carbon impurities incorporated into the buffer layer as byproducts from the crystal growth methodologies employed). These impurities and/or other defects may, in certain cases, act as trapping centers and cause deleterious performance results (e.g., memory effects) for the device if electrons from the channel layer penetrate into the

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underlying buffer layer. Back barrier layers can, in certain cases, help confine the electrons in the channel layer and prevent spill over into the more defective buffer layer and/or other underlying III-nitride layers. In certain embodiments, one or more AlGaN back barrier layers may be used. In certain embodiments, one or more InGaN back barrier layers may be used. In some embodiments, one or more AlInN back barrier layers may be employed. According to certain embodiments, the thickness of the back-barrier (either in the form of a single layer or a combination of layers) is in the range of about 1-300 angstroms.

In certain cases, the III-nitride material device region 190 (e.g., which may comprise at least one gallium nitride material layer) has a single crystal (i.e., monocrystalline) structure. In some cases, the III-nitride material device region (e.g., which may comprise at least one gallium nitride material layer) includes one or more layers having a Wurtzite (hexagonal) structure.

In some embodiments, the III-nitride material device region comprises an optional channel layer. The channel layer may be positioned, according to certain embodiments, over the back barrier layer when present. For example, in FIG. 1C, exemplary III-nitride material device region 190 comprises optional channel layer 190B, which as shown in FIG. 1C, is positioned over optional back barrier layer 190A. In other embodiments in which the back barrier layer is not present, the channel layer can be the layer within the III-nitride material device region that is closest to the underlying substrate. According to certain embodiments, the channel layer composition is selected with a smaller bandgap than either the spacer and or front-barrier layers (described in more detail below). Such arrangements can create a heterostructure forming a two-dimensional electron gas (2DEG) near the interface between the channel layer and an overlying layer (e.g., the spacer layer and/or the front barrier layer, described in more detail below). Such arrangements may be present, for example, in High Electron Mobility Transistors (HEMTs) and Schottky diodes. Electron flow through HEMTs and HFETs between the source and the drain of the device can, in some instances, be controlled by the gate of the device which acts to interrupt electron current flow between the source and drain. The channel layer can be formed, in certain cases, such that impurities or other point defects (which can act as trapping centers) are kept at a relatively low level, for example, to avoid impeding the mobility of the electrons and/or to avoid adding memory effects to the device. Trapping centers can adversely impact

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linearity in RF devices and turn-on and turn-off (switching) speeds in power management devices. The thickness of the channel layer can vary, for example, depending on the operational voltage desired for the device. As the drain voltage is increased, the depth of the depletion area between the gate and drain generally increases.

5 In certain cases, if the channel is formed too thin, punch through into the buffer layer can occur, which can result in drain leakage and breakdown of the device.

According to certain embodiments, the III-nitride material device region comprises an optional spacer layer (sometimes also referred to as an interlayer). The spacer layer may be positioned, according to certain embodiments, over the channel layer and/or the back barrier layer when present. For example, in FIG. 1C, exemplary III-nitride material device region 190 comprises optional spacer layer 190C, which as shown in FIG. 1C, is positioned over optional back barrier layer 190A and over optional channel layer 190B. In some embodiments, the interface between the channel layer and the spacer layer can form a 2-dimensional electron gas region (i.e., a “2DEG region”).

15 For example, in FIG. 1C, 2DEG region 191 is located at the interface of spacer layer 190C and channel layer 190B. Typically the spacer layer, when used, is formed with a high aluminum content. In some embodiments, the spacer layer is configured to have a relatively high bandgap offset with the underlying channel layer (e.g., by using a relatively high aluminum content in the spacer layer), which can lead to enhancement of the 2DEG. In certain embodiments, the spacer layer comprises  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ . In certain such embodiments,  $(1-x) = 0.5$  or greater. In some embodiments, the spacer layer comprises AlN. According to certain embodiments, the spacer layer is relatively thin (for example, less than about 50 Angstroms, less than about 20 Angstroms, or less). The use of a relatively thin spacer layer can avoid, in some cases, adversely impacting the ohmic

20 contact resistance of the source and drain to the 2DEG and channel layer of the device.

The III-nitride material device region comprises, in some embodiments, an optional front barrier layer. The front barrier layer may be positioned, according to certain embodiments, over the spacer layer, the channel layer, and/or the back barrier layer when present. For example, in FIG. 1C, exemplary III-nitride material device region 190 comprises optional front barrier layer 190D, which as shown in FIG. 1C, is positioned over optional back barrier layer 190A, over optional channel layer 190B, and over optional spacer layer 190C. According to certain embodiments (and as described above), if the device structure is a HEMT and/or if a 2DEG is desired, the optional front-

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barrier 190A can be formed over the channel layer 190B (or spacer layer 190C, if used) to form a heterojunction. The composition of the front-barrier is selected, according to certain embodiments, such that the carrier density and/or sheet charge of the 2DEG is tailored (e.g., optimized) for the device desired. In certain embodiments, the front-  
5 barrier layer comprises AlGaN. According to certain embodiments in which an AlGaN-containing front-barrier layer is used, the aluminum concentration of the AlGaN front-barrier is less than about 30 atomic percent (at%), less than about 25 at%, or between about 15 at% and about 20 at%. In certain embodiments, it may be desirable to match or substantially match the lattice constant between the channel and the front-barrier, and to  
10 maintain a bandgap offset, for example, to create a 2DEG. In some such cases, an AlInN or InGaN front-barrier layer can be created to provide the bandgap offset and match or substantially match the lattice constants.

According to some embodiments, the III-nitride material device region comprises an optional cap layer. The cap layer may be positioned, according to certain  
15 embodiments, over the front barrier layer, the spacer layer, the channel layer, and/or the back barrier layer when present. For example, in FIG. 1C, exemplary III-nitride material device region 190 comprises optional cap layer 190E, which as shown in FIG. 1C, is positioned over optional back barrier layer 190A, over optional channel layer 190B, over optional spacer layer 190C, and over optional front barrier layer 190D. Cap layers have  
20 been found useful in optimizing the semiconductor surface of the device structure, according to certain embodiments. For example, in certain cases in which the cap layer(s) comprises GaN, the resulting surface morphology may be smoother and/or include fewer defects, relative to surfaces formed when the cap layer(s) is not present. In addition, in some cases, a more uniform source composition may also be provided (i.e.,  
25 terminated with gallium atoms rather than a mixture of gallium and aluminum atoms), which may, in some instances, aid in surface chemistry processing of the semiconductor surface and/or reduce the number of surface defects under the gate of the HFET. Such surface defects may, for example, act as shallow trapping centers and compromise the performance of the device, for example, due to increased gate leakage or lateral  
30 breakdown of the device, increased dispersion, increased gate and drain lag of the device, amongst other reductions in performance. Additionally, in certain cases, by providing a more consistently terminated semiconductor surface, the repeatability and consistency of the contact resistance may be enhanced, which can lead to higher manufacturing yields.

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In some embodiments, it may be desired to dope the cap layer(s). In some instances in which the barrier is doped, it may be desirable to use a GaN cap layer which is n-type doped (e.g., using silicon). The use of an n-type doped cap layer may, according to certain embodiments, reduce  $I_{dss}$  degradation of the device. In some embodiments, the cap layer(s) may comprise a conductive GaN material layer, for example, used as a conductive field plate.

In certain embodiments, the cap layer(s) 190E may be doped p-type, for example, with magnesium. Such doping may be desirable, for example, in certain cases in which a normally OFF or enhancement mode HFET is being fabricated. As one non-limiting example, by forming a localized p-type GaN region under the gate of the HFET, the 2DEG can be disrupted and the channel depleted such that under no bias, the device is normally off. In some such cases, a positive bias to the gate would then be needed to restore the 2DEG locally under the gate and allow current flow from the source to the drain. It should be noted that one or more layers may be used as the cap layer(s), and that whether a single cap layer or multiple cap layers are employed may depend, for example, on the specifics of the design device structure.

In some embodiments, the cap layer may include an in-situ silicon nitride cap layer and/or passivation layer. Such layer(s) may be used to terminate the III-Nitride structure and/or stabilize the surface of the GaN material.

In some embodiments, the III-nitride material device region 190 comprises at least two device layers. In some embodiments, the first device layer can be the closest of two or three layers to the substrate. If three layers are present, the second device layer can be an intermediate layer (i.e., between the first device layer and a third device layer), and the third device layer can be the farthest of the three layers from the substrate. In some such embodiments, the first layer can be a channel layer, the second device layer can be a front-barrier layer, and the third device layer can be a cap layer. In some embodiments, the cap layer may not be present. Referring to FIG. 1C, for example, III-nitride material device region 190 can comprise channel layer 190B, front-barrier layer 190D, and cap layer 190E. In some such embodiments, back-barrier layer 190A and spacer layer 190C are each optional, and one or both may be present or not present. According to some such embodiments, channel layer 190B can be the closest of these three layers (i.e., channel layer 190B, front barrier layer 190D, and cap layer 190E) to the underlying substrate. In certain embodiments, it may be preferable for the second device

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layer to have an aluminum concentration that is greater than the concentration of aluminum in the first layer and/or the third layer. For example, referring to FIG. 1C, in some embodiments, front-barrier layer 190D can have an aluminum concentration that is greater than the concentration of aluminum in channel layer 190B and cap layer 190E.

5 In some embodiments, the first and second layers (e.g., channel layer 190B and front-barrier layer 190D in FIG. 1C, respectively) can be gallium nitride material layers, and the value of  $x$  (as used elsewhere herein with reference to gallium nitride material layers, in subscripts to denote the relative amount of aluminum in a compound (e.g., the “ $x$ ” in  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ )) in the second gallium nitride material layer may have a value that is  
10 between about 0.15 and about 0.3 greater, or between about 0.15 and about 0.75 greater than the value of  $x$  in the first gallium nitride material layer. For example, the second device layer may be formed of  $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ , while the first device layer may be formed of GaN. This difference in aluminum concentration may lead to formation of a highly conductive region at the interface of the second and first device layer (i.e., a 2DEG  
15 region). In some embodiments, the first device layer may be formed of GaN.

According to certain embodiments, the III-nitride material device region (e.g., which may comprise at least one gallium nitride material layer) has a low crack level. As described above, the transition layer (particularly when compositionally-graded) and/or the nucleation layer may reduce crack formation. Gallium nitride materials and  
20 other III-nitride materials having low crack levels have been described, for example, in U.S. Pat. No. 6,649,287, which is incorporated herein by reference in its entirety for all purposes. In some cases, the III-nitride material device region (e.g., which may comprise at least one gallium nitride material layer) has a crack level of less than  $0.005 \mu\text{m}/\mu\text{m}^2$ . In some embodiments, the III-nitride material device region (e.g., which may comprise at  
25 least one gallium nitride material layer) has a very low crack level of less than  $0.001 \mu\text{m}/\mu\text{m}^2$ . In certain cases, it may be preferable for the III-nitride material device region (e.g., which may comprise at least one gallium nitride material layer) to be substantially crack-free as defined by a crack level of less than  $0.0001 \mu\text{m}/\mu\text{m}^2$ .

The optional III-nitride material nucleation layer, the optional III-nitride material transition layer, and the optional III-nitride material buffer layer are not typically (though  
30 may be) part of the active region of devices formed from structures of the embodiments described herein. As described above, these layers may be formed to facilitate deposition of the layer(s) of the III-nitride material device region.

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Active regions of devices formed from certain of the structures described herein may be formed, in part, in one or more layers of the III-nitride material device region (e.g., gallium nitride material layers). Suitable gallium nitride material layer arrangements have been described, for example, in U.S. Patent No. 7,071,498, entitled  
5 “Gallium Nitride Material Devices Including an Electrode-Defining Layer and Methods of Forming the Same,” issued on July 4, 2006, which is incorporated herein by reference in its entirety for all purposes. Other commonly used III-nitride material device layers include channel layers, spacer layers, barrier layers, capping layers, and P-type layers used under the gate electrodes used for the design of enhancement mode (normally OFF)  
10 transistor designs. These III-nitride material device layers may also include, according to certain embodiments, intentionally doped layers in addition to various III-nitride layers exhibiting different alloy compositions.

According to some embodiments, a semiconductor structure can comprise a second III-nitride material region 120. In certain embodiments, the semiconductor  
15 structure comprises a second III-nitride material region over the III-nitride material region 120 (second III-nitride material region not shown in FIG. 1A and 1B). In certain embodiments, the second III-nitride material region is an epitaxial III-nitride material region. In some embodiments, the second III-nitride material region comprises a III-nitride device region. According to some embodiments, the second III-nitride material  
20 region comprises a 2DEG.

The semiconductor structures described herein may, according to certain embodiments, form the basis of a variety of integrated semiconductor devices and/or discrete components (e.g., capacitors, resistors, thermistors, microstrip transmission lines, and inductors). Suitable devices include, but are not limited to, active devices like  
25 transistors (e.g., field effect transistors (FETs); either enhancement or depletion mode), Schottky diodes, junction diodes, PIN diodes, as well as light-emitting devices including light emitting diodes (LEDs) and laser diodes. Likewise, suitable devices also include integrated circuits (e.g., monolithic microwave integrated circuits (MMICs) having combinations of two or more active devices and/or discrete components, e.g., for  
30 assembly of front end modules (FEMs). It may be particularly advantageous, according to certain but not necessarily all embodiments, to use structures of the invention in devices that operate at high frequencies (e.g., at frequencies of 50 MHz or higher for certain power management applications, at frequencies of 1 GHz or higher (e.g., up to 20

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GHz) for certain RF applications). Other non-limiting examples of RF applications include discretes and integrated circuits used for transmit and receive functions associated wireless and wireline communications, RF energy, RF plasma lighting, wireless charging, RF induction and microwave heating, RF spark-plugs, ISM, medical devices, RADAR, and electronic warfare and countermeasure devices. Additional applications using III-nitride devices operating at lower frequencies include power management discretes, devices, and integrated circuits used to switch, rectify, monitor, or control electric power from a source to a load (e.g., buck converters, boost converters, half bridges, H-bridges, full bridges, three-phase bridges and multi-phase bridges). Such power management devices can operate at frequencies down to 1 MHz or lower (e.g., down to about 50 kHz). In certain embodiments, there may be integrated circuits and/or multiple dice on a chip combining both RF devices and switching devices used to monitor, switch, or control the electric power delivery from a source to a load.

According to certain embodiments, the devices have active regions that are typically, at least in part, formed within the III-nitride material region (e.g., in one or more layers of the III-nitride material device region, such as one or more gallium nitride material layers). According to some embodiments, the devices include a variety of other functional layers and/or features (e.g., electrodes, dielectric regions, field plate layers, etc.).

According to certain embodiments, semiconductor devices can comprise the semiconductor structures described herein. Example devices include a transistor (e.g., a field effect transistor (FET)) or a diode. The transistor can comprise, according to certain embodiments, a source electrode and a drain electrode. The source electrode and the drain electrode can be electronically isolated from each other. For example, in some embodiments, the source electrode and the drain electrode are spatially separated. In some embodiments, the transistor further comprises a gate electrode. The gate electrode may be a Schottky gate or an insulated gate electrode. According to certain embodiments, during use, application of a voltage at the gate electrode can create and/or modify an electric field at least partially positioned between the source electrode and the drain electrode, such that electrons are transferred from the source electrode to the drain electrode.

Suitable transistors (e.g., FETs) that may be used in association with certain of the embodiments described herein include depletion mode (normally-ON) transistors and



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enhancement mode (normally OFF) transistors. A transistor can be associated with any of the semiconductor structures described elsewhere herein, including but not limited to those described with respect to FIGS. 1A-1C.

FIG. 2A is a cross-sectional schematic illustration of a portion of an exemplary semiconductor device 200A comprising a semiconductor structure, according to certain 5 embodiments. In this example, the illustrated device 200A includes elements of a transistor, though the invention is not limited to only transistors. The inventive embodiments of semiconductor structures described herein can be applied to diodes, PIN switches, integrated inductors, and integrated capacitors, for example. The structure 10 shown in FIG. 2A is also not limited to transistors. Such structure can be used for a diode, as described in U.S. patent publication No. 2017/0301798, titled “High Voltage Lateral GaN-on-Silicon Schottky Diode,” filed July 29, 2016, which is incorporated herein by reference. For example, the gate electrode 260 can be used as an anode electrode of a Schottky diode. The source electrode 220 and drain electrode 230 can be 15 electrically connected together and serve as cathodes for the diode.

FIGS. 3A-3H are top, perspective-view schematic illustrations of contacts and electrodes that can be patterned on the semiconductor device of which device 200A shown in FIG. 2A is a part, with the cross-section shown in FIG. 2A taken along line “2A” illustrated in FIGS. 3G and 3H. FIGS. 3A-3H represent a schematic progression of 20 the addition of various components to the semiconductor device.

In FIG. 3A, a plurality of electrode pairs 215 have been added over III-nitride material region 120. According to certain embodiments, each of the electrode pairs (e.g., components of a transistor) has a source electrode and a drain electrode, each of which define ohmic contacts with an underlying III-nitride material region. As shown in FIG. 25 3A, semiconductor device 200A comprises six electrode pairs 215A-215F, wherein each electrode pair 215A-215F comprises source electrodes 220A-220F and drain electrodes 230A-230F. The source electrodes make ohmic contacts with the underlying III-nitride material region. For example, in FIG. 2A, source electrode 220 makes ohmic contact 302A with III nitride material 120. The drain electrodes also make ohmic contacts with the underlying III-nitride material region. For example in FIG. 2A, drain electrode 230 30 makes ohmic contact 302B with III-nitride material region 120. Electrode pairs 215A-215F may be, in accordance with various embodiments, evenly and/or non-evenly spaced on III-nitride material region 120.

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In FIG. 3B, the electrode pairs have been removed to illustrate the interfacial areas between the electrode structures and the underlying semiconductor material (i.e., the ohmic contact interfacial areas), described in more detail below.

FIG. 3C is a top, perspective-view schematic illustration of the semiconductor structure of FIG. 3A, but in which gate electrodes 240A-240F have been added relative to the structure shown in FIG. 3A. In FIG. 3C, gate electrodes 240A-240F have been added between each of electrode pairs 215A-215F (each electrode pair including a source electrode 220 and a drain electrode 230), creating transistors 210A-210F.

In FIG. 3D, gate contact pad 244, which establishes electrical connections to gate contacts 240, has been added.

In FIG. 3E, drain contact pad 234, which establishes electrical connections to drain contacts 230, has been added.

In FIG. 3F, source contact pads 224A-224D, which establish electrical connections to source contacts 220, have been added.

FIG. 3G is a top, perspective-view schematic illustration of the completed device, with FIG. 3H showing a magnified view of portion 350.

In certain embodiments, as shown in FIG. 3C-3H, the semiconductor structure comprises multiple transistors. In other embodiments, the semiconductor structure includes only a single transistor. When multiple transistors are present, any suitable number of transistors (e.g. one, two, three, four, or more) can be present.

Referring back to FIG. 2A, transistor 210 comprises source electrode 220 and drain electrode 230. Transistor 210 also comprises gate electrode 240. Source electrode 220, drain electrode 230, and gate electrode 240 are positioned on III-nitride material region 120. The device also includes dielectric region 250. The dielectric region can be a passivating layer that protects and passivates the surface of the III-nitride material region. Via 260 is formed within the dielectric region 250 in which gate electrode 240 is, in part, formed. In FIG. 2A, as described above, III-nitride material region 120 is formed directly on substrate 110. It is also noted that the configuration of gate electrode 240 in direct contact with the III-nitride material device region 120 forms a Schottky-gated FET. In other embodiments (not shown in FIG. 2A) there may be an insulator layer formed between gate electrode 240 and III-nitride material device region 120 configured as a Metal Insulated Field Effect Transistor (MISFET) or more generically an insulated gate transistor. It should also be noted that, although FIG. 2A shows via 260

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formed within dielectric region 250, in certain other embodiments, via 260 could extend down and terminate within III-nitride material region 120.

The transistor structures illustrated in FIGS. 2A-2D (and FIGS. 3A-3H) are exemplary, and other structures could also be used. For example, according to some  
5 embodiments, a single transistor comprising a semiconductor structure described herein may be located over the surface region of the substrate. In some embodiments, at least one second transistor or at least one diode comprising a semiconductor structure described herein can be located over the substrate and laterally spaced apart from the first transistor.

10 As noted above, certain embodiments are related to systems and methods for mitigating the impact of temperature increases on device performance. The maximum junction temperature in III-nitride materials on silicon substrates is typically fundamentally limited by junction reliabilities within the semiconductor device, and more specifically, by the substrate (e.g., silicon-containing substrate) resistivity at  
15 elevated temperatures. In certain cases, a resistive silicon-containing substrate at the epitaxial interface heats up under RF operation and elevated temperatures, and conducts RF current that degrades product performance such as output power and efficiency. In some cases, “high resistivity” silicon does not retain its high resistivity properties above 50 °C. For example, 10kΩ·cm high resistivity silicon at 25 °C becomes 100Ω·cm at 177  
20 °C. As a result, in certain cases, current through the transistor (i.e., dissipated power) generates heat that spreads into the substrate from the III-nitride material.

In certain cases, the substrate is capacitively coupled with conductive structures (e.g., source, drain, or gate electrodes, associated contact pads, etc.), for example, at the  
25 III-nitride material interface. In some such cases, application of an RF voltage across the drain electrode to the source electrode generates heat in the substrate, leading to thermal runaway by increasing the heat source temperature and reducing the substrate resistance even further.

Effectively, in certain instances, as the temperature of the package flange and/or supply voltage of the semiconductor device is increased, the substrate resistance is  
30 decreased, and as a result the semiconductor structure has both lower output power and lower efficiency. RF induced substrate power dissipation is a strong function of supply voltage, and the power dissipated in the silicon-containing substrate is proportional to the

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square of the peak RF voltage, leading to significant performance degradation for semiconductor structures containing highly resistive silicon-containing substrates.

In some cases, when a voltage is applied to a semiconductor device, current is generated within the semiconductor structure between at least two electrodes (e.g.,  
5 between a source electrode and a drain electrode). The flow of current within the semiconductor structure is generally dictated by Ohm's law, which dictates that the current is inversely proportional to the resistance. In some cases, the passage of electrical current through the semiconductor structure produces heat (also referred to as Joule heating or resistive heating); in this process, electric current energy is converted to  
10 heat through resistive losses (e.g., dissipated power) in the substrate of the semiconductor structure.

As discussed above, certain of the devices and semiconductor structures described herein comprise electronically conductive substrates (e.g., electronically conductive substrates comprising bulk silicon). The electrical resistance in the substrate  
15 can be reduced by the use of electronically conductive substrates (e.g., as the conductivity of the substrate increases, the resistance of the substrate decreases). As a result, the resistive heating of the semiconductor structure is lowered, resulting in semiconductor devices and semiconductor structures with less performance degradation and better efficiencies at higher operating temperatures, which is explained in more  
20 detail herein.

In certain embodiments, semiconductor structures comprising thick III-nitride material regions are described. The use of thick III-nitride materials can reduce leakage current between the substrate and components of a device that is formed using a semiconductor structure described herein. As a result, in some embodiments, the use of  
25 thick III-nitride layers can reduce the degree to which electrons are transported, undesirably, between the substrate and electronically conductive structures on the III-nitride material surface.

In some cases, ohmic contacts are present between electrode structures (e.g., metal structures) and the III-nitride material region, and in certain cases, the ohmic contact areas capacitively couple RF current to the electronically conductive substrate.  
30 In some cases, capacitive coupling results from the transfer of energy within the electrical network of the semiconductor structure by means of displacement current

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between transistor components incorporated in the semiconductor structure (e.g., a source electrode and/or a drain electrode) and the substrate.

According to certain embodiments, the capacitive coupling and displacement current generated during operation of the semiconductor structure can be decreased by the use of small ohmic contacts over the III-nitride material surface. Reduced ohmic contact interfacial areas on the III-nitride material surface have the effect, in accordance with certain embodiments, of lowering the amount of dissipated current transported through the substrate of the semiconductor structure.

Some embodiments described herein are related to the use of small ohmic contacts with large contact pads. In certain embodiments, the contact pads are present above and electrically connect to the electrode structures (e.g., metal structures) that make ohmic contacts with the III-nitride material surface. According to certain embodiments, large contact pads are useful for making external electrical connections to the semiconductor device.

In certain embodiments, the contact pads described above are present on a thick dielectric region that separates the large contact pads from the III-nitride material region. According to some embodiments, the use of a thick dielectric region between the large contact pads and the III-nitride material region can reduce the capacitance to the electronically conductive substrate, resulting in higher operating temperatures and better efficiencies at said temperatures.

Certain of the semiconductor structures described herein can be “self-grounding,” for example, by including an electrical coupling between an electronically conductive component (e.g., on the top side of the device, such as an electrode or a contact pad) and the electronically conductive substrate (or an electronically conductive portion of the substrate). For example, in some embodiments, the semiconductor structures include a cavity formed in the top portion of the device. The cavity can be, in accordance with certain embodiments, a front-side via (also referred to as a top-side via). The cavity can be configured to expose the electronically conductive substrate (or an electronically conductive portion thereof), for example by extending through the III-nitride material region. In some embodiments, an electronically conductive material (e.g., a metal) can be disposed such that it establishes an electronically conductive grounding pathway between an electronically conductive component on the top side of the device to the electronically conductive substrate (or an electronically conductive portion of the

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substrate). The electronically conductive pathway between the electronically conductive component and the substrate can ensure that charge does not accumulate in an unwanted location, and can help limit the amount of power dissipated during operation. This arrangement can result in a “self-grounding” structure where no external electrical connection, such as a wire, is required to ground the device.

Certain embodiments are related to semiconductor structures comprising a substrate, at least a portion of which is electronically conductive. Referring back to FIGS. 2A, substrate 110 can be an electronically conductive substrate (e.g., a bulk silicon substrate) and/or may include a portion that is electronically conductive. In some embodiments, the use of substrates having electronically conductive regions can reduce the amount of heat that is generated during device operation. For example, in some cases, as a voltage is applied to the semiconductor structure, an electrical current is generated between at least two electrode structures, such as a source electrode and a gate electrode. Additionally, current can also be (undesirably) transported through the substrate. As current is transported through the substrate, heat can be generated (for example, due to Joule heating). In the case of highly resistive substrates, the generation of heat can result in a decrease in resistivity, which can result in an increase in the current transported through the substrate (which still remains relatively highly resistive), increased Joule heating, and increased substrate temperatures. In certain embodiments described herein, however, the use of substrates having electronically conductive regions can allow for current to be transferred through the substrate relatively efficiently, with little or no Joule heating. The relatively efficient transport of electrical current through the substrate can improve the efficiency of devices and components formed from the semiconductor structure, for example, even at relatively high operating temperatures.

In certain embodiments, the devices having semiconductor structures described herein comprise at least one ohmic contact located over the III-nitride material region. Certain devices (e.g., Schottky diodes and HEMTs) can also include Schottky contacts at the anode and gate, respectively. Referring to FIGS. 2A and 3A-3B, semiconductor device 200A comprises ohmic contacts 302A and 302B located over III-nitride material region 120. In certain embodiments, the ohmic contacts are an electrical junction between an electrode structure (e.g., a source electrode and/or a drain electrode of a transistor) and an underlying portion of the semiconductor structure (e.g., the III-nitride material region). In some cases, capacitive coupling occurs between the ohmic

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contact(s) and the substrate. The capacitive coupling between the ohmic contact(s) and the substrate can lead to the displacement current flowing through the substrate, resulting in dissipated power.

5 In some embodiments, as the ohmic contact area of the at least one ohmic contact decreases, the capacitive coupling between the ohmic contact(s) and the substrate decreases. In some such cases, less displacement current is transported through the substrate. Accordingly, in accordance with certain embodiments, the semiconductor devices described herein comprise ohmic contacts that are relatively small, which can help reduce capacitive coupling losses.

10 It should be understood that an ohmic contact that is “over” a III-nitride material region can sit on top of the III-nitride material region or be at least partially embedded in the III-nitride material region. For example, referring to FIGS. 2A, ohmic contact 302A and ohmic contact 302B are embedded in III-nitride material region 120. FIG. 2C is, in accordance with certain embodiments, a side-view schematic illustration of a  
15 semiconductor device with ohmic contacts on top of the III-nitride material region. In some embodiments, such as those illustrated in FIG. 2C, ohmic contact 302A and ohmic contact 302B sit on top of III-nitride material region 120.

According to certain embodiments, at least one ohmic contact defines an ohmic contact interfacial area with the III-nitride material region. The ohmic contact interfacial  
20 area of a given ohmic contact type (e.g., drain ohmic contact) refers to the area of the interface between the ohmic contact or contacts of the same type in a device and the III-nitride material. The ohmic contact interfacial area of a device (also referred to herein as the “device ohmic interfacial area”) refers to the sum of all of the interfacial areas of the ohmic contacts of that device. For example, in the case of a transistor having a source  
25 electrode and a drain electrode, the device ohmic contact interfacial area for that device would correspond to the sum of the ohmic contact interfacial areas of all ohmic contacts for the source electrode and the drain electrode. The ohmic contact interfacial area of that transistor device would not include the interfacial area of the gate electrode, since in some cases the gate electrode may form a Schottky contact or a capacitive contact, rather  
30 than an ohmic contact.

Referring to FIGS. 2A, for example, ohmic contact 302A of source electrode 220 has interfacial area 308, and ohmic contact 302B of drain electrode 230 has interfacial area 309. In addition, Schottky contact 303 of gate electrode 240 for the depicted type of

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transistor has interfacial area 310. FIG. 2D is a top-view schematic illustration of the semiconductor device illustrated in FIG. 2A (with the cross-sections shown in FIG. 2A taken along line 2A in FIG. 2D). In FIG. 2D, ohmic contact 302A of source electrode 220 has interfacial area 308, where source electrode 220 contacts III-nitride material region 120. In FIG. 2D, ohmic contact 302B of drain electrode 230 has interfacial area 309, where drain electrode 230 contacts III-nitride material region 120. Schottky contact 303 of gate electrode 240 has interfacial area 310, where gate electrode 240 contacts III-nitride material region 120.

Ohmic contact interfacial areas are further shown in FIG. 3B. In FIG. 3B, source electrodes 220A-220F that make ohmic contacts 302A with underlying III-nitride material region and drain electrodes 230A-230F that each make an ohmic contact 302B with underlying III-nitride material region 120 have been removed (relative to FIG. 3A) for purposes of clarity, and to illustrate the interfacial areas defined by the electrodes of the electrode pairs. Referring to FIG. 3B, each of areas 308A-308F and 309A-309F correspond to the interfacial area defined by one of the ohmic contacts (e.g., 302A and 302B) from FIG. 3A. For example, in FIG. 3B, electrode pair 215A comprises interfacial area 308A that is defined by ohmic contact 302A of source electrode 220A, and interfacial area 309A that is defined by ohmic contact 302B of drain electrode 230A. In certain embodiments, each electrode pair 215A-215F comprises interfacial areas 308A-308F and 309A-309F. Where there are multiple electrodes of a same type (e.g., drain, source, cathode) present in a device, the ohmic contact interfacial area for a type of an electrode is a sum of all constituent ohmic contact interfacial areas for electrodes of a same type. For example, a drain ohmic contact interfacial area for the device of FIG. 3B would be a sum of interfacial areas 309A-309F.

The ohmic contact interfacial area can generally be calculated by examining a top-down view of the semiconductor device and determining the geometric area of the III-nitride region that is covered by the conductive material forming the ohmic contact with the III-nitride region.

The interfacial areas of the ohmic contacts can have any of a variety of suitable shapes including, but not limited to, square, rectangular, circular, and the like.

According to certain embodiments, the ohmic contact interfacial area of the device is less than  $50 \mu\text{m}^2$ , less than  $40 \mu\text{m}^2$ , less than  $30 \mu\text{m}^2$ , less than  $20 \mu\text{m}^2$ , or less



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than  $10 \mu\text{m}^2$ . In certain embodiments, the ohmic contact interfacial area of the device is greater than  $1 \mu\text{m}^2$ , greater than  $10 \mu\text{m}^2$ , greater than  $20 \mu\text{m}^2$ , greater than  $30 \mu\text{m}^2$ , or greater than  $40 \mu\text{m}^2$ . Combinations of these ranges are also possible (e.g., less than  $40 \mu\text{m}^2$  and greater than  $20 \mu\text{m}^2$ , less than  $30 \mu\text{m}^2$  and greater than  $10 \mu\text{m}^2$ ).

5           According to some embodiments, an ohmic contact interfacial area ratio can be defined for a device. For example, an ohmic contact interfacial area ratio can be defined as a ratio of the ohmic contact interfacial area of at least one type of ohmic contact for a device (e.g., interfacial area of a source or drain of a transistor or interfacial area of a cathode for a Schottky diode) to a peripheral length of a gate or anode for the device.

10          For example and referring to FIG. 2A and FIG. 2D, an ohmic contact interfacial area ratio for a transistor can be a ratio of a drain interfacial area 309 to a gate peripheral length  $L$  that is measured transverse to the direction of current flow under the gate electrode 240. In this regard, gate peripheral length  $L$  is measured in a direction that is transverse to conventional “gate length.” If a device has more than one gate or anode,

15          then the peripheral length for the device will be the sum of all peripheral lengths for the constituent gates (e.g., 240A-240F as depicted in FIG. 3C) or anodes for the device. For a diode, anode peripheral length would correspond to a length of the anode (or all anodes of the device) measured transverse to the direction of current flow from the anode. If an ohmic contact for a device comprises a plurality of ohmic contacts of a particular type

20          (e.g., a plurality of drain contacts, as described in connection with FIG. 3A for example) then the ohmic contact interfacial area for the device is a sum of all relevant ohmic contact interfacial areas (e.g., a sum of ohmic contact interfacial areas 309A-309F for drain contacts of the device) divided by the peripheral length of a selected terminal for the device. For a transistor, an ohmic contact interfacial area ratio can be calculated for

25          the drain contact(s). Additionally or alternatively, an ohmic contact interfacial area ratio can be calculated for the source contact(s).

          The units of an ohmic contact interfacial area ratio (and other area-to-peripheral length ratios described herein) can be expressed in square microns/micron ( $\mu\text{m}^2/\mu\text{m}$ ) or ( $\mu\text{m}$ ), where the size of the ohmic contact interfacial area and the peripheral length are

30          both measured in microns. Other units may be used to express area-to-peripheral length ratio with a corresponding change in ratio value.

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In some implementations, devices formed in accordance with the present embodiments can have an ohmic contact interfacial area ratio for at least one type of ohmic contact of the device. An ohmic contact interfacial area ratio can be between 1  $\mu\text{m}^2/\mu\text{m}$  and 30  $\mu\text{m}^2/\mu\text{m}$ . The ohmic contact interfacial area ratio for at least one type of ohmic contact of a device can be less than 5  $\mu\text{m}^2/\mu\text{m}$  according to some embodiments, less than 10  $\mu\text{m}^2/\mu\text{m}$  according to some embodiments, less than 20  $\mu\text{m}^2/\mu\text{m}$  according to some embodiments, and yet less than 40  $\mu\text{m}^2/\mu\text{m}$  according to some embodiments.

According to certain embodiments, the semiconductor devices described herein comprise components of transistor, including a source electrode over the III-nitride material region. For instance, referring to FIGS. 2A, semiconductor device 200A comprises source electrode 220 over III-nitride material region 120. In certain embodiments, the source electrode defines a source electrode interfacial area with the III-nitride material region. The source electrode interfacial area corresponds to interfacial area of the ohmic contact between the source electrode and the III-nitride material region. For example, referring to FIG. 2A and FIG. 2D, source electrode 220 has interfacial area 308.

In some embodiments, the semiconductor devices described herein comprise a drain electrode over the III-nitride material region. For instance, referring to FIGS. 2A, semiconductor device 200A comprises drain electrode 230 over III-nitride material region 120. In certain embodiments, the drain electrode defines a drain electrode interfacial area with the III-nitride material region. The drain electrode interfacial area corresponds to the interfacial area of the ohmic contact between the drain electrode and the III-nitride material region. Referring to FIGS. 2A and FIG. 2D, for example, drain electrode 230 has interfacial area 309.

According to certain embodiments, the semiconductor devices described herein comprise a gate electrode over the III-nitride material region. For instance, referring to FIGS. 2A, semiconductor device 200A comprises gate electrode 240 over III-nitride material region 120. In certain embodiments, the gate electrode defines a gate electrode interfacial area with the III-nitride material region. The gate electrode interfacial area corresponds to the interfacial area of the contact between the gate electrode and the underlying material, which could be the III-nitride material or an intermediate material

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between the gate electrode and the III-nitride material.. Referring to FIGS. 2A and FIG. 2D, for example, gate electrode 230 has interfacial area 310.

According to some embodiments, it may be beneficial to have an ohmic contact interfacial area that is less than 50 times the gate electrode interfacial area because  
5 reduced interfacial areas of the source and drain ohmic contacts on the III-nitride material surface can reduce the capacitive coupling to the substrate (e.g., an electronically conductive substrate). In certain embodiments, the ohmic contact interfacial area defined by the source electrodes is less than 50 times (or less than 40 times, less than 30 times, less than 20 times, less than 10 times, or less than 5 times) the  
10 Schottky contact interfacial area defined by the gate electrodes. In some embodiments, the ohmic contact interfacial area defined by the source electrodes is at least 0.01 times, at least 0.1 times, or at least 1 time the Schottky contact interfacial area defined by the gate electrodes. Combinations of these ranges are also possible.

For example, referring to FIG. 2D, the ohmic contact interfacial area 308 defined  
15 by source electrode 220 is less than 50 times the Schottky contact interfacial area 310 defined by the gate electrode. To calculate the ratio of the ohmic contact interfacial area defined by the source electrodes to the Schottky contact interfacial area defined by the gate electrodes, one would determine the ratio of:

- (1) interfacial area 308 defined by source electrode 220 to
- 20 (2) interfacial area 310 defined by gate electrode 240.

According to certain embodiments, the ohmic contact interfacial area defined by the drain electrodes is less than 50 times (or less than 40 times, less than 30 times, less than 20 times, less than 10 times, or less than 5 times) the Schottky contact interfacial area defined by the gate electrodes. In some embodiments, the ohmic contact interfacial  
25 area defined by the drain electrodes is at least 0.01 times, at least 0.1 times, or at least 1 time the Schottky contact interfacial area defined by the gate electrodes. Combinations of these ranges are also possible. For example, referring to FIG. 2D, the ohmic contact interfacial area 309 defined by drain electrode 230 is less than 50 times the Schottky contact interfacial area 310 defined by the gate electrode. To calculate the ratio of the  
30 ohmic contact interfacial area defined by the drain electrodes to the Schottky contact interfacial area defined by the gate electrodes, one would determine the ratio of:

- (1) interfacial area 309 defined by drain electrode 230 to
- (2) interfacial area 310 defined by gate electrode 240.

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In certain embodiments, the ohmic contacts define an active area. For example, in embodiments in which the semiconductor device comprises a transistor, the source electrode and the drain electrode define an active area. The active area generally refers to the area over which electrons are transported between ohmic contacts during normal operation of the semiconductor structure. For example, in the case of a transistor, the active area refers to the area under and between the source and the drain electrodes over which electrons are transported during device operation.

One example of an active area is shown in FIGS. 2A. In FIGS. 2A, the active area 306 is the area over which the drain current is transported between ohmic contacts 302A and 302B. In certain embodiments, the active area of a semiconductor device includes the area both beneath the ohmic contact, as well as the area between them. For example, referring to FIGS. 2A, ohmic contact active area 306 includes the area beneath ohmic contacts 302A and 302B, as well as the area between ohmic contacts 302A and 302B.

The active area shown in FIGS. 2A is also shown in the top-view schematic illustration of FIG. 2D. In FIG. 2D, semiconductor device 200A comprises source electrode 220, drain electrode 230, and gate electrode 240. Source electrode 220 and drain electrode 230 define active area 306, denoted by dotted box 307.

Exemplary active areas are also shown in the top, perspective view schematic illustration shown in FIG. 3B. In FIG. 3B, each electrode pair 215A-215F comprises ohmic contacts 302A and 302B where source electrode 220A-220F and drain electrode 230A-230F contact the III-nitride material region 120. (See FIG. 3A). As shown in FIG. 3B, in some embodiments, each electrode pair 215A-215F has an active area (306A-306F), which are denoted by dotted boxes.

The active area of a given semiconductor device can be defined by a single continuous region or a plurality of regions (as shown in FIGS. 3A-3H). In instances in which a plurality of regions define the active area of the semiconductor device, the active area of the device (also referred to herein as the “cumulative active area” of the device) is calculated by summing the areas of the individual active area regions in the semiconductor device. For example, referring to FIG. 3B, the cumulative active area of semiconductor device 200A would be determined by adding the areas of regions 306A, 306B, 306C, 306D, 306E, and 306F.

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The size and shape of the active area of a given semiconductor device will depend upon the size, shape, and layout of the ohmic contacts. According to certain embodiments, the active area of the semiconductor device can be defined by regions having any of a variety of suitable shapes, including but not limited to, square regions, 5 rectangular regions, circular regions, and the like.

While examples of active areas have been described with reference to an exemplary transistor, other semiconductor devices also have active areas, and those of ordinary skill in the art would be capable of determining the active area of a given semiconductor device based on its geometry and operation. For example, in some cases, 10 the semiconductor device can be a diode. Referring to FIG. 2A, for example, a diode could be created by short circuiting electrode 220 (previously referred to as the source electrode in exemplary transistor embodiments) and electrode 230 (previously referred to as the drain electrode in exemplary transistor embodiments) such that, together, they form one electrode (*e.g.*, a cathode of a diode). Electrode 240 (previously referred to as 15 the gate electrode in exemplary transistor embodiments) could be used as a second electrode (*e.g.*, an anode). In such a case, each of source electrode 220 and drain electrode 230 would establish an ohmic contact (*i.e.*, contacts 308 and 309 would remain ohmic contacts. Contact 310 would remain a Schottky contact. The active area in such a device would correspond to the area over which electrons would be transported between 20 the Schottky contact and ohmic contacts during normal operation of the diode. For the example of FIG. 2A, the active area for a corresponding diode embodiment may be slightly less than the active area of the transistor embodiment. However, for short gate lengths, the difference in active area may be insignificant.

According to certain embodiments, the ohmic contacts in the semiconductor 25 device define a cumulative active area that is less than  $100\ \mu\text{m}^2$ , less than  $80\ \mu\text{m}^2$ , less than  $60\ \mu\text{m}^2$ , less than  $40\ \mu\text{m}^2$ , or less than  $20\ \mu\text{m}^2$ . In certain embodiments, the ohmic contacts define an active area that is greater than  $10\ \mu\text{m}^2$ , greater than  $20\ \mu\text{m}^2$ , greater than  $40\ \mu\text{m}^2$ , greater than  $60\ \mu\text{m}^2$ , or greater than  $80\ \mu\text{m}^2$ . Combinations of these ranges are also possible (*e.g.*, greater than  $40\ \mu\text{m}^2$  and less than  $80\ \mu\text{m}^2$ , greater than  $10\ \mu\text{m}^2$  and 30 less than  $40\ \mu\text{m}^2$ ).

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In some embodiments, the semiconductor device includes at least one region having a continuous active area that is at least  $10\ \mu\text{m}^2$  (or at least  $20\ \mu\text{m}^2$ , at least  $40\ \mu\text{m}^2$ , at least  $60\ \mu\text{m}^2$ , at least  $80\ \mu\text{m}^2$ , or at least  $100\ \mu\text{m}^2$ ) in size.

According to some embodiments, an active-area ratio can be defined for a device.

5 For example, an active-area ratio can be defined as a ratio of the active area of a device to a peripheral length of a gate or anode for the device. The gate or anode peripheral length can be determined as described above. The active area can be the active area (*e.g.*, active area 306) of a single device having one gate or anode, or the sum of all active areas of constituent devices (*e.g.*, when there is more than one gate or anode present in a device). In some implementations, devices formed in accordance with the present embodiments can have an active-area ratio that is between  $10\ \mu\text{m}^2/\mu\text{m}$  and  $250\ \mu\text{m}^2/\mu\text{m}$ . The active-area ratio of a device can be less than  $20\ \mu\text{m}^2/\mu\text{m}$  according to some embodiments, less than  $50\ \mu\text{m}^2/\mu\text{m}$  according to some embodiments, less than  $100\ \mu\text{m}^2/\mu\text{m}$  according to some embodiments, and yet less than  $200\ \mu\text{m}^2/\mu\text{m}$  according to some embodiments.

In certain embodiments, the sum of the source electrode interfacial area, the drain electrode interfacial area, and the gate electrode interfacial area is substantially less than the active area defined by the source electrode, drain electrode, and the gate electrode. Without wishing to be bound by any particular theory, it is believed that employing electrodes and active areas that are sized in this way advantageously reduces capacitive coupling between the electrodes and the substrate. According to certain embodiments, the sum of the source electrode interfacial area, the drain electrode interfacial area, and the gate electrode interfacial area is less than 65% of the active area. For example, referring to FIG. 2D, source electrode 220 has interfacial area 308 with III-nitride material region 120 that is about 30% of active area 306. In addition, in FIG. 2D, drain electrode 230 has interfacial area 309 with III-nitride material region 120 that is about 30% of active area 306. In certain embodiments, in FIG. 2D, gate electrode 240 has interfacial area 310 with III-nitride material region 120 that is about 2.5% of active area 306. Thus, in FIG. 2D, the sum of the interfacial areas 310, 309, and 310 is about 60% of active area 306 (which is less than 65% of active area 306).

In certain embodiments, the sum of the source electrode interfacial area and the drain electrode interfacial area is less than 60% of the active area. For example, referring

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to FIG. 2D, in some embodiments, the sum of interfacial areas 308 and 309 is less than 58.5% of active area 306.

In certain embodiments, the gate electrode interfacial area is less than 3% of the active area. For example, in FIG. 2D, in some embodiments, the interfacial area 310 is  
5 less than 2.6% of active area 306.

In certain embodiments, the sum of the device ohmic interfacial area and the device gate interfacial areas is substantially less than the device cumulative active area. According to certain embodiments, the sum of the device ohmic interfacial area and the device gate interfacial areas is less than 65% of the device cumulative active area. For  
10 example, referring to FIG. 3B, the sum of interfacial areas 308A-308F is about 30% of the sum of active areas 306A-306F. In addition, in FIG. 3B, the sum of interfacial areas 309A-309F is about 30% of the sum of active areas 306A-306F. In certain  
embodiments, in FIG. 3C, gate electrodes 240A-240F define interfacial areas 310A-310F with III-nitride material region 120 that is about 5% of the sum of active areas 306A-  
15 306F (in FIG. 3B). Thus, the sum of the interfacial areas 308A-309F, 309A-309F, and 310A-310F is about 60% of active area 306A-306F (which is less than 65% of active area 306A-306F).

In certain embodiments, the device ohmic interfacial area is substantially less than the device cumulative active area. According to certain embodiments, the device  
20 ohmic interfacial area is less than 60% of the device cumulative active area. For example, referring to FIG. 3B, the sum of interfacial areas 308A-308F is about 30% of the sum of active areas 306A-306F. In addition, in FIG. 3B, the sum of interfacial areas 309A-309F is about 30% of the sum of active areas 306A-306F. Thus, the sum of the interfacial areas 308A-309F and 309A-309FF is about 58% of active area 306A-306F  
25 (which is less than 60% of active area 306A-306F).

In certain embodiments, the gate electrode cumulative interfacial area is less than 3% of the cumulative active area. For example, referring to FIG. 3C, in some  
embodiments, the sum of interfacial areas 310A-310F is less than 2.5% of active area 306A-306 (in FIG. 3B).

30 According to certain embodiments, the semiconductor structures described herein comprise a thick III-nitride material region located over the substrate. For example, referring to FIGS. 2A, semiconductor device 200A comprises III-nitride material region 120 that can be thick. As noted above, in certain embodiments the III-nitride material

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region located over the substrate has a thickness of at least 2.0 micrometers. For example, in some embodiments, the III-nitride material region located over the substrate has a thickness of 4.8 micrometers.

According to certain embodiments, the use of a relatively thick III-nitride material region reduces undesired leakage current and transport of electrons from a first electrode structure (e.g., a source electrode), through the electronically conductive substrate (e.g., a silicon-containing substrate), and to a second electrode structure (e.g., a drain electrode). FIG. 2B is a cross-sectional schematic illustration of a semiconductor device having a semiconductor structure that includes an electronically conductive substrate, according to some embodiments. Referring to FIG. 2B, source electrode 220 is electrically connected to drain electrode 230 by current flow 304 through III-nitride material region 120 and substrate 110. In certain embodiments, the use of a thick III-nitride material region 120 can reduce the amount of leakage current between source electrode 220 and drain electrode 230 as less current is leaked along current flow 304.

In certain embodiments, the use of a relatively thick III-nitride material region reduces the capacitive coupling between electrode structures (e.g., metal electrodes) and the substrate. In some instances, the use of an electronically conductive substrate (e.g., a silicon-containing substrate) results in an increase in the capacitance between electrode structures and the substrate, effectively reducing the efficiency of devices or components formed using the semiconductor structure. Thickening the III-nitride material region, according to some embodiments, reduces the amount of energy transferred between the electrode structures and the substrate. Referring to FIG. 2B, use of a thick III-nitride material region 120 can reduce the amount of capacitive coupling between source electrode 220, drain electrode 230, and gate electrode 240 with substrate 110.

In certain cases, the source electrode, the drain electrode, and/or the gate electrode of transistors can capacitively couple to the substrate. Similarly, anode and cathode electrodes of diodes can capacitively couple to the substrate. Certain embodiments are directed to employing component configurations and/or methods of operation that reduce the degree to which capacitive coupling is observed. In some cases, the capacitive coupling results from the use of conductive substrates, as conductive structures (e.g., source, drain, and/or gate electrodes) capacitively couple to the substrate (e.g., silicon-containing substrate). In certain embodiments, the capacitive



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coupling can be reduced by the use of thick III-nitride materials, and/or the use of small ohmic contacts associated with the electrodes.

In certain embodiments, the capacitive coupling of the at least one type of ohmic contact (*e.g.*, drain, source, cathode) with the substrate is small. According to some implementations, an ohmic contact capacitance ratio can be defined for a device. The ohmic contact capacitance can depend on at least the ohmic contact area and on a thickness of the epitaxial structure between the ohmic contact(s) and the conductive substrate. Without being bound to any particular theory, a capacitance ratio of an ohmic contact can be expressed as follows

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$$C_{oc} = (\epsilon_0 \epsilon_r A_{oc}) / (tL) \quad (2)$$

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where  $\epsilon_0$  is the permittivity of free space,  $\epsilon_r$  is the effective relative permittivity of the epitaxial structure between the ohmic contact and the conductive substrate,  $A_{oc}$  is the area of the ohmic contact,  $t$  is the thickness of the epitaxial structure between the ohmic contact and the conductive substrate, and  $L$  is the gate or anode peripheral length. If there is more than one ohmic contact (*e.g.*, multiple drain contacts), then the areas of the ohmic contacts are summed to obtain  $A_{oc}$ . Similarly, the gate or anode peripheral length  $L$  is a sum of peripheral lengths of constituent gates or anodes in a device, as described above.

20

As an example for an epitaxial structure of the present embodiments that is approximately 1.6 microns thick with  $\epsilon_r$  of approximately 9.5, an ohmic contact capacitance ratio for at least one type of ohmic contact of a device can have a value between 0.1 pF/mm and 2.5 pF/mm. The ohmic contact capacitance ratio for at least one type of ohmic contact of a device can be less than 0.25 pF/mm in some cases, less than 0.5 pF/mm in some cases, less than 1 pF/mm in some cases, and yet less than 2 pF/mm in some cases.

25

As another example for an epitaxial structure of the present embodiments that is approximately 4.8 microns thick with  $\epsilon_r$  of approximately 9.5, an ohmic contact capacitance ratio for at least one type of ohmic contact of a device can have a value between 0.05 pF/mm and 0.8 pF/mm. For this example, the ohmic contact capacitance ratio for at least one type of ohmic contact of a device can be less than 0.1 pF/mm in

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some cases, less than 0.2 pF/mm in some cases, less than 0.4 pF/mm in some cases, and yet less than 0.6 pF/mm in some cases.

According to some embodiments, the semiconductor devices comprise at least one contact pad over the substrate, over the III-nitride material region, and over at least  
5 one ohmic contact. In some embodiments, the ohmic contacts are relatively small compared to the size of the contact pads. Large contact pads are, in accordance with certain embodiments, beneficial in the operation of the semiconductor devices that include semiconductor structures, as external connections can easily be made to the semiconductor structure through the large contact pads.

10 According to certain embodiments, the contact pads are located over the substrate, over the III-nitride material, and over an electrode (including the electrode's ohmic contact).

In some embodiments, the gate contact pad(s) is(are) located over the substrate, over the III-nitride material, and over the gate electrode(s). Referring back to FIG. 3D,  
15 for example, gate contact pad 244 is positioned over and in electrical contact with gate electrodes 240A, 240B, 240C, 240D, 240E, and 240F. Gate contact pad 244 is not visible in FIGS. 2A-2D, as the gate contact pad resides behind the plane of the cross-section.

According to certain embodiments, the drain contact pad(s) is(are) located over  
20 the substrate, over the III-nitride material, and over the drain electrode(s). Referring back to FIG. 3E, for example, drain contact pad 234 is positioned over and in electrical contact with drain electrodes 230A, 230B, 230C, 230D, 230E, and 230F. Drain contact pad 234 is also illustrated in the cross-sections shown in FIGS. 2A-2D. In FIGS. 2A-2D, drain contact pad 234 contacts drain electrode 230, and extends laterally beyond  
25 interfacial area 309 of ohmic contact 302B.

In some embodiments, the source contact pad(s) is(are) located over the substrate, over the III-nitride material, and over the source electrode(s). Referring back to FIG. 3F,  
for example, source contact pad 224A is positioned over and in electrical contact with source electrode 220A, source contact pad 224B is positioned over and in electrical  
30 contact with source electrode 220B, source contact pad 224C is positioned over and in electrical contact with source electrode 220C, and source contact pad 224D is positioned over an in electrical contact with source electrode 220D. Source contact pad 224A is also illustrated in the cross-sections shown in FIGS. 2A-2D. In FIGS. 2A-2D, source

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contact pad 224A contacts source electrode 220A and extends laterally beyond interfacial area 308 of ohmic contact 302A.

FIGS. 3G and 3H include top, perspective views of the device once the source, gate, and drain contact pads have been added to the device.

5 To reduce deleterious effects of contact pads above a conductive substrate, areas of the contact pads can be reduced. In this regard, contact-pad area ratios  $Ar_{cp}$  referenced to peripheral lengths can be defined for devices of the present embodiments and represented, for example, as follows

$$10 \quad Ar_{cp} = A_{cp}/L \quad (3)$$

where  $A_{cp}$  represents the area of all contact pads of a same type (*e.g.*, all drain contact pads, all anode contact pads) for a device, and  $L$  is the gate peripheral length or anode peripheral length for a device as described above.

15 In some implementations, devices formed in accordance with the present embodiments can have a contact-pad area ratio for gate or anode contact pads that is between  $15 \mu\text{m}^2/\mu\text{m}$  and  $20 \mu\text{m}^2/\mu\text{m}$ . In some cases, the contact-pad area ratio for gate or anode contact pads of a device can be less than  $17 \mu\text{m}^2/\mu\text{m}$  according to some embodiments, less than  $18 \mu\text{m}^2/\mu\text{m}$  according to some embodiments, less than  $19$   
20  $\mu\text{m}^2/\mu\text{m}$  according to some embodiments, and yet less than  $20 \mu\text{m}^2/\mu\text{m}$  according to some embodiments.

In some implementations, devices formed in accordance with the present embodiments can have a contact-pad area ratio for drain, source, or cathode contact pads that is between  $30 \mu\text{m}^2/\mu\text{m}$  and  $50 \mu\text{m}^2/\mu\text{m}$ . In some cases, the contact-pad area ratio for  
25 gate or anode contact pads of a device can be less than  $35 \mu\text{m}^2/\mu\text{m}$  according to some embodiments, less than  $40 \mu\text{m}^2/\mu\text{m}$  according to some embodiments, less than  $45 \mu\text{m}^2/\mu\text{m}$  according to some embodiments, and yet less than  $50 \mu\text{m}^2/\mu\text{m}$  according to some embodiments.

In embodiments, any of the aforementioned contact pads can capacitively couple  
30 to a conductive substrate. Accordingly, capacitance of a contact pad can be reduced to ameliorate deleterious effects of such capacitive coupling. A contact-pad capacitance ratio referenced to peripheral length can be defined for contact pads of devices of the

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present embodiments. Without being bound to any particular theory, a contact-pad capacitance ratio can be expressed as follows

$$C_{cp} = \left( \frac{1}{C_1} + \frac{1}{C_2} \right)^{-1} \quad (4)$$

where  $C_1$  represents a capacitance component attributed to epitaxial material in a region between the conductive substrate 110 and dielectric region 250, and  $C_2$  represents a capacitance component attributed to the dielectric region 250, for example and referring to FIG. 2A.  $C_1$  and  $C_2$  can be expressed as follows

$$C_1 = (\epsilon_0 \epsilon_{r1} A_{cp}) / (t_1 L) \quad (5)$$

$$C_2 = (\epsilon_0 \epsilon_{r2} A_{cp}) / (t_2 L)$$

where  $\epsilon_0$  is the permittivity of free space,  $\epsilon_{r1}$  is the effective relative permittivity of the epitaxial structure between the conductive substrate 110 and dielectric region 250,  $\epsilon_{r2}$  is the relative permittivity of the dielectric region 250,  $A_{cp}$  is the area of the contact pad as described above,  $t_1$  is the thickness of the epitaxial structure between the conductive substrate 110 and dielectric region 250,  $t_2$  is the thickness of the dielectric region 250, and  $L$  is the gate peripheral length or anode peripheral length as described above. The area of the contact pad can be the area of a source contact pad, a drain contact pad, a gate contact pad, an anode contact pad, or a cathode contact pad. If there is a plurality of a same type of contact pads in a device (*e.g.*, plural drain contact pads for a transistor), then the area of the contact pad  $A_{cp}$  would be the sum of all areas of the contact pads of the same type when determining the capacitance ratio. If there is a plurality of gates or anodes for a device, then the peripheral length  $L$  would be the sum of all gate peripheral lengths or anode peripheral lengths.

As examples for an epitaxial structure of the present embodiments that is approximately 4.8 microns thick with  $\epsilon_{r1}$  of approximately 9.5 and that is covered with at least one layer of dielectric material (*e.g.*, approximately 4 microns of benzocyclobutane (BCB) with  $\epsilon_{r2}$  of approximately 2.65), a contact-pad capacitance ratio for a gate or anode of a device can have a value between 0.05 pF/mm and 1.0 pF/mm. The contact-pad capacitance ratio for a gate or anode of a device can be less than 0.1 pF/mm in some

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cases, less than 0.2 pF/mm in some cases, less than 0.4 pF/mm in some cases, less than 0.6 pF/mm in some cases, less than 0.8 pF/mm in some cases, and yet less than 1 pF/mm in some cases. In some implementations, the dielectric region can include additional layers of dielectric material (*e.g.*, a layer of silicon nitride between 0.1 micron and 1  
5 micron thick with  $\epsilon_{r2}$  of approximately 6.44).

As additional examples for an epitaxial structure of the present embodiments that is approximately 4.8 microns thick with  $\epsilon_{r1}$  of approximately 9.5 and that is covered with at least one layer of dielectric material (*e.g.*, approximately 4 microns of benzocyclobutane (BCB) with  $\epsilon_{r2}$  of approximately 2.65), a contact-pad capacitance ratio  
10 for a drain, source, or cathode of a device can have a value between 0.1 pF/mm and 1.5 pF/mm. The contact-pad capacitance ratio for a drain, source, or cathode of a device can be less than 0.2 pF/mm in some cases, less than 0.4 pF/mm in some cases, less than 0.6 pF/mm in some cases, less than 0.8 pF/mm in some cases, less than 1.0 pF/mm in some cases, and yet less than 1.2 pF/mm in some cases. In some implementations, the  
15 dielectric region can include additional layers of dielectric material (*e.g.*, a layer of silicon nitride between 0.1 micron and 1 micron thick with  $\epsilon_{r2}$  of approximately 6.44).

According to some embodiments, an active-area capacitance ratio  $C_a$  can be defined for a device formed over a conductive substrate as follows

$$20 \quad C_a = (\epsilon_0 \epsilon_r A_a) / (tL) \quad (6)$$

where  $\epsilon_0$  is the permittivity of free space,  $\epsilon_r$  is the effective relative permittivity of the epitaxial structure between the conductive substrate 110 and the devices active area 306,  $A_a$  is the active area of the device as described above (*e.g.*, a sum of active areas for a  
25 transistor that comprises multiple source, gate, and drain electrode groups as in FIG. 3C),  $t$  is the thickness of the epitaxial structure between the conductive substrate 110 and active area 306, and  $L$  is the gate peripheral length or anode peripheral length as described above.

In some implementations, an active-area capacitance ratio  $C_a$  for a device is  
30 between 0.05 pF/mm and 0.5 pF/mm. The active-area capacitance ratio  $C_a$  for a device can be no greater than 0.2 pF/mm in some embodiments, no greater than 0.3 pF/mm in some embodiments, and yet no greater than 0.4 pF/mm in some embodiments.

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In certain embodiments, the at least one contact pad defines a contact pad area. The contact pad area of a particular contact pad refers to the area over which that contact pad forms an interface with the underlying material. For example, referring to FIG. 3D, gate contact pad 244 defines contact pad area 242, which is the entire black area of contact pad 244. In FIG. 3E, drain contact pad 234 defines contact pad area 232, which is the entire black area of contact pad 234. Referring to FIG. 3F, source contact pads 224A, 224B, 224C, and 224D define contact pad areas 222A, 222B, 222C, and 222D, respectively (which, each, correspond to the entire black areas of contact pads 224A-224D).

10 In some embodiments, for at least one contact pad, the ratio of (1) the ohmic contact interfacial area of the electrode connected to that contact pad to (2) the contact pad area of that contact pad is less than 12%. In some cases, the ratio of (1) the ohmic contact interfacial area of the electrode connected to that contact pad to (2) the contact pad area of that contact pad is less than 10%. In some cases, the ratio of (1) the ohmic contact interfacial area of the electrode connected to that contact pad to (2) the contact pad area of that contact pad is less than 15%. In some cases, the ratio of (1) the ohmic contact interfacial area of the electrode connected to that contact pad to (2) the contact pad area of that contact pad is less than 20%. In some cases, the ratio of (1) the ohmic contact interfacial area of the electrode connected to that contact pad to (2) the contact pad area of that contact pad is less than 30%.

In certain embodiments, for at least one gate or anode contact pad, the ratio of (1) the Schottky contact interfacial area of the gate or anode electrode(s) connected to the gate or anode contact pad to (2) the contact pad area of the gate or anode contact pad is less than 2.5%. For example, in FIG. 3D, gate contact pad 244 is connected to each of gate electrodes 240A, 240B, 240C, 240D, 240E, and 240F. Thus, to calculate the ratio of the Schottky contact interfacial area to the contact pad area for contact pad 244, one would determine the ratio of:

(1) the sum of the interfacial areas of the gate (or anode) electrodes 240A-240F (which would be determined by summing the interfacial areas of each of the six gate or anode electrodes) to  
30 (2) the contact pad area 242.

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According to certain embodiments, this ratio is less than 1.5%. In some cases, this ratio is less than 30%. In some cases, this ratio is less than 20%. In some cases, this ratio is less than 15%.

In accordance with certain embodiments, for at least one drain or cathode contact pad, the ratio of (1) the ohmic contact interfacial area of the drain or cathode electrode(s) connected to the drain or cathode contact pad to (2) the contact pad area of the drain or cathode contact pad is less than 12%. For example, referring to FIG. 3E, drain contact pad 234 is connected to each of drain electrodes 230A, 230B, 230C, 230D, 230E, and 230F. Thus, to calculate the ratio of the ohmic contact interfacial area to the contact pad area for contact pad 234, one would determine the ratio of:

(1) the sum of the interfacial areas of the drain (or cathode) electrodes 230A-230F (which would be determined by summing the interfacial areas of each of the six drain electrodes) to

(2) the drain or cathode contact pad area 232.

According to certain embodiments, this ratio is less than 10%. In some cases, this ratio is less than 30%. In some cases, this ratio is less than 20%. In some cases, this ratio is less than 15%.

In some embodiments, for at least one source contact pad, the ratio of (1) the ohmic contact interfacial area of the source electrode(s) connected to the source contact pad to (2) the contact pad area of the source contact pad is less than 15%. For example, referring to FIG. 3F, source contact pad 224A is connected to a single source electrode 220A. Thus, to calculate the ratio of the ohmic contact interfacial area to the contact pad area for contact pad 224A, one would determine the ratio of:

(1) the interfacial area of the source electrodes 220A connected to contact pad 224A to

(2) the source contact pad area 222A.

According to certain embodiments, this ratio is less than 28%. In some cases, this ratio is less than 30%. In some cases, this ratio is less than 20%. In some cases, this ratio is less than 15%.

As another example, in FIG. 3F, source contact pad 224B is connected to two source electrodes 220B and 220C. Thus, to calculate the ratio of the ohmic contact interfacial area to the contact pad area for contact pad 224B, one would determine the ratio of:

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- (1) the interfacial areas of the two source electrodes 220B and 220C connected to contact pad 224B to
- (2) the source contact pad area 222B.

According to certain embodiments, this ratio is less than 13.6%. In some cases, this ratio is less than 30%. In some cases, this ratio is less than 20%. In some cases, this ratio is less than 15%.

According to certain embodiments, the device ohmic interfacial area is relatively small compared to the device ohmic contact pad area. As noted above, the device ohmic interfacial area refers to the sum of all of the interfacial areas of the ohmic contacts of that device. In a similar manner, the “device ohmic contact pad area” refers to the sum of all of the areas of contact pads connected to electrodes that establish ohmic contacts of that device. For example, referring back to FIG. 3G. The device ohmic interfacial area would be calculated by summing twelve (12) interfacial areas (i.e., the six interfacial areas defined by the six source electrodes 220 and the six interfacial areas defined by the six drain electrodes 230). In FIG. 3G, the device ohmic contact pad area would be calculated by summing five (5) contact pad areas (i.e., drain contact pad area 232, source contact pad area 222A, source contact pad area 222B, source contact pad area 222C, and source contact pad area 222D).

In certain embodiments, the ratio of the device ohmic interfacial area to the device ohmic contact pad area is less than 13.6%. In some cases, the ratio of the device ohmic interfacial area to the device ohmic contact pad area is less than 15%. In some cases, the ratio of the device ohmic interfacial area to the device ohmic contact pad area is less than 20%. In some cases, the ratio of the device ohmic interfacial area to the device ohmic contact pad area is less than 30%.

According to certain embodiments, the semiconductor devices and semiconductor structures described herein comprise a dielectric region (e.g., a single dielectric layer, a combination of dielectric layers). In certain embodiments, the dielectric region is located over the substrate and over the III-nitride material region. For instance, as shown in FIG. 2B, semiconductor device 200A comprises dielectric region 250 located over substrate 110 and over III-nitride material region 120.

According to certain embodiments, the dielectric region can be made of any of a variety of suitable dielectric materials. Non-limiting examples of suitable materials from which the dielectric region can be made include silicon dioxide (SiO<sub>2</sub>), tetraethyl



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orthosilicate (TEOS), high-k dielectrics or transition metal (TM) oxides, polyimide, polybenzoxazole (PBO), and/or benzocyclobutane (BCB).

In some embodiments, the dielectric region of the semiconductor device is thick. For example, referring to FIGS. 2A-2D, in some embodiments, dielectric region 250 can be relatively thick (with the thickness illustrated in FIGS. 2A-2D as dimension 252). In certain embodiments, the dielectric region has a thickness of at least 1 micrometer, at least 2 micrometers, at least 3 micrometers, at least 5 micrometers, or at least 10 micrometers. In some embodiments, the dielectric region thickness is less than 10 micrometers, less than 5 micrometers, less than 3 micrometers, or less than 2 micrometers. Combinations of these ranges are also possible (e.g., greater than 3 micrometers and less than 10 micrometers, greater than 1 micrometer and less than 5 micrometers).

In certain embodiments, at least one of the contact pads is located over the dielectric region. Contact pad(s) located over the dielectric region can, for example, sit on top of the dielectric region. Referring to FIG. 2A, for example, semiconductor device 200A comprises contact pad 244 located over substrate 110, over III-nitride material region 120, and over dielectric region 250. In other cases, a contact pad(s) positioned over the dielectric region can be embedded within the dielectric layer. According to certain embodiments, a large contact pad located over a thick dielectric region can lower the amount of RF current displaced through the silicon-containing substrate.

In certain embodiments, the dielectric region material has any of variety of suitable dielectric constants. In certain embodiments, the dielectric material has a dielectric constant of less than 4, less than 3, or less than 2. In certain embodiments, the dielectric material has a dielectric constant of greater than 1, greater than 2, or greater than 3. Combinations of these ranges are also possible (e.g., greater than 1 and less than 4, greater than 2 and less than 3). In some embodiments, the dielectric material has a dielectric constant of 2.65.

According to certain embodiments, the semiconductor devices described herein comprise an electronically conductive material located within and/or over the III-nitride material region. The electrically conductive material (e.g., a conductive via) can be arranged such that it establishes an electrical connection between top side electronic structures (e.g., one or more contact pads) and the electronically conductive substrate by passing vertically through the III-nitride material region. In some implementations, the

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electrically conductive substrate can be held at ground potential (or some other reference potential) and provide a backside ground at the location of integrated circuit components. According to certain embodiments, the use of electronically conductive materials located within and/or over the III-nitride material region is advantageous as grounding can be  
5 achieved in such devices without the need for an external wire(s) and/or patterning other interconnects on the substrate to provide ground. The backside ground can also provide, in accordance with certain embodiments, improved gain.

FIG. 4 is a cross-sectional schematic illustration of a semiconductor device comprising an electronically conductive material coupled to a contact pad and a  
10 substrate, according to certain embodiments. As shown in FIG. 4, semiconductor structure 600A comprises substrate 110 and III-nitride material region 120 over substrate 110. Also shown in FIG. 4 is electronically conductive material 610, which has been deposited within cavity 612 formed in the device.

In some embodiments, the electronically conductive material is electrically  
15 coupled to the electronically conductive portion of the substrate through the thickness of the III-nitride material region. For example, referring to FIG. 4, electronically conductive material 610 is electrically coupled to electronically conductive portion of substrate 110 through the thickness of the III-nitride material region 120 by way of cavity 612. Cavity 612 can function, for example, as a front-side (or top-side) via. In  
20 certain embodiments, cavity 612 is formed (e.g., etched) into the layers of the semiconductor structure (such as III-nitride material region 120), and electronically conductive material 610 is deposited or otherwise formed in cavity 612 such that it is coupled to the electronically conductive portion of the substrate through the thickness of the III-nitride material region. In some embodiments, the perimeter (e.g., sidewalls and  
25 base) of the cavity or via is lined with a conductive metal, and in other embodiments a metal or conductive plug is formed by filling the cavity or via. According to certain embodiments, the semiconductor structure can be grounded to the electronically conductive substrate through electronically conductive material 610 without using an external connection from the drain electrode to an external ground.

30 In certain embodiments, the electronically conductive material can make an electrical connection from the source electrode to an electronically conductive portion of the substrate. For example, in FIG. 4, electronically conductive material makes an

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electrical connection from source electrode 220 to substrate 110 by connecting source contact pad 224 (which is electrically coupled to source electrode 220) to substrate 110.

As described elsewhere herein, the use of an electronically conductive substrate can lower thermal runaway within the semiconductor structure. In addition, the use of  
5 thick III-nitride materials, small ohmic contacts, and/or thick dielectric regions can reduce capacitive coupling. Such improvements can, in accordance with certain embodiments, result in performance enhancements with high operational frequencies and/or high input frequencies are employed. In certain embodiments, operating  
10 semiconductor structures with electronically conductive structures at high operational frequencies and high input frequencies results in generated RF signals with a reduction in the dissipated current throughout the electronically conductive substrate. As a result, and according to certain embodiments, the devices can be operated at high frequencies at higher temperatures with less device degradation, which will be described herein in further detail.

15 In some embodiments, the semiconductor structures described herein are capable of operation at a high operational frequency. As used herein, operational frequency can be understood as the frequency of a signal that is input to a device having a semiconductor structure of the present embodiments, and operated on by the device (*e.g.*, amplified, switched, modulated, *etc.*) to produce an output signal. In some  
20 embodiments, the semiconductor structures described herein are capable of receiving a high input frequency without significant attenuation (*e.g.*, less than 6 dB of power attenuation between input and output of a device formed using the semiconductor structures described herein). As used herein, input frequency can be understood as the frequency of the applied signal to the gate of a transistor or anode of a diode. High  
25 operational frequencies can be in the radio frequency (RF) range and have a value between 50 MHz and 50 GHz.

In some embodiments, certain of the devices described herein are configured to maintain high operational frequencies over a relatively large number of operation cycles. For example, in some embodiments, devices and components formed using the  
30 semiconductor structure can maintain an operational frequency of greater than 50 MHz (or greater than 60 MHz, greater than 70 MHz, greater than 80 MHz, greater than 90 MHz, or greater than 100 MHz, and/or, in some embodiments, up to 50GHz) for at least

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10 seconds, at least 100 seconds, at least 10 minutes, at least 100 minutes, at least 10 hours, at least 100 hours, or more (and/or, in some embodiments, up to  $10^7$  hours).

According to certain embodiments, devices and components formed using the semiconductor structures have an operational frequency of greater than 50 MHz. In  
5 certain embodiments, the operational frequency of the devices or components is greater than 60 MHz, greater than 70 MHz, greater than 80 MHz, greater than 90 MHz, or greater than 100 MHz. According to certain embodiments, the operational frequency is less than 110 MHz, less than 100 MHz, less than 90 MHz, less than 80 MHz, less than  
10 70 MHz, or less than 60 MHz. Combinations of these ranges are also possible (e.g., greater than 50 MHz and less than 80 MHz, greater than 70 MHz and less than 100 MHz).

In certain embodiments, devices or components comprising the semiconductor structures have an input frequency of greater than 800 MHz. The input frequency can be less than 20 GHz in some cases, can be less than 10 GHz in some cases, less than 7 GHz  
15 in some cases, less than 4 GHz in some cases, less than 2 GHz in some cases, and yet less than 1 GHz in some cases. Combinations of these ranges are also possible (e.g., greater than 800 MHz and less than 1 GHz, greater than 800 MHz and less than 4 GHz).

According to certain embodiments, devices formed using certain semiconductor structures described herein have high operating efficiency at elevated temperatures (e.g.,  
20 substrate lattice temperatures). For example, transistors having semiconductor structures described herein can operate with high drain efficiencies (DE) or power-added efficiencies (PAE). Drain efficiency as used herein is a ratio of RF power output from a device to the DC power input to the device. Power-added efficiency as used herein is a ratio of a net RF power output from a device (RF power out minus RF power input) to  
25 the DC power input to the device. Without wishing to be bound by any theory, it is believed that relatively high efficiencies can be achieved, at least in part, due to the use of electronically conductive substrates, thick-III nitride layers, small ohmic contact areas, and/or a backside ground plane, which can result in reduced capacitive coupling and/or leakage current to the substrate.

30 In certain embodiments, a device comprising a semiconductor structure of the present embodiments is configured such that when the device's conductive substrate is at 25 °C the device exhibits a power-added efficiency between 50% and 60% and that a PAE of greater than 50% can be maintained for an increases in substrate temperature to

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as high as 100 °C. According to some embodiments, a device is configured such that when the device's conductive substrate is at 25 °C the device exhibits a PAE between 50% and 60% and that a PAE of greater than 50% can be maintained for an increase in substrate temperature to as high as 135 °C. According to some embodiments, a device is  
5 configured such that when the device's conductive substrate is at 25 °C the device exhibits a PAE between 50% and 60% and that a PAE of greater than 45% can be maintained for an increase in substrate temperature to as high as 200 °C. In some embodiments, a device is configured such that when the device's conductive substrate is at 25 °C the device exhibits a PAE of up to 55%, up to 60%, up to 65%, up to 70%, up to  
10 75%, up to 80%, up to 85%, or more.

According to some embodiments, a device comprising a semiconductor structure of the present embodiments can exhibit a drop in PAE of no greater than 5% when the temperature of the device's conductive substrate is increased in temperature from 25°C to 100 °C. According to some embodiments, a device comprising a semiconductor  
15 structure of the present embodiments can exhibit a drop in PAE of no greater than 5% when the temperature of the device's conductive substrate is increased in temperature from 25°C to 130 °C. According to some embodiments, a device comprising a semiconductor structure of the present embodiments can exhibit a drop in PAE of no greater than 10% when the temperature of the device's conductive substrate is increased  
20 in temperature from 25°C to 130 °C. According to some embodiments, a device comprising a semiconductor structure of the present embodiments can exhibit a drop in PAE of no greater than 10% when the temperature of the device's conductive substrate is increased in temperature from 25°C to 200 °C.

In some embodiments, a device comprising a semiconductor structure of the  
25 present embodiments can exhibit a drop in PAE of up to 1%, up to 2%, up to 3%, up to 4%, or more when the substrate is increased in temperature from 25°C to 105 °C. According to certain embodiments, a device comprising a semiconductor structure of the present embodiments can exhibit a drop in PAE of as little as 4%, as little as 3%, as little as 2%, as little as 1%, or less when the substrate is increased in temperature from 25°C to  
30 105 °C. Combinations of these ranges are also possible (e.g., as little as 2% and up to 4%, as little as 3% and up to 5%). According to certain embodiments, a device comprising a semiconductor structure of the present embodiments can exhibit a drop in PAE of up to 1%, up to 3%, up to 5%, up to 7%, up to 9%, or more when the substrate is

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increased in temperature from 25°C to 125 °C. According to certain embodiments, a device comprising a semiconductor structure of the present embodiments can exhibit a drop in PAE of as little as 9%, as little as 7%, as little as 5%, as little as 3%, or less when the substrate is increased in temperature from 25°C to 125 °C. Combinations of these  
5 ranges are also possible (e.g., as little as 3% and up to 10%, as little as 5% and up to 7%).

According to certain embodiments, the semiconductor structures described herein can be used in RF signal handling (e.g., wireless communications), radar applications, RF switching, and power applications. In certain embodiments, the semiconductor  
10 structures used for such applications comprise GaN on a conductive silicon substrate.

Various of the devices described herein may be made using conventional semiconductor processing techniques. Such processing techniques can involve, for example, growing layers on the substrate in a process chamber under vacuum conditions.

Some methods may include cleaning the substrate surface prior to growing  
15 overlying layers and, typically, before introduction into the process chamber. The substrate surface may be cleaned to remove residual dopant species that may diffuse into the substrate during processing. For example, the substrate may be cleaned by wet chemical cleaning agents such as buffered oxide etch (BOE), hydro-fluoric acid (HF), RCA clean (which is a commercial, proprietary silicon surface cleaning agent), etc.  
20 Substrates may also be cleaned by a combination of such agents. The surface of the substrate may be cleaned with organic solvents such as acetone, methanol, trichloroethylene, isopropyl alcohol, etc., for example, to rid a surface of organic contamination.

In some embodiments, methods may include controlling the residual (e.g.,  
25 residual reaction by-products) amounts of dopant in the process chamber. For example, the amount of residual dopant may be reduced by purging the chamber with a gas (e.g., NH<sub>3</sub>) while heating to an elevated temperature, prior to introducing the substrate into the chamber. Purging has been found to minimize accumulation of reaction-by-products on reaction chamber walls and components.

In certain embodiments in which a diffusion barrier layer is present, the diffusion  
30 barrier layer may be formed in-situ with overlying layers (e.g., the III-nitride material region) of the structure. That is, the diffusion barrier layer may be formed during the same deposition step as the III-nitride material region (e.g., including the optional III-

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nitride material nucleation layer, the optional III-nitride material transition layer, the optional III-nitride material buffer layer, and/or the III-nitride material device region).

The III-nitride material region may be formed using known growth techniques.

In some embodiments, the optional III-nitride nucleation layer, the optional III-nitride transition layer, the optional III-nitride buffer layer, and/or the III-nitride device region are grown using a metalorganic chemical vapor deposition (MOCVD) process. It should be understood that other suitable techniques known in the art may also be utilized to deposit these layers including molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE), and the like. In certain embodiments, more than one growth technique may be used to grow different III-nitride material layers. For example, in one set of embodiments, MBE could be used to grow the nucleation layer, and the remaining III-nitride material layers may be formed using MOCVD. Other combinations are also possible.

Generally, the MOCVD process involves introducing different reactive source gases (e.g., Al source gases, Ga source gases, N source gases) into the process chamber and providing conditions which promote a reaction between the gases to form a layer. The reaction proceeds until a layer of desired thickness is achieved. The composition of the layer may be controlled, as described further below, by several factors including gas composition, gas concentration, and the reaction conditions (e.g., temperature and pressure).

Examples of suitable source gases for MOCVD growth of the optional III-nitride material nucleation layer, the optional III-nitride material transition layer, the optional III-nitride material buffer layer, and/or the III-nitride material device region include trimethylaluminum (TMA) or triethylaluminum (TEA) as sources of aluminum; trimethylindium (TMI) or triethylindium (TEI) as sources of indium; trimethylgallium (TMG) or trimethylgallium (TEG) as sources of gallium; and ammonia (NH<sub>3</sub>) as a source of nitrogen. The particular source gas used depends upon the desired composition of the layers. For example, an aluminum source (e.g., TMA or TEA), a gallium source (TMG or TEG), and a nitrogen source are used to deposit films having an Al<sub>x</sub>Ga<sub>1-x</sub>N composition.

The flow rates of the source gases, the ratios of the source gases, and the absolute concentrations of the source gases may be controlled to provide layers (e.g., transition layers and gallium nitride material regions) having a desired composition. For the

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growth of  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layers, typical TMA flow rates are between about 5  $\mu\text{mol}/\text{min}$  and about 50  $\mu\text{mol}/\text{min}$  with a flow rate of about 20  $\mu\text{mol}/\text{min}$  being preferred in some cases; typical TMG flow rates are between about 5  $\mu\text{mol}/\text{min}$  and 250  $\mu\text{mol}/\text{min}$ , with a flow rate of 115  $\mu\text{mol}/\text{min}$  being preferred in some cases; and the flow rate of ammonia is typically between about 3 slpm to about 10 slpm. According to certain embodiments, relatively high flow rates (and also higher gas velocities) can be used, which have been found to be particularly effective in minimizing accumulation of dopants.

According to certain embodiments, the reaction temperatures are generally between about 900 °C. and about 1200 °C. In some embodiments, the process pressures are between about 1 Torr and about 760 Torr. It is to be understood that the process conditions, and in particular the flow rate, are highly dependent on the process system configuration. Typically, smaller throughput systems require less flow than larger throughput systems.

When forming a compositionally-graded layer (e.g., a compositionally graded transition layer, which might be formed, for example, within transition layer 170), process parameters may be suitably adjusted to control the compositional grading. The composition may be graded by changing the process conditions to favor the growth of particular compositions. For example, to increase incorporation of gallium in the transition layer thereby increasing the gallium concentration, the flow rate and/or the concentration of the gallium source (e.g., TMG or TEG) may be increased. Similarly, to increase incorporation of aluminum into the transition layer thereby increasing the aluminum concentration, the flow rate and/or the concentration of the aluminum source (e.g., TMA or TEA) may be increased. The manner in which the flow rate and/or the concentration of the source is increased (or decreased) can control the manner in which the composition is graded. In other embodiments, the temperature and/or pressure is adjusted to favor the growth of a particular compound. Growth temperatures and pressures favoring the incorporation of gallium into the transition layer differ from the growth temperatures and pressures favoring the incorporation of aluminum into the transition layer. Thus, the composition may be graded by suitably adjusting temperature and pressure.

When depositing a layer having a constant composition (e.g., a transition layer, a gallium nitride material layer, etc.), however, the process parameters can be maintained constant so as to provide a layer having a constant composition. When III-nitride



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material regions (e.g., gallium nitride material regions) include more than one material layer (e.g., more than one gallium nitride material layer) having different respective compositions, the process parameters may be changed at the appropriate time to change the composition of the layer being formed.

5           It should be understood that all of the layers/regions on the substrate (e.g., the optional III-nitride material nucleation layer, the optional III-nitride material transition layer, the optional III-nitride material buffer layer, and/or the III-nitride material device region) may be grown in the same process, or respective layers/regions may be grown separately.

10           The processes described herein have been described as involving growing the layers/regions (e.g., the optional III-nitride material nucleation layer, the optional III-nitride material transition layer, the optional III-nitride material buffer layer, and/or the III-nitride material device region) in vertical growth processes. That is, these layers/regions have been described as being grown in a vertical direction with respect to  
15           underlying layers/regions (including the substrate). However, in other embodiments of the invention (not shown), it is possible to grow at least a portion of the layer(s) of the III-nitride material region (e.g., gallium nitride material layer(s)) using a lateral epitaxial overgrowth (LEO) technique, for example, as described in U.S. Pat. No. 6,051,849; or a pendeoepitaxial technique that involves growing sidewalls of gallium nitride material  
20           posts into trenches until growth from adjacent sidewalls coalesces to form a gallium nitride material region, for example, as described in U.S. Pat. No. 6,265,289. U.S. Patent. No. 7,071,498 entitled “Gallium Nitride Material Devices Including an Electrode-Defining Layer and Methods of Forming the Same,” filed Dec. 17, 2003, and issued July 4, 2006, which is incorporated herein by reference above, further describes  
25           techniques used to grow other layers and features shown in the various embodiments described herein.

It should also be understood that other processes may be used to form structures and devices of the present invention as known to those of ordinary skill in the art.

30           Certain of the layers and/or regions are referred to as being “formed on,” “formed over,” “formed directly on,” “formed directly over,” and/or “covering” another layer or region (e.g., the substrate). It should be understood that such phrases include situations in which a top surface of an underlying region or layer (e.g., substrate) is converted to the layer or region that is being formed. Such phrases also refer to situations in which

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new layers are formed by depositing the new, separate layer on the top surface of the underlying layer and/or region (e.g., a substrate).

As noted above, the term “region” may refer to one layer or may refer to multiple layers. It should also be understood that, wherever a single layer is described, the single layer may be replaced, according to certain embodiments, with multiple layers. For example, in certain instances, single layers described herein can be replaced with multiple layers that perform a similar function.

The following examples are intended to illustrate certain embodiments of the present invention, but do not exemplify the full scope of the invention.

10

### EXAMPLE 1

Example results from fabricated devices and simulations are described in this section. FIG. 5A shows measured power-added efficiency (PAE) at 2.5 GHz for two GaN-on-silicon high-electron mobility transistors (HEMTs) versus measured temperature of the silicon substrate. One GaN HEMT transistor was manufactured on a 625  $\mu\text{m}$  thick highly conductive (0.02  $\Omega\text{-cm}$  i.e. conductive) silicon substrate and the other was manufactured on a 625  $\mu\text{m}$  thick highly resistive (10,000  $\Omega\text{-cm}$  i.e. float-zone) silicon substrate. The transistor using a highly conductive substrate (upper trace) shows improved power added efficiency at all temperatures and particularly at elevated substrate temperatures compared to the HEMT formed on the highly resistive substrate.

FIG. 5B shows measured output power density at 2.5 GHz as a function of substrate temperature for the same two GaN-on-silicon HEMT transistors that were used to obtain the results in FIG. 5A. The transistor formed on a highly conductive substrate (upper trace) shows improved output power density at all temperatures and particularly at elevated substrate temperatures compared to the transistor formed on the highly resistive substrate.

FIG. 6 plots calculated power dissipation in a 50 $\mu\text{m}$  thick silicon substrate as a function of the substrate’s bulk resistivity for five different applied RF signals. The RF signals (2.5 GHz sinusoidal), ranging from 10 volts peak-to-peak to 50 volts peak-to-peak are capacitively coupled (over a 1 mm  $\times$  1 mm area) to the silicon substrate through a 400-nm-thick silicon-nitride layer and 1.6- $\mu\text{m}$ -thick GaN dielectric layer on top of the silicon substrate. The bottom of the silicon substrate is at ground potential. To

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minimize power dissipation in the silicon substrate, either a highly conductive or highly resistive substrate can be used (corresponding to either side of the bell curves).

However, the change in bulk resistivity of highly resistive silicon substrates at elevated temperatures ( $\sim 200$  °C) tends towards the peak of the bell curves in FIG. 6, whereas the

5 change in bulk resistivity of highly conductive silicon substrates at elevated temperatures tends away from the peak of the bell curves. Therefore, highly conductive silicon substrates dissipate less power at elevated substrate temperatures compared to highly resistive ones and are preferred for GaN-on-silicon HEMTs, diodes, and other semiconductor devices operating at elevated temperatures.

10 Figure 7 plots simulated power dissipation in a silicon substrate for a 1mm gate peripheral length GaN-on-silicon HEMT transistor versus the silicon substrate temperature for five 2.5 GHz sinusoidal RF signals (ranging from 10 volts to 50 volts peak-to-peak) that are applied between the transistor's drain and source contacts. The simulation uses a silicon substrate thickness of 50  $\mu\text{m}$  (10,000  $\Omega\text{-cm}$  bulk resistivity),  
15 gate-to-gate pitch of 65  $\mu\text{m}$ , and total GaN layer thickness of 1.6  $\mu\text{m}$  for the transistor to calculate capacitive coupling to the substrate. Also plotted on the same graph are simulation results at 50 volts peak-to-peak for a same structure that instead has a highly conductive substrate (0.015  $\Omega\text{-cm}$  bulk resistivity).

As can be seen, for a 50 volt signal, the power dissipated in the highly resistive  
20 silicon at 180 °C substrate temperature is about 1.0 Watt/mm and essentially zero for the highly conductive silicon substrate. In embodiments, a GaN-on-silicon HEMT transistor can output about 7.0 Watts/mm (gate peripheral length) RF output power at 2.5GHz with a drain-to-source bias  $V_{\text{DS}}$  of 50 volts. Accordingly, 1.0 Watt/mm dissipation into the substrate will dramatically degrade both output power capability of the transistor (*e.g.*,  
25 reduced to about 6.0 Watts/mm) as well as degrade device efficiency and increase the transistor junction temperature due to substrate heating.

FIG. 8 plots calculated active-area-to-substrate capacitance of a 1.0 mm gate peripheral length GaN-on-silicon HEMT transistor formed on a highly conductive silicon substrate as a function of GaN epitaxy thickness in the semiconductor structure. For this  
30 simulation the thickness of the epitaxial region is measured from the location of the 2-dimensional electron gas (2DEG) down to the surface of the conductive substrate. The simulation results represent a lower bound to the device's output capacitance that can be

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achieved for a GaN on highly conductive silicon substrate HEMT transistor, since it does not include capacitances associated with interconnects and contact pads, for example. The plotted capacitance values can influence maximum transistor bandwidth. The calculation assumes reduced-size ohmic contacts (*e.g.*, 4.5 $\mu\text{m}$  wide) and a gate-to-drain  
5 ohmic contact spacing of 5.0  $\mu\text{m}$  (which can be typical for transistors configured for 50-volt operation). The results of FIG. 8 indicate that a thicker GaN epitaxy is desired to minimize the active area capacitance and capacitive coupling to a highly conductive silicon substrate (which may be held at a reference potential, such as ground potential).

While several embodiments of the present invention have been described and  
10 illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the functions and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the present invention. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials,  
15 and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the teachings of the present invention is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments of the invention  
20 described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, the invention may be practiced otherwise than as specifically described and claimed. The present invention is directed to each individual feature, system, article, material, and/or method described herein. In addition, any combination  
25 of two or more such features, systems, articles, materials, and/or methods, if such features, systems, articles, materials, and/or methods are not mutually inconsistent, is included within the scope of the present invention.

In cases where the present specification and a document incorporated by reference include conflicting and/or inconsistent disclosure, the present specification  
30 shall control. If two or more documents incorporated by reference include conflicting and/or inconsistent disclosure with respect to each other, then the document having the later effective date shall control.

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All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

5 The indefinite articles “a” and “an,” as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean “at least one.”

10 The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Other elements may optionally be present other than the elements specifically identified by the “and/or” clause, whether related or unrelated to those elements specifically identified unless clearly indicated to the contrary. Thus, as a non-limiting example, a reference to “A and/or B,” when used in conjunction with open-ended language such as “comprising” can refer, in one embodiment, to A without B (optionally including elements other than B); in another embodiment, to B without A (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

15 As used herein in the specification and in the claims, “or” should be understood to have the same meaning as “and/or” as defined above. For example, when separating items in a list, “or” or “and/or” shall be interpreted as being inclusive, i.e., the inclusion of at least one, but also including more than one, of a number or list of elements, and, optionally, additional unlisted items. Only terms clearly indicated to the contrary, such as “only one of” or “exactly one of,” or, when used in the claims, “consisting of,” will refer to the inclusion of exactly one element of a number or list of elements. In general, the term “or” as used herein shall only be interpreted as indicating exclusive alternatives (i.e. “one or the other but not both”) when preceded by terms of exclusivity, such as “either,” “one of,” “only one of,” or “exactly one of.” “Consisting essentially of,” when used in the claims, shall have its ordinary meaning as used in the field of patent law.

20 As used herein in the specification and in the claims, the phrase “at least one,” in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the

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elements specifically identified within the list of elements to which the phrase “at least one” refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, “at least one of A and B” (or, equivalently, “at least one of A or B,” or, equivalently “at least one of A and/or B”) can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

In the claims, as well as in the specification above, all transitional phrases such as “comprising,” “including,” “carrying,” “having,” “containing,” “involving,” “holding,” and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases “consisting of” and “consisting essentially of” shall be closed or semi-closed transitional phrases, respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

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### CLAIMS

What is claimed is:

1. A semiconductor structure for an integrated circuit component, comprising:  
a substrate, at least a portion of which is made of bulk silicon having an  
5 electronic resistivity of less than  $0.10 \Omega\text{-cm}$  when the silicon is at  $25 \text{ }^\circ\text{C}$ ; and  
a III-nitride material region located over the substrate.
2. A semiconductor structure for an integrated circuit component, comprising:  
a substrate, at least a portion of which comprises silicon having an electronic  
10 resistivity of less than  $0.10 \Omega\text{-cm}$  when the silicon is at  $25 \text{ }^\circ\text{C}$ ; and  
a III-nitride material region located over the substrate, wherein the integrated  
circuit component is configured to operate at a frequency greater than  $50 \text{ MHz}$ .
3. The semiconductor structure of claim 1, wherein the integrated circuit component  
15 is configured to operate at a frequency greater than  $50 \text{ MHz}$ .
4. The semiconductor structure of any one of claims 1 through 3, wherein the  
integrated circuit component is an active device.
- 20 5. The semiconductor structure of any one of claims 1 through 4, wherein the  
integrated circuit component is a discrete component.
6. The semiconductor structure of any one of claims 1 through 5, wherein the  
substrate includes a silicon-on-insulator structure.  
25
7. The semiconductor structure of any one of claims 2 through 5, wherein the  
substrate comprises bulk silicon or silicon carbide.
8. The semiconductor structure of any one of claims 1 through 7, wherein the III-  
30 nitride material region comprises gallium nitride material.
9. The semiconductor structure of any one of claims 1 through 8, wherein the III-  
nitride material region comprises:

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a nucleation layer formed over the substrate;  
a buffer layer formed over the nucleation layer; and  
a device region formed over the buffer layer.

- 5 10. The semiconductor structure of claim 9, further comprising a transition layer located between the nucleation layer and the buffer layer.
11. The semiconductor structure of claim 10, wherein the transition layer is a superlattice.
- 10 12. The semiconductor structure of claim 10 or 11, wherein the transition layer is compositionally graded.
13. The semiconductor structure of any one of claims 9 through 12, further comprising the integrated circuit component that is formed, at least in part, in the device region.
- 15 14. The semiconductor structure of claim 13, wherein the integrated circuit component is a transistor or a diode.
- 20 15. The semiconductor structure of claim 14, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
16. The semiconductor structure of claim 14 or 15, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm.
- 25 17. The semiconductor structure of any one of claims 14 through 16, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
- 30 18. The semiconductor structure of any one of claims 14 through 17, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.



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19. A semiconductor device, comprising:  
a substrate, at least a portion of which comprises silicon;  
a III-nitride material region having a thickness of at least 2.0 micrometers located over  
5 the substrate;  
a source electrode over the III-nitride material region, the source electrode defining a  
source electrode interfacial area with the III-nitride material region;  
a drain electrode over the III-nitride material region, the drain electrode defining a drain  
electrode interfacial area with the III-nitride material region; and  
10 a gate electrode over the III-nitride material region, the gate electrode defining a gate  
electrode interfacial area with the III-nitride material region;  
wherein:  
the source electrode, and the drain electrode, and the gate electrode define an active area,  
and  
15 the sum of the source electrode interfacial area, the drain electrode interfacial area, and  
the gate electrode interfacial area is less than 30% of the active area.

20. A semiconductor device, comprising:  
a substrate, at least a portion of which comprises silicon;  
20 a III-nitride material region having a thickness of at least 2.0 micrometers located over  
the substrate;  
at least one cathode electrode over the III-nitride material region, the at least one cathode  
electrode defining a cathode electrode interfacial area with the III-nitride material region;  
and  
25 an anode electrode over the III-nitride material region, the anode electrode defining an  
anode electrode interfacial area with the III-nitride material region;  
wherein:  
the at least one cathode electrode and the anode electrode define an active area, and  
the sum of the cathode electrode interfacial area and the anode electrode  
30 interfacial area is less than 30% of the active area.

21. A semiconductor device, comprising:  
a substrate, at least a portion of which comprises silicon;

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- a III-nitride material region having a thickness of at least 2.0 micrometers located over the substrate;
- an ohmic contact over the III-nitride material region, the ohmic contact defining an ohmic contact interfacial area with the III-nitride material region; and
- 5 a gate electrode over the III-nitride material region, the gate electrode defining a gate electrode interfacial area with the III-nitride material region, wherein the ohmic contact interfacial area is less than 50 times the gate electrode interfacial area.
- 10 22. The semiconductor device of any of claims 19 through 21, further comprising an integrated circuit component formed in the III-nitride material region and including the ohmic contact.
23. The semiconductor device of claim 22, wherein the integrated circuit component is
- 15 configured to operate at a frequency greater than 50 MHz.
24. The semiconductor device of claim 22 or 23, wherein the substrate includes a silicon-on-insulator structure.
- 20 25. The semiconductor device of any one of claims 19 through 24, wherein the substrate comprises bulk silicon or silicon carbide.
26. The semiconductor device of any one of claims 19 through 25, wherein the III-nitride material region comprises gallium nitride material.
- 25 27. The semiconductor device of any one of claims 19 through 26, wherein the III-nitride material region comprises:
- a nucleation layer formed over the substrate;
  - a buffer layer formed over the nucleation layer; and
  - 30 a device region formed over the buffer layer.
28. The semiconductor device of claim 27, further comprising a transition layer located between the nucleation layer and the buffer layer.

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29. The semiconductor device of claim 28, wherein the transition layer is compositionally graded.
- 5 30. The semiconductor device any one of claims 27 through 29, wherein the integrated circuit component is formed, at least in part, in the device region.
31. The semiconductor device of claim 30, wherein the integrated circuit component is a transistor or a diode.
- 10 32. The semiconductor device of claim 31, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
33. The semiconductor device of claim 31 or 32, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm.
- 15 34. The semiconductor device of any one of claims 31 through 33, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
- 20 35. The semiconductor device of any one of claims 31 through 34, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
- 25 36. A semiconductor device comprising:  
a substrate, at least a portion of which comprises silicon;  
a III-nitride material region having a thickness of at least 2.0 micrometers located over the substrate;  
30 an integrated circuit component formed, at least in part, in the III-nitride material region; and  
at least one ohmic contact over the III-nitride material region,  
wherein:

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the at least one ohmic contact defines, at least in part, an active area of the integrated circuit component, and  
an active-area capacitance ratio for the integrated circuit component is no greater than 0.4 pF/mm.

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37. The semiconductor device of claim 36, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.

38. The semiconductor device of claim 36 or 37, wherein the substrate includes a  
10 silicon-on-insulator structure.

39. The semiconductor device of any one of claims 36 through 38, wherein the substrate comprises bulk silicon or silicon carbide.

15 40. The semiconductor device of any one of claims 36 through 39, wherein the III-nitride material region comprises gallium nitride material.

41. The semiconductor device of any one of claims 36 through 40, wherein the III-nitride material region comprises:

20 a nucleation layer formed over the substrate;  
a buffer layer formed over the nucleation layer; and  
a device region formed over the buffer layer.

42. The semiconductor device of any one of claims 36 through 41, further comprising a  
25 transition layer located between the nucleation layer and the buffer layer.

43. The semiconductor device of claim 42, wherein the transition layer is compositionally graded.

30 44. The semiconductor device of any one of claims 41 through 43, wherein the integrated circuit component is formed, at least in part, in the device region.

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45. The semiconductor device of any one of claims 36 through 44, wherein the integrated circuit component is a transistor or a diode.
46. The semiconductor device of claim 45, wherein the transistor or diode is  
5 configured to operate at a frequency between 100 MHz and 20 GHz.
47. The semiconductor device of claim 45 or 46, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the semiconductor  
10 device and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the semiconductor device.
48. The semiconductor device of any one of claims 45 through 47, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of  
15 the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
49. The semiconductor device of any one of claims 45 through 48, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is  
20 increased to 125 °C.
50. A semiconductor device, comprising:  
a substrate, at least a portion of which is bulk silicon; and  
a III-nitride material region located over the substrate, wherein:  
25 the semiconductor device is configured such that at 25°C, the device is capable of a power added efficiency of at least 50%, and  
the semiconductor device is configured such that:  
when the substrate is increased in temperature from 25°C to 105 °C, the device exhibits a drop in power added efficiency of less than 5%, and/or  
30 when the substrate is increased in temperature from 25°C to 125 °C, the device exhibits a drop in power added efficiency of less than 10%.

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51. The semiconductor device of claim 50, wherein the semiconductor device is configured to operate at a frequency greater than 50 MHz.
52. The semiconductor device of claim 50 or 51, wherein the substrate includes a silicon-on-insulator structure.
53. The semiconductor device of any one of claims 50 through 52, wherein the III-nitride material region comprises gallium nitride material.
- 10 54. The semiconductor device of any one of claims 50 through 53, wherein the III-nitride material region comprises:
- a nucleation layer formed over the substrate;
  - a buffer layer formed over the nucleation layer; and
  - a device region formed over the buffer layer.
- 15 55. The semiconductor device of claim 54, further comprising a transition layer located between the nucleation layer and the buffer layer.
56. The semiconductor device of claim 55, wherein the transition layer is compositionally graded.
- 20 57. The semiconductor device of any one of claims 54 through 56, wherein the semiconductor device comprises a transistor and is formed, at least in part, in the device region.
- 25 58. The semiconductor device of any one of claims 50 through 57, wherein the semiconductor device is configured to operate at a frequency between 100 MHz and 20 GHz.
- 30 59. The semiconductor device of any one of claims 50 through 58, wherein the semiconductor device has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the semiconductor device and a length value for the active-area

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capacitance ratio is based on a peripheral length of a gate or anode of the semiconductor device.

60. The semiconductor device of any one of claims 57 through 59, wherein an amount  
5 of power dissipated into the substrate due to capacitive coupling between components of the transistor and the substrate is no larger than  $0.1 \text{ Watts/mm}^2$  when the substrate temperature is at  $120 \text{ }^\circ\text{C}$ .

61. The semiconductor device of any one of claims 57 through 60, wherein a power  
10 added efficiency of the transistor remains above 50 % when the substrate temperature is increased to  $125 \text{ }^\circ\text{C}$ .

62. A semiconductor structure, comprising:  
a substrate, at least a portion of which is electronically conductive, the substrate having a  
15 thickness of less than 150 micrometers;  
a III-nitride material region located over the substrate; and  
an electronically conductive material located over the III-nitride material region,  
wherein:

20 the electronically conductive material is electrically coupled to the electronically conductive portion of the substrate through the thickness of the III-nitride material region.

63. The semiconductor structure of claim 62, wherein the electronically conductive  
25 material extends through the III-nitride material region and is connected between the substrate and at least one integrated circuit component formed at least in part in the III-nitride material region, wherein the electrically conductive material provides a reference potential for the integrated circuit component.

64. The semiconductor structure of claim 62 or 63, further comprising and integrated  
30 circuit component wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.

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65. The semiconductor structure of any one of claims 62 through 64, wherein the substrate includes a silicon-on-insulator structure.
66. The semiconductor structure of any one of claims 62 through 65, wherein the substrate comprises bulk silicon or silicon carbide.
67. The semiconductor structure of any one of claims 62 through 66, wherein the III-nitride material region comprises gallium nitride material.
68. The semiconductor structure of any one of claims 62 through 67, wherein the III-nitride material region comprises:
- a nucleation layer formed over the substrate;
  - a buffer layer formed over the nucleation layer; and
  - a device region formed over the buffer layer.
69. The semiconductor structure of claim 68, further comprising a transition layer located between the nucleation layer and the buffer layer.
70. The semiconductor structure of claim 69, wherein the transition layer is compositionally graded.
71. The semiconductor structure of any one of claims 62 through 70, further comprising an integrated circuit component wherein the integrated circuit component is formed, at least in part, in the device region.
72. The semiconductor structure of claim 71, wherein the integrated circuit component is a transistor or a diode.
73. The semiconductor structure of claim 72, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
74. The semiconductor structure of claim 72 or 73, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance



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value for the active-area capacitance ratio is based on an active area of the semiconductor device and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the semiconductor device.

- 5 75. The semiconductor structure of any one of claims 72 through 74, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than  $0.1 \text{ Watts/mm}^2$  when the substrate temperature is at  $120 \text{ }^\circ\text{C}$ .
- 10 76. The semiconductor structure of any one of claims 72 through 75, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to  $125 \text{ }^\circ\text{C}$ .
- 15 77. A semiconductor device, comprising:  
a substrate comprising silicon;  
a III-nitride material region located over the substrate;  
at least one ohmic contact located over the substrate and the III-nitride material region and defining an ohmic contact interfacial area with the III-nitride material region;  
a dielectric region located over the substrate and over the III-nitride material  
20 region; and  
at least one contact pad located over the substrate, over the III-nitride material region, and over the dielectric region, the at least one contact pad defining a contact pad area,  
wherein the ratio of the ohmic contact interfacial area to the contact pad area is  
25 less than 28%.
- 30 78. The semiconductor device of claim 77, further comprising an integrated circuit component formed in the III-nitride material region and including the at least one ohmic contact.
79. The semiconductor device of claim 78, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.

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80. The semiconductor device of any one of claims 77 through 79, wherein the substrate includes a silicon-on-insulator structure.
81. The semiconductor device of any one of claims 77 through 80, wherein the substrate comprises bulk silicon or silicon carbide.
82. The semiconductor device of any one of claims 77 through 81, wherein the III-nitride material region comprises gallium nitride material.
83. The semiconductor device of any one of claims 77 through 82, wherein the III-nitride material region comprises:
- a nucleation layer formed over the substrate;
  - a buffer layer formed over the nucleation layer; and
  - a device region formed over the buffer layer.
84. The semiconductor device of claim 83, further comprising a transition layer located between the nucleation layer and the buffer layer.
85. The semiconductor device of claim 84, wherein the transition layer is compositionally graded.
86. The semiconductor device of any one of claims 78 and 83 through 85, wherein the integrated circuit component is formed, at least in part, in the device region.
87. The semiconductor device of any one of claims 83 through 86, wherein the integrated circuit component is a transistor or a diode.
88. The semiconductor device of claim 87, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
89. The semiconductor device of claims 87 or 88, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the semiconductor

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device and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the semiconductor device.

90. The semiconductor device of any one of claims 87 through 89, wherein an amount  
5 of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
91. The semiconductor device of any one of claims 87 through 90, wherein a power  
10 added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
92. A structure comprising:  
a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
15 a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and wherein the integrated circuit component has a ratio of an active-area of the device, measured in square microns, to a gate or anode peripheral length, measured in microns, that is no greater than 200.  
20
93. The structure of claim 92, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.
94. The structure of claim 92 or 93, wherein the substrate includes a silicon-on-  
25 insulator structure.
95. The structure of any one of claims 92 through 94, wherein the substrate comprises bulk silicon or silicon carbide.
- 30 96. The structure of any one of claims 92 through 95, wherein the III-nitride material region comprises gallium nitride material.

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97. The structure of any one of claims 92 through 96, wherein the III-nitride material region comprises:
- a nucleation layer formed over the substrate;
  - a buffer layer formed over the nucleation layer; and
  - 5 a device region formed over the buffer layer.
98. The structure of claim 97, further comprising a transition layer located between the nucleation layer and the buffer layer.
- 10 99. The structure of claim 98, wherein the transition layer is compositionally graded.
100. The structure of any one of claims 97 through 99, wherein the integrated circuit component is formed, at least in part, in the device region.
- 15 101. The structure of any one of claims 92 through 100, wherein the integrated circuit component is a transistor or a diode.
102. The structure of claim 101, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
- 20 103. The structure of claim 101 or 102, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate
- 25 or anode of the transistor or diode.
104. The structure of any one of claims 101 through 103, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate
- 30 temperature is at 120 °C.

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105. The structure of any one of claims 101 through 104, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
- 5 106. A structure, comprising:  
a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one ohmic contact of a first type, wherein the integrated circuit  
10 component has a ratio of an ohmic contact interfacial area, measured in square microns, for the first type of ohmic contact to a gate or anode peripheral length, measured in microns, that is no greater than 30.
107. The structure of claim 106, wherein the integrated circuit component is configured  
15 to operate at a frequency greater than 50 MHz.
108. The structure of claim 106 or 107, wherein the substrate includes a silicon-on-insulator structure.
- 20 109. The structure of any one of claims 106 through 108, wherein the substrate comprises bulk silicon or silicon carbide.
110. The structure of any one of claims 106 through 109, wherein the III-nitride material region comprises gallium nitride material.  
25
111. The structure of any one of claims 106 through 110, wherein the III-nitride material region comprises:  
a nucleation layer formed over the substrate;  
a buffer layer formed over the nucleation layer; and  
30 a device region formed over the buffer layer.
112. The structure of claim 111, further comprising a transition layer located between the nucleation layer and the buffer layer.

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113. The structure of claim 112, wherein the transition layer is compositionally graded.
114. The structure of any one of claims 111 through 113, wherein the integrated circuit  
5 component is formed, at least in part, in the device region.
115. The structure of any one of claims 106 through 114, wherein the integrated circuit component is a transistor or a diode.
- 10 116. The structure of claim 115, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
117. The structure of claim 115 or 116, wherein the transistor or diode has an active-area  
15 active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.
118. The structure of any one of claims 115 through 117, wherein an amount of power  
20 dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
119. The structure of any one of claims 115 through 118, wherein a power added  
25 efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
120. A structure, comprising:  
30 a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one gate or anode contact pad, wherein the integrated circuit component has a ratio of a contact-pad area, measured in square microns, for the at least

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one gate or anode contact pad to a gate or anode peripheral length, measured in microns, that is no greater than 20.

5 121. The structure of claim 120, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.

122. The structure of claim 120 or 121, wherein the substrate includes a silicon-on-insulator structure.

10 123. The structure of any one of claims 120 through 122, wherein the substrate comprises bulk silicon or silicon carbide.

124. The structure of any one of claims 120 through 123, wherein the III-nitride material region comprises gallium nitride material.

15

125. The structure of any one of claims 120 through 124, wherein the III-nitride material region comprises:

- a nucleation layer formed over the substrate;
- a buffer layer formed over the nucleation layer; and
- 20 a device region formed over the buffer layer.

20

126. The structure of claim 125, further comprising a transition layer located between the nucleation layer and the buffer layer.

25 127. The structure of claim 126, wherein the transition layer is compositionally graded.

128. The structure of any one of claims 125 through 127, wherein the integrated circuit component is formed, at least in part, in the device region and is a transistor or diode.

30 129. The structure of claim 128, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.

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130. The structure of claim 128 or 129, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.
- 5
131. The structure of any one of claims 128 through 130, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
- 10
132. The structure of any one of claims 128 through 131, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
- 15
133. A structure, comprising:
- a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;
  - a III-nitride material region located over the substrate; and
  - an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one drain, source, or cathode contact pad, wherein the integrated circuit component has a ratio of a contact-pad area, measured in square microns, for the at least one drain, source, or cathode contact pad to a gate or anode peripheral length, measured in microns, that is no greater than 50.
- 20
134. The structure of claim 133, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.
- 25
135. The structure of claim 133 or 134, wherein the substrate includes a silicon-on-insulator structure.
- 30
136. The structure of any one of claims 133 through 135, wherein the substrate comprises bulk silicon or silicon carbide.



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137. The structure of any one of claims 133 through 136, wherein the III-nitride material region comprises gallium nitride material.
138. The structure of any one of claims 133 through 137, wherein the III-nitride material region comprises:
- a nucleation layer formed over the substrate;
  - a buffer layer formed over the nucleation layer; and
  - a device region formed over the buffer layer.
139. The structure of claim 138, further comprising a transition layer located between the nucleation layer and the buffer layer.
140. The structure of claim 139, wherein the transition layer is compositionally graded.
141. The structure of any one of claims 138 through 140, wherein the integrated circuit component is formed, at least in part, in the device region and is a transistor or diode.
142. The structure of claim 141, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
143. The structure of claims 141 or 142, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.
144. The structure of any one of claims 141 through 143, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.

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145. The structure of any one of claims 141 through 144, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
- 5 146. A structure, comprising:  
a substrate comprising silicon and having a bulk resistivity less than 0.10  $\Omega$ -cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one ohmic contact of a first type, wherein the integrated circuit  
10 component has a ratio of an ohmic contact capacitance, in picofarads, calculated based on an area of the at least one ohmic contact, for the first type of ohmic contact to a gate or anode peripheral length, measured in millimeters, that is no greater than 2.5.
147. The structure of claim 146, wherein the integrated circuit component is configured  
15 to operate at a frequency greater than 50 MHz.
148. The structure of claim 146 or 147, wherein the substrate includes a silicon-on-insulator structure.
- 20 149. The structure of any one of claims 146 through 148, wherein the substrate comprises bulk silicon or silicon carbide.
150. The structure of any one of claims 146 through 149, wherein the III-nitride material region comprises gallium nitride material.  
25
151. The structure of any one of claims 146 through 150, wherein the III-nitride material region comprises:  
a nucleation layer formed over the substrate;  
a buffer layer formed over the nucleation layer; and  
30 a device region formed over the buffer layer.
152. The structure of claim 151, further comprising a transition layer located between the nucleation layer and the buffer layer.

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153. The structure of claim 152, wherein the transition layer is compositionally graded.
154. The structure of any one of claims 151 through 153, wherein the integrated circuit  
5 component is formed, at least in part, in the device region.
155. The structure of any one of claims 151 through 154, wherein the integrated circuit component is a transistor or a diode.
- 10 156. The structure of claim 155, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
157. The structure of claim 155 or 156, wherein the transistor or diode has an active-area  
15 active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.
- 20 158. The structure of any one of claims 155 through 157, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
- 25 159. The structure of any one of claims 155 through 158, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
160. A structure, comprising:  
a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
30 a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one gate or anode contact pad, wherein the integrated circuit component has a ratio of a contact pad capacitance, in picofarads, calculated based on an

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area of the at least one gate or anode contact pad, to a gate or anode peripheral length, measured in millimeters, that is no greater than 1.0.

5 161. The structure of claim 160, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.

162. The structure of claim 160 or 161, wherein the substrate includes a silicon-on-insulator structure.

10 163. The structure of any one of claims 160 through 162, wherein the substrate comprises bulk silicon or silicon carbide.

164. The structure of any one of claims 160 through 163, wherein the III-nitride material region comprises gallium nitride material.

15 165. The structure of claim 160, wherein the III-nitride material region comprises:  
a nucleation layer formed over the substrate;  
a buffer layer formed over the nucleation layer; and  
a device region formed over the buffer layer.

20 166. The structure of claim 165, further comprising a transition layer located between the nucleation layer and the buffer layer.

167. The structure of claim 167, wherein the transition layer is compositionally graded.

25 168. The structure of any one of claims 165 through 167, wherein the integrated circuit component is formed, at least in part, in the device region and is a transistor or a diode.

30 169. The structure of claim 168, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.

170. The structure of claim 168 or 169, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the

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active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.

- 5 171. The structure of any one of claims 168 through 170, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
- 10 172. The structure of any one of claims 168 through 171, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
173. A structure, comprising:
- 15 a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one source, drain, or cathode contact pad, wherein the integrated circuit component has a ratio of a contact pad capacitance, in picofarads,  
20 calculated based on an area for the at least one source, drain, or cathode contact pad, to a gate or anode peripheral length, measured in millimeters, that is no greater than 1.5.
174. The structure of claim 173, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.
- 25 175. The structure of claim 173 or 174, wherein the substrate includes a silicon-on-insulator structure.
176. The structure of any one of claims 173 through 175, wherein the substrate  
30 comprises bulk silicon or silicon carbide.
177. The structure of any one of claims 173 through 176, wherein the III-nitride material region comprises gallium nitride material.

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178. The structure of any one of claims 173 through 177, wherein the III-nitride material region comprises:

- 5 a nucleation layer formed over the substrate;
- a buffer layer formed over the nucleation layer; and
- a device region formed over the buffer layer.

179. The structure of claim 178, further comprising a transition layer located between the nucleation layer and the buffer layer.

10

180. The structure of claim 179, wherein the transition layer is compositionally graded.

181. The structure of any one of claims 178 through 180, wherein the integrated circuit component is formed, at least in part, in the device region and is a transistor or a diode.

15

182. The structure of claim 181, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.

20

183. The structure of claim 181 or 182, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.

25

184. The structure of any one of claims 181 through 183, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.

30

185. The structure of any one of claims 181 through 184, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.

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186. A semiconductor device comprising:  
a substrate, at least a portion of which comprises silicon;  
a III-nitride material region having a thickness of at least 2.0 micrometers located over the substrate;
- 5 an integrated circuit component formed, at least in part, in the III-nitride material region; and  
at least one ohmic contact over the III-nitride material region,  
wherein:  
the at least one ohmic contact defines, at least in part, an active area of the integrated  
10 circuit component, and  
an active-area capacitance ratio for the integrated circuit component is no greater than 0.4 pF/mm.
187. The semiconductor device of claim 186, wherein the integrated circuit component  
15 is configured to operate at a frequency greater than 50 MHz.
188. The semiconductor device of any one of claims 186 through 187, wherein the substrate includes a silicon-on-insulator structure.
- 20 189. The semiconductor device of any one of claims 186 through 187, wherein the substrate comprises bulk silicon or silicon carbide.
190. The semiconductor device of any one of claims 186 through 189, wherein the III-nitride material region comprises gallium nitride material.  
25
191. The semiconductor device of any one of claims 186 through 190, wherein the III-nitride material region comprises:  
a nucleation layer formed over the substrate;  
a buffer layer formed over the nucleation layer; and  
30 a device region formed over the buffer layer.
192. The semiconductor device of claim 191, further comprising a transition layer located between the nucleation layer and the buffer layer.

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193. The semiconductor device of claim 192, wherein the transition layer is compositionally graded.
- 5 194. The semiconductor device of any one of claims 186 through 193, wherein the integrated circuit component is formed, at least in part, in the device region.
195. The semiconductor device of any one of claims 186 through 194, wherein the integrated circuit component is a transistor or a diode.
- 10 196. The semiconductor device of claim 195, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
197. The semiconductor device of claim 195, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the semiconductor device and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the semiconductor device.
- 15 198. The semiconductor device of any one of claims 195 through 197, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
- 20 199. The semiconductor device of any one of claims 195 through 198, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
- 25 200. A structure comprising:
- 30 a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and wherein the integrated circuit component has a ratio of an active-area of the



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device, measured in square microns, to a gate or anode peripheral length, measured in microns, that is no greater than 200.

201. The structure of of claim 200, wherein the integrated circuit component is  
5 configured to operate at a frequency greater than 50 MHz.

202. The structure of any one of claims 200-201, wherein the substrate includes a silicon-on-insulator structure.

10 203. The structure of any one of claims 200-201, wherein the substrate comprises bulk silicon or silicon carbide.

204. The structure of any one of claims 200-203, wherein the III-nitride material region comprises gallium nitride material.

15

205. The structure of any one of claims 200-204, wherein the III-nitride material region comprises:

- a nucleation layer formed over the substrate;
- a buffer layer formed over the nucleation layer; and
- 20 a device region formed over the buffer layer.

206. The structure of claim 205, further comprising a transition layer located between the nucleation layer and the buffer layer.

25 207. The structure of claim 206, wherein the transition layer is compositionally graded.

208. The structure of any one of claims 200-207, wherein the integrated circuit component is formed, at least in part, in the device region.

30 209. The structure of any one of claims 200-208, wherein the integrated circuit component is a transistor or a diode.

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210. The structure of claim 209, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
211. The structure of any one of claims 209-210, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.
212. The structure of any one of claims 209-211, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
213. The structure of any one of claims 209-212, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
214. A structure, comprising:  
a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one ohmic contact of a first type, wherein the integrated circuit component has a ratio of an ohmic contact interfacial area, measured in square microns, for the first type of ohmic contact to a gate or anode peripheral length, measured in microns, that is no greater than 30.
215. The structure of claim 214, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.
216. The structure of any one of claims 214-215, wherein the substrate includes a silicon-on-insulator structure.

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217. The structure of any one of claims 214-215, wherein the substrate comprises bulk silicon or silicon carbide.
218. The structure of any one of claims 214-217, wherein the III-nitride material region  
5 comprises gallium nitride material.
219. The structure of any one of claims 214-218, wherein the III-nitride material region comprises:
- 10 a nucleation layer formed over the substrate;
  - a buffer layer formed over the nucleation layer; and
  - a device region formed over the buffer layer.
220. The structure of claim 219, further comprising a transition layer located between the nucleation layer and the buffer layer.  
15
221. The structure of claim 220, wherein the transition layer is compositionally graded.
222. The structure of any one of claims 214-221, wherein the integrated circuit component is formed, at least in part, in the device region.  
20
223. The structure of any one of claims 214-222, wherein the integrated circuit component is a transistor or a diode.
224. The structure of claim 223, wherein the transistor or diode is configured to operate  
25 at a frequency between 100 MHz and 20 GHz.
225. The structure of any one of claims 223-224, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or  
30 diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.

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226. The structure of any one of claims 223-225, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than  $0.1 \text{ Watts/mm}^2$  when the substrate temperature is at  $120 \text{ }^\circ\text{C}$ .

5

227. The structure of any one of claims 223-226, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to  $125 \text{ }^\circ\text{C}$ .

228. A structure, comprising:

10           a substrate comprising silicon and having a bulk resistivity less than  $0.10 \text{ } \Omega\text{-cm}$ ;  
              a III-nitride material region located over the substrate; and  
              an integrated circuit component formed, at least in part, in the III-nitride material  
region and having at least one ohmic contact of a first type, wherein the integrated circuit  
component has a ratio of an ohmic contact capacitance, in picofarads, calculated based  
15           on an area of the at least one ohmic contact, for the first type of ohmic contact to a gate  
or anode peripheral length, measured in millimeters, that is no greater than 2.5.

229. The structure of claim 228, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.

20

230. The structure of any one of claims 228-229, wherein the substrate includes a silicon-on-insulator structure.

231. The structure of any one of claims 228-229, wherein the substrate comprises bulk  
25           silicon or silicon carbide.

232. The structure of any one of claims 228-231, wherein the III-nitride material region comprises gallium nitride material.

30           233. The structure of any one of claims 228-232, wherein the III-nitride material region comprises:

              a nucleation layer formed over the substrate;

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a buffer layer formed over the nucleation layer; and  
a device region formed over the buffer layer.

234. The structure of claim 233, further comprising a transition layer located between  
5 the nucleation layer and the buffer layer.
235. The structure of claim 234, wherein the transition layer is compositionally graded.
236. The structure of any one of claims 228-235, wherein the integrated circuit  
10 component is formed, at least in part, in the device region.
237. The structure of claim 233, wherein the integrated circuit component is a transistor  
or a diode.
- 15 238. The structure of claim 237, wherein the transistor or diode is configured to operate  
at a frequency between 100 MHz and 20 GHz.
239. The structure of any one of claims 237-238, wherein the transistor or diode has an  
active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance  
20 value for the active-area capacitance ratio is based on an active area of the transistor or  
diode and a length value for the active-area capacitance ratio is based on a peripheral  
length of a gate or anode of the transistor or diode.
240. The structure of any one of claims 237-239, wherein an amount of power dissipated  
25 into the substrate due to capacitive coupling between components of the transistor or  
diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is  
at 120 °C.
241. The structure of any one of claims 237-240, wherein a power added efficiency of  
30 the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
242. A structure, comprising:  
a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;

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a III-nitride material region located over the substrate; and

an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one gate or anode contact pad, wherein the integrated circuit component has a ratio of a contact-pad area, measured in square microns, for the at least  
5 one gate or anode contact pad to a gate or anode peripheral length, measured in microns, that is no greater than 20.

243. The structure of claim 242, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.

10

244. The structure of any one of claims 242-243, wherein the substrate includes a silicon-on-insulator structure.

245. The structure of any one of claims 242-244, wherein the substrate comprises bulk  
15 silicon or silicon carbide.

246. The structure of any one of claims 242-245, wherein the III-nitride material region comprises gallium nitride material.

20 247. The structure of any one of claims 242-246, wherein the III-nitride material region comprises:

- a nucleation layer formed over the substrate;
- a buffer layer formed over the nucleation layer; and
- a device region formed over the buffer layer.

25

248. The structure of claim 247, further comprising a transition layer located between the nucleation layer and the buffer layer.

249. The structure of claim 248, wherein the transition layer is compositionally graded.

30

250. The structure of any one of claims 242-249, wherein the integrated circuit component is formed, at least in part, in the device region and is a transistor or diode.

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251. The structure of claim 250, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
252. The structure of any one of claims 250-251, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.
253. The structure of any one of claims 250-252, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.
254. The structure of any one of claims 250-253, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
255. A structure, comprising:  
a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one gate or anode contact pad, wherein the integrated circuit component has a ratio of a contact pad capacitance, in picofarads, calculated based on an area of the at least one gate or anode contact pad, to a gate or anode peripheral length, measured in millimeters, that is no greater than 1.0.
256. The structure of claim 255, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.
257. The structure of any one of claims 255-256, wherein the substrate includes a silicon-on-insulator structure.

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258. The structure of any one of claims 255-256, wherein the substrate comprises bulk silicon or silicon carbide.
259. The structure of any one of claims 255-258, wherein the III-nitride material region  
5 comprises gallium nitride material.
260. The structure of any one of claims 255-259, wherein the III-nitride material region comprises:  
a nucleation layer formed over the substrate;  
10 a buffer layer formed over the nucleation layer; and  
a device region formed over the buffer layer.
261. The structure of claim 260, further comprising a transition layer located between the nucleation layer and the buffer layer.  
15
262. The structure of claim 261, wherein the transition layer is compositionally graded.
263. The structure of any one of claims 255-262, wherein the integrated circuit component is formed, at least in part, in the device region and is a transistor or a diode.  
20
264. The structure of claim 263, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
265. The structure of any one of claims 263-264, wherein the transistor or diode has an  
25 active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.
- 30 266. The structure of any one of claims 263-265, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is at 120 °C.



267. The structure of any one of claims 263-266, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to 125 °C.
- 5 268. A structure, comprising:  
a substrate comprising silicon and having a bulk resistivity less than 0.10  $\Omega$ -cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material region and having at least one drain, source, or cathode contact pad, wherein the  
10 integrated circuit component has a ratio of a contact-pad area, measured in square microns, for the at least one drain, source, or cathode contact pad to a gate or anode peripheral length, measured in microns, that is no greater than 50.
269. The structure of claim 268, wherein the integrated circuit component is configured  
15 to operate at a frequency greater than 50 MHz.
270. The structure of any one of claims 268-269, wherein the substrate includes a silicon-on-insulator structure.
- 20 271. The structure of any one of claims 268-269, wherein the substrate comprises bulk silicon or silicon carbide.
272. The structure of any one of claims 268-272, wherein the III-nitride material region comprises gallium nitride material.  
25
273. The structure of any one of claims 268-272, wherein the III-nitride material region comprises:  
a nucleation layer formed over the substrate;  
a buffer layer formed over the nucleation layer; and  
30 a device region formed over the buffer layer.
274. The structure of claim 273, further comprising a transition layer located between the nucleation layer and the buffer layer.

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275. The structure of claim 274, wherein the transition layer is compositionally graded.

276. The structure of any one of claims 268-275, wherein the integrated circuit  
5 component is formed, at least in part, in the device region and is a transistor or diode.

277. The structure of claim 276, wherein the transistor or diode is configured to operate  
at a frequency between 100 MHz and 20 GHz.

10 278. The structure of any one of claims 276-277, wherein the transistor or diode has an  
active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance  
value for the active-area capacitance ratio is based on an active area of the transistor or  
diode and a length value for the active-area capacitance ratio is based on a peripheral  
length of a gate or anode of the transistor or diode.

15 279. The structure of any one of claims 276-278, wherein an amount of power dissipated  
into the substrate due to capacitive coupling between components of the transistor or  
diode and the substrate is no larger than 0.1 Watts/mm<sup>2</sup> when the substrate temperature is  
at 120 °C.

20 280. The structure of any one of claims 276-279, wherein a power added efficiency of  
the transistor remains above 50 % when the substrate temperature is increased to 125 °C.

281. A structure, comprising:  
25 a substrate comprising silicon and having a bulk resistivity less than 0.10 Ω-cm;  
a III-nitride material region located over the substrate; and  
an integrated circuit component formed, at least in part, in the III-nitride material  
region and having at least one source, drain, or cathode contact pad, wherein the  
integrated circuit component has a ratio of a contact pad capacitance, in picofarads,  
30 calculated based on an area for the at least one source, drain, or cathode contact pad, to a  
gate or anode peripheral length, measured in millimeters, that is no greater than 1.5.

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282. The structure of claim 281, wherein the integrated circuit component is configured to operate at a frequency greater than 50 MHz.
283. The structure of any one of claims 281-282, wherein the substrate includes a silicon-on-insulator structure.
284. The structure of any one of claims 281-282, wherein the substrate comprises bulk silicon or silicon carbide.
285. The structure of any one of claims 281-284, wherein the III-nitride material region comprises gallium nitride material.
286. The structure of any one of claims 281-285, wherein the III-nitride material region comprises:
- a nucleation layer formed over the substrate;
  - a buffer layer formed over the nucleation layer; and
  - a device region formed over the buffer layer.
287. The structure of claim 286, further comprising a transition layer located between the nucleation layer and the buffer layer.
288. The structure of claim 287, wherein the transition layer is compositionally graded.
289. The structure of any one of claims 281-288, wherein the integrated circuit component is formed, at least in part, in the device region and is a transistor or a diode.
290. The structure of claim 289, wherein the transistor or diode is configured to operate at a frequency between 100 MHz and 20 GHz.
291. The structure of any one of claims 289-290, wherein the transistor or diode has an active-area capacitance ratio that is no larger than 0.4 pF/mm, wherein a capacitance value for the active-area capacitance ratio is based on an active area of the transistor or

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diode and a length value for the active-area capacitance ratio is based on a peripheral length of a gate or anode of the transistor or diode.

5 292. The structure of any one of claims 289-291, wherein an amount of power dissipated into the substrate due to capacitive coupling between components of the transistor or diode and the substrate is no larger than  $0.1 \text{ Watts/mm}^2$  when the substrate temperature is at  $120 \text{ }^\circ\text{C}$ .

10 293. The structure of any one of claims 289-291, wherein a power added efficiency of the transistor remains above 50 % when the substrate temperature is increased to  $125 \text{ }^\circ\text{C}$ .

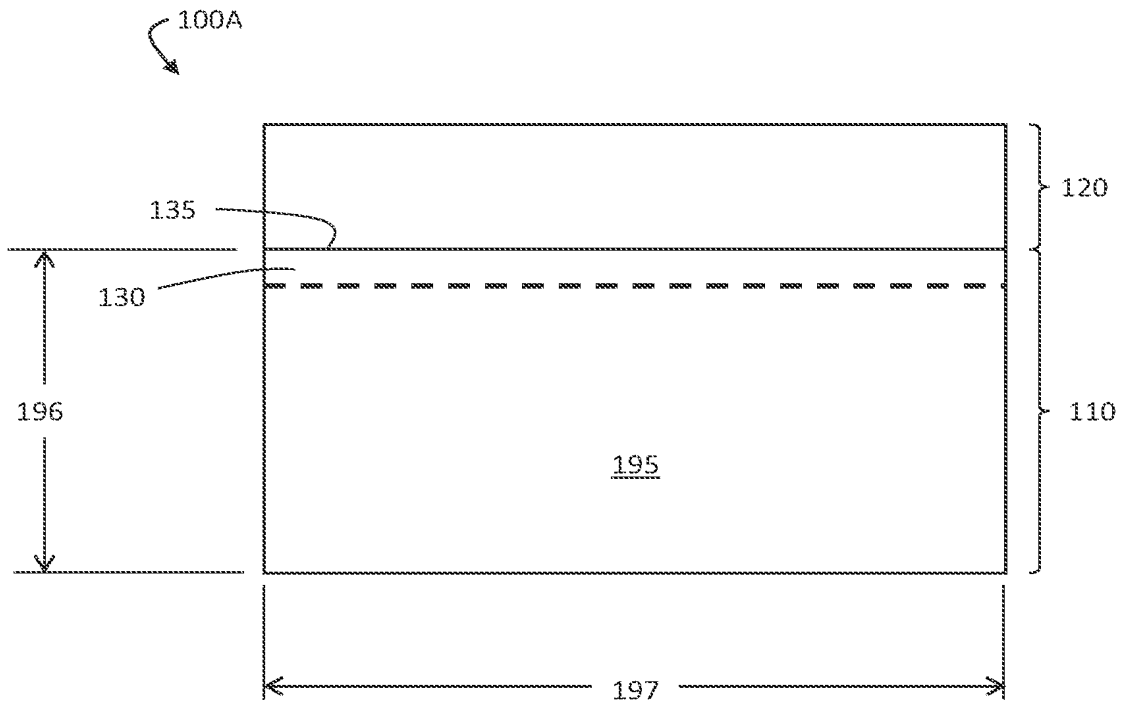


FIG. 1A

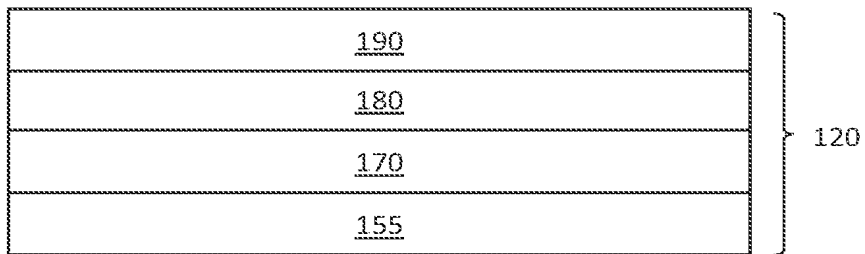
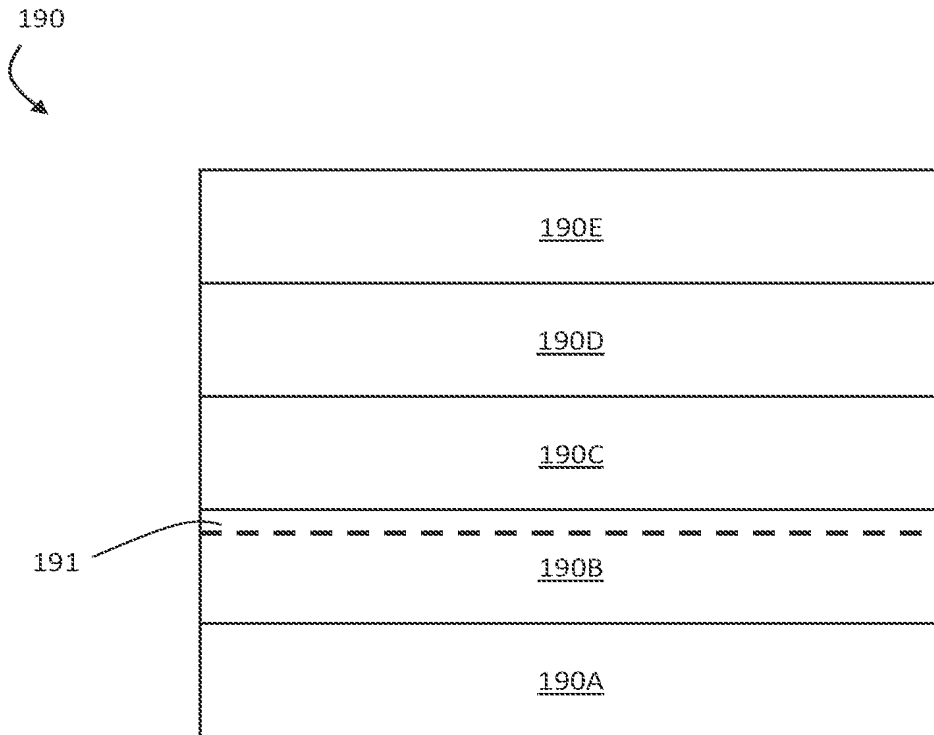


FIG. 1B



*FIG. 1C*

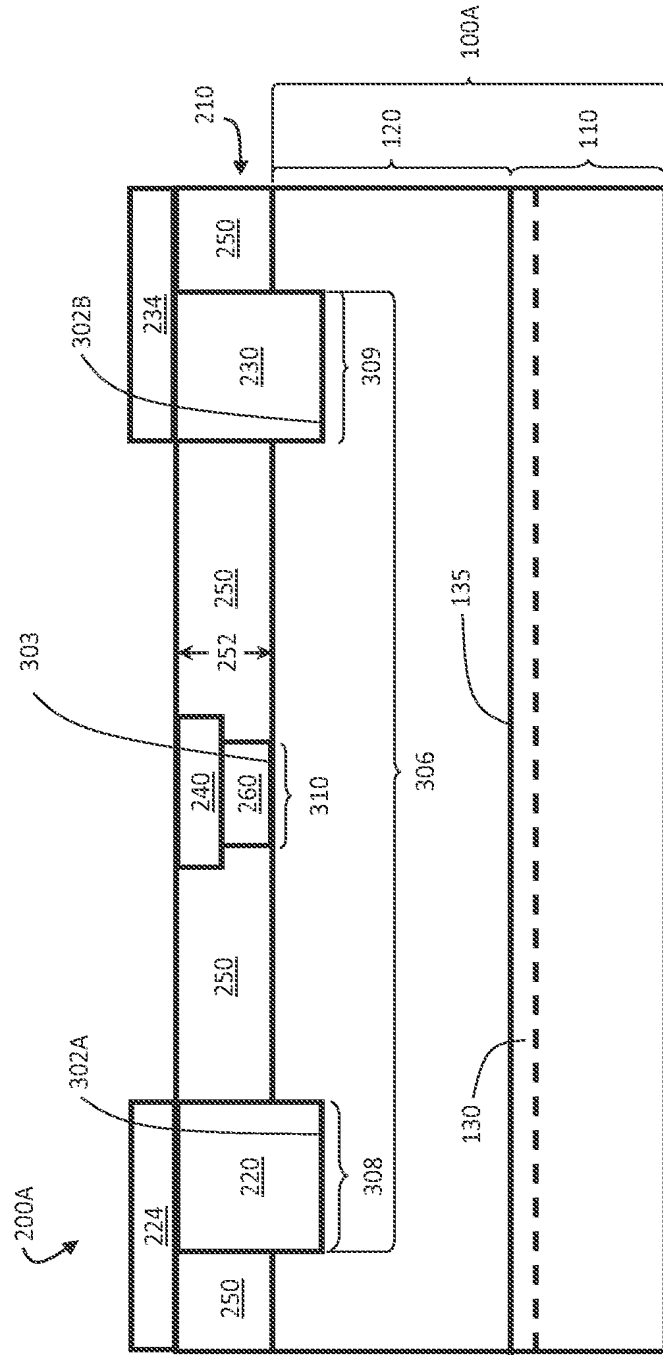


FIG. 2A

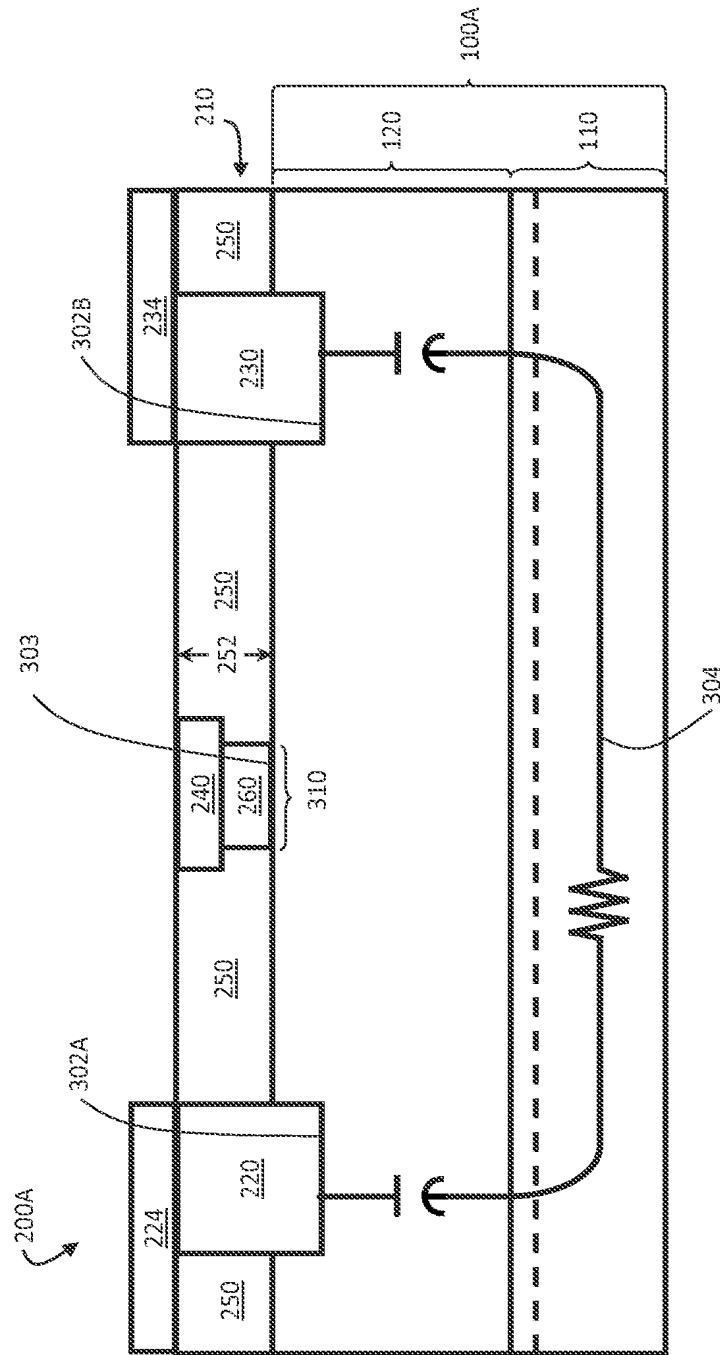


FIG. 2B



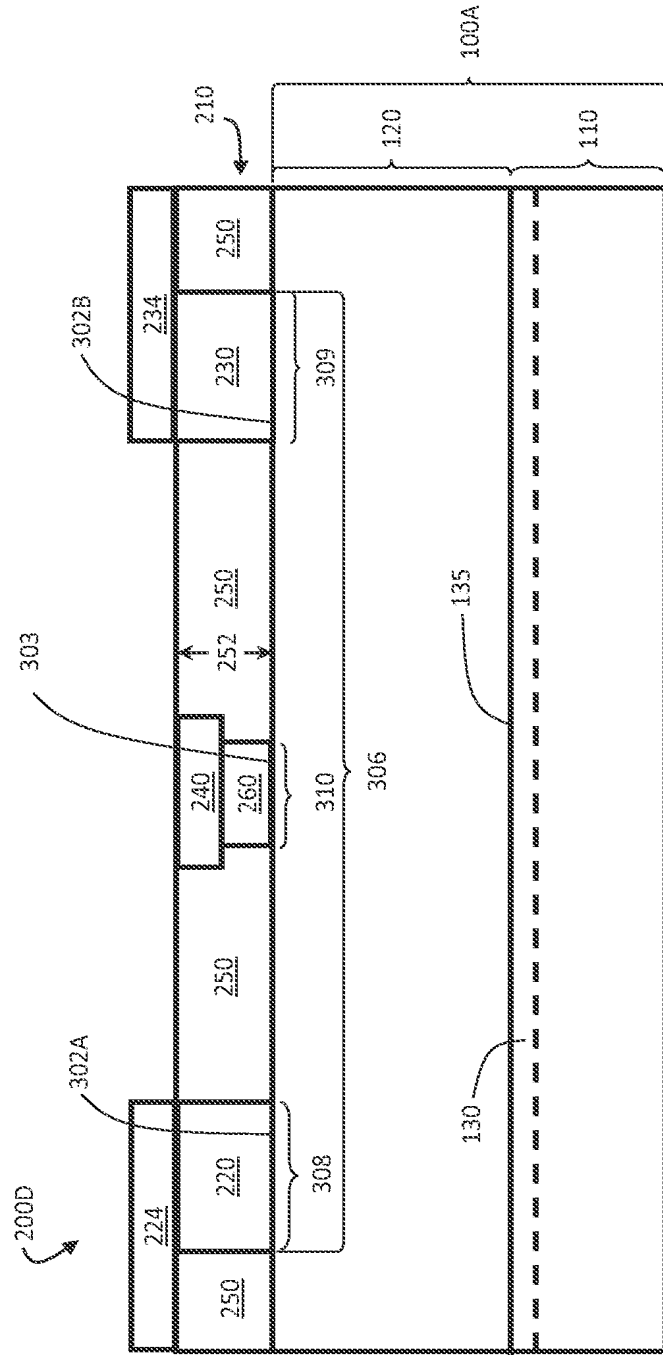


FIG. 2C

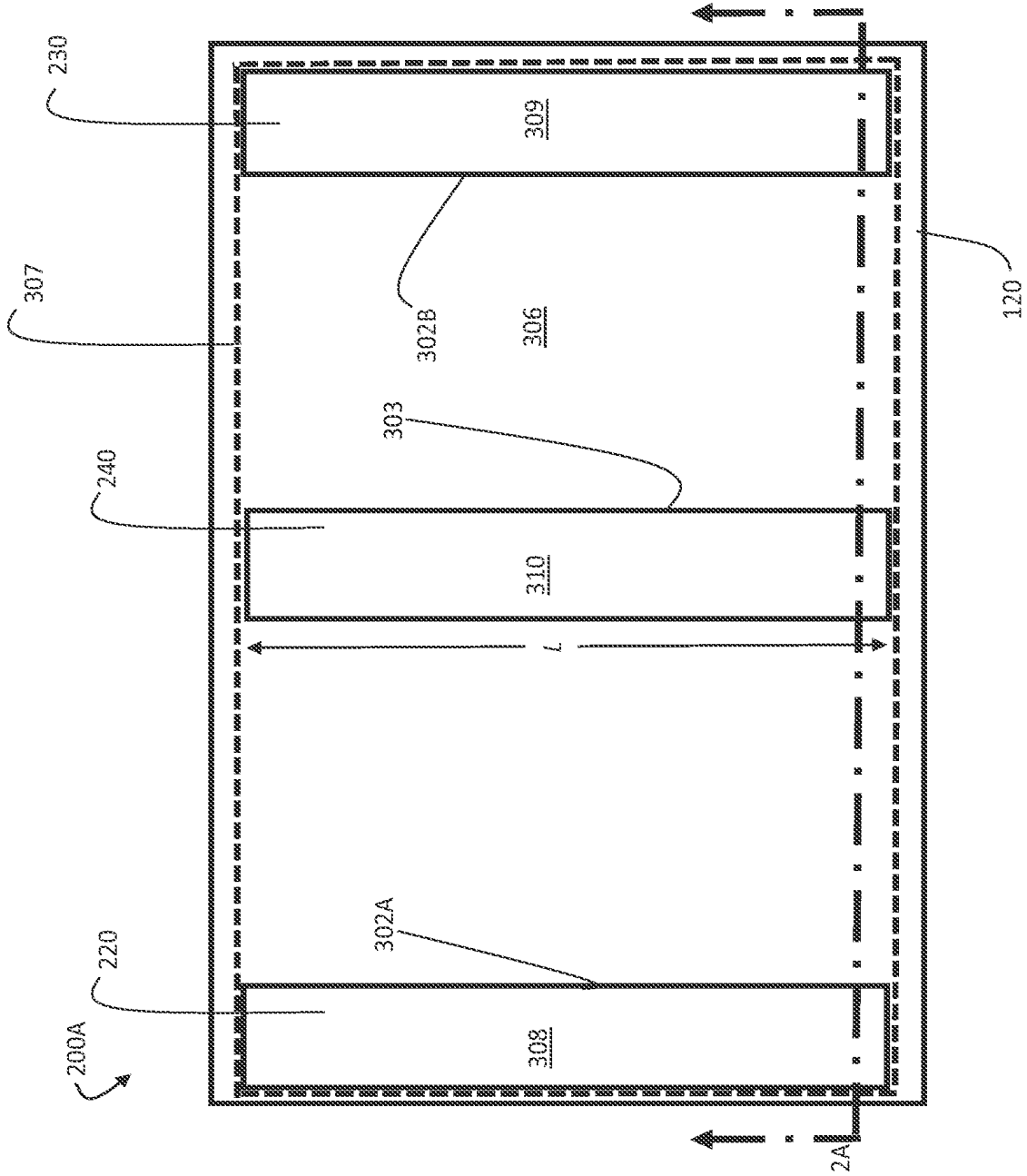


FIG. 2D

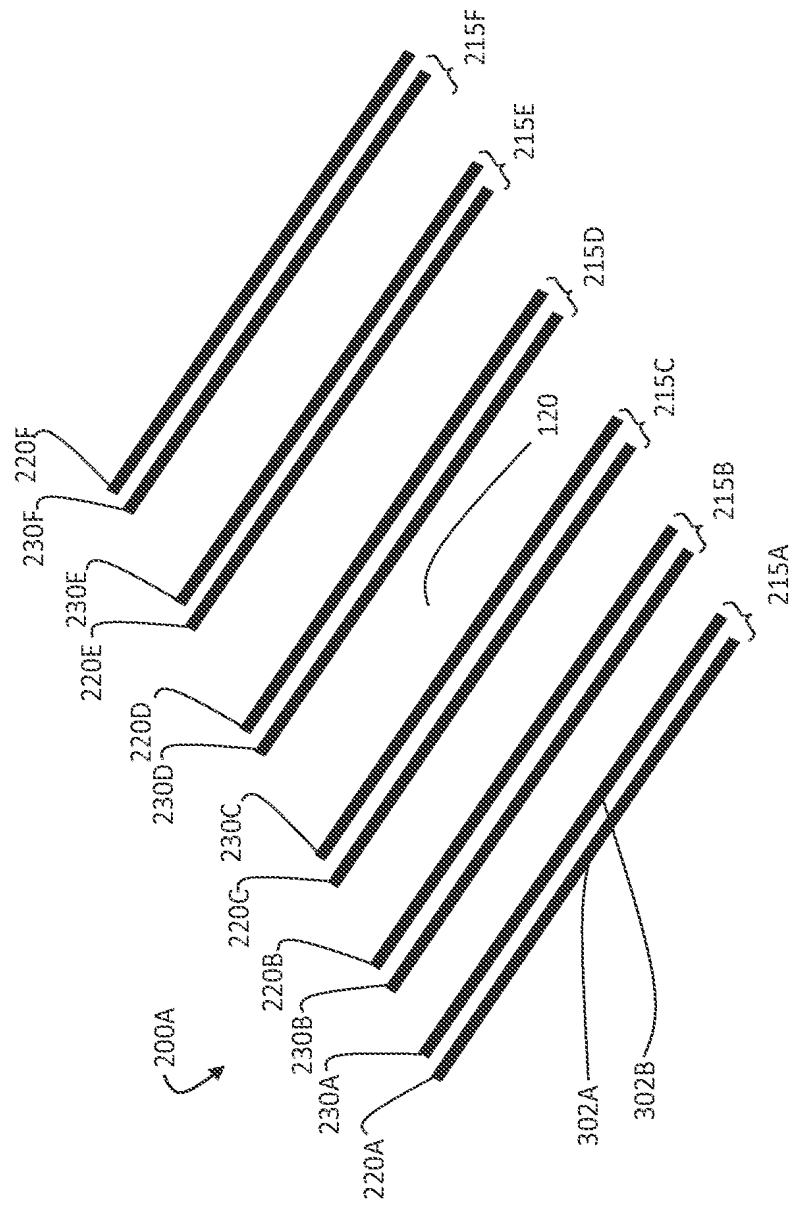


FIG. 3A

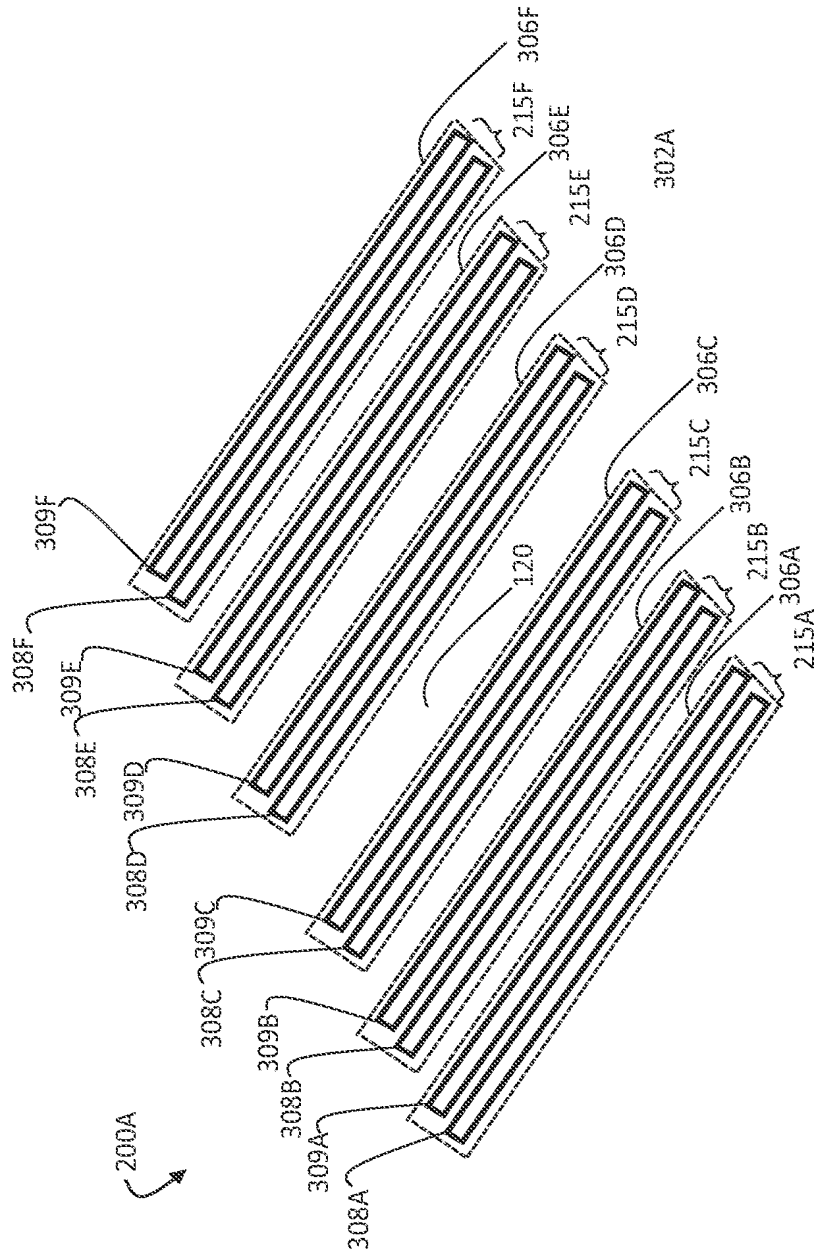


FIG. 3B

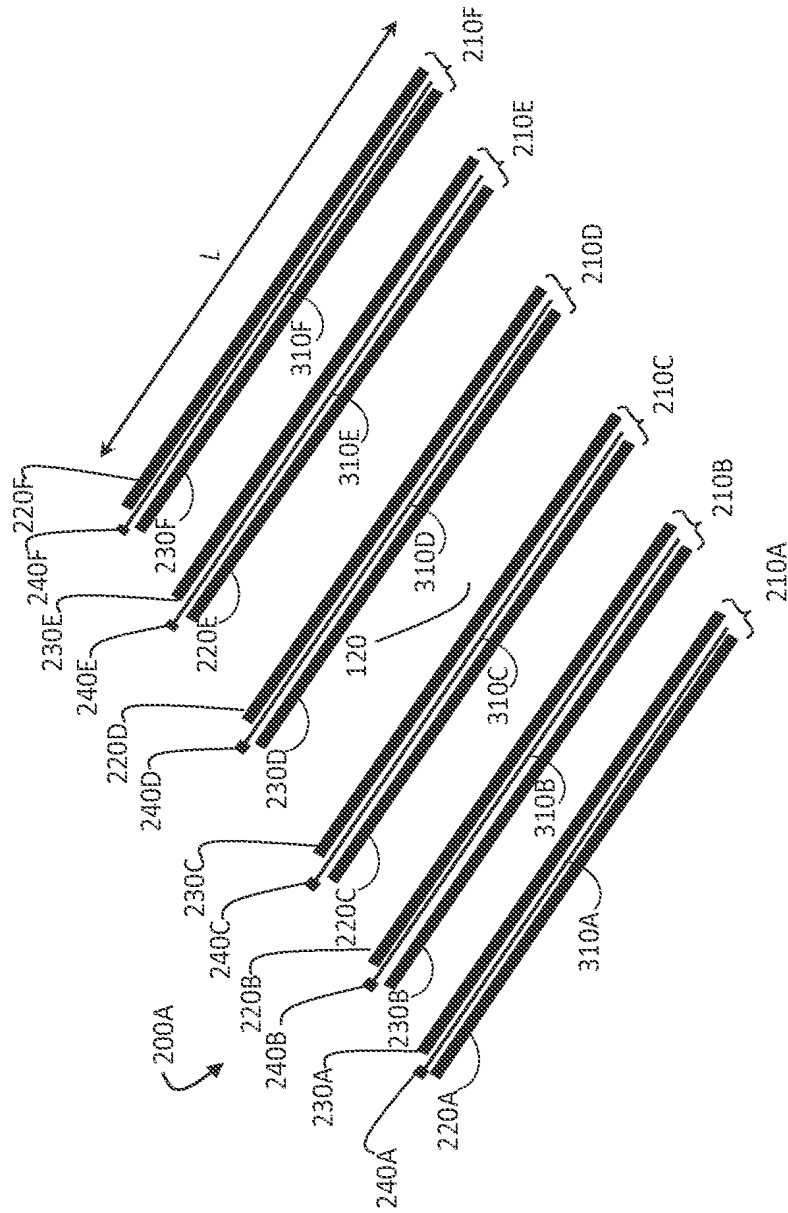


FIG. 3C

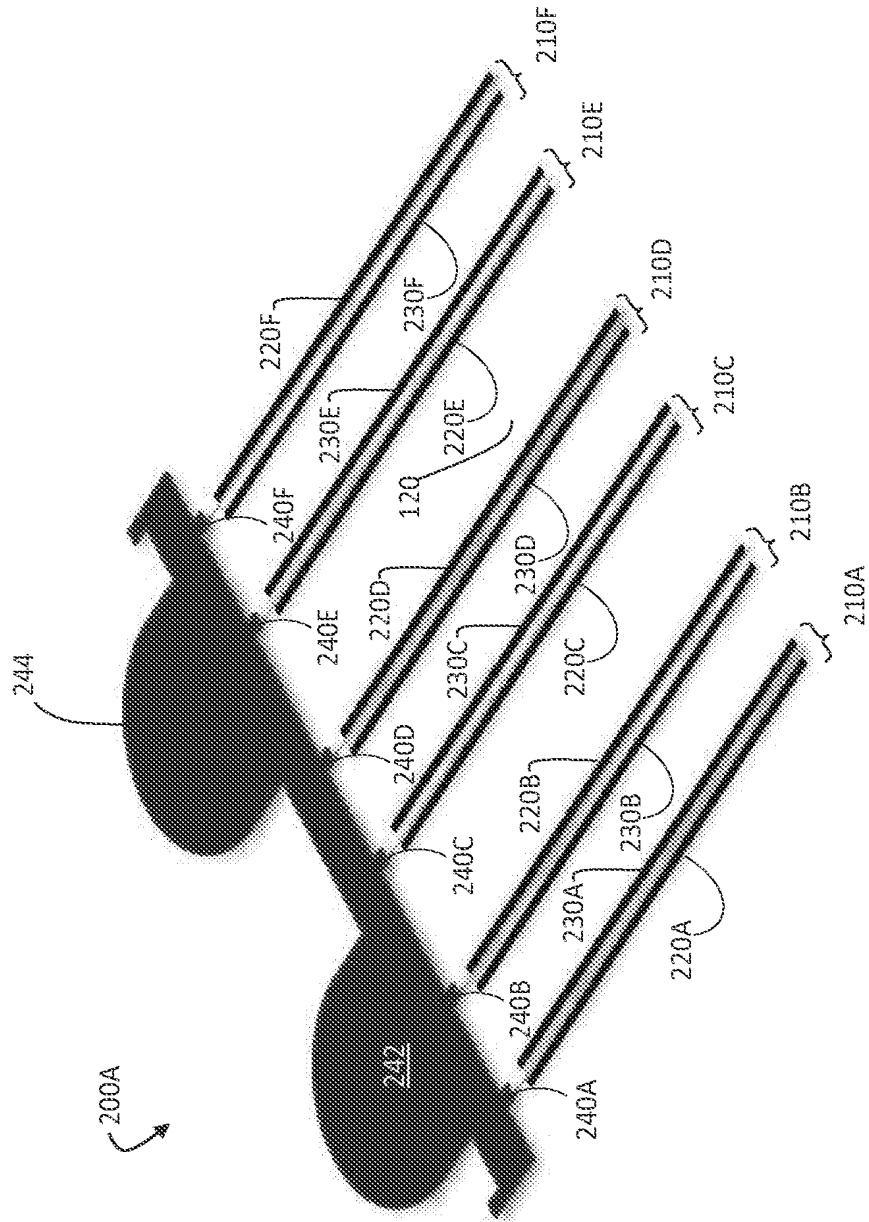


FIG. 3D

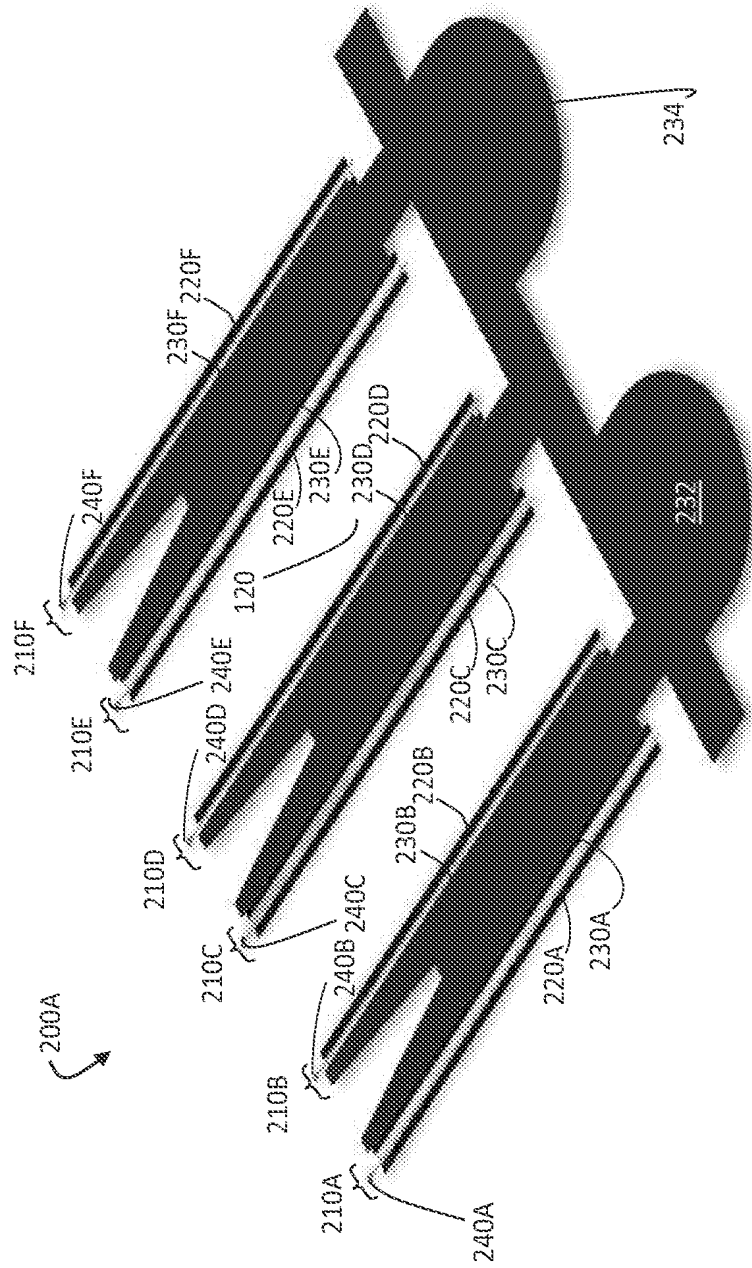


FIG. 3E

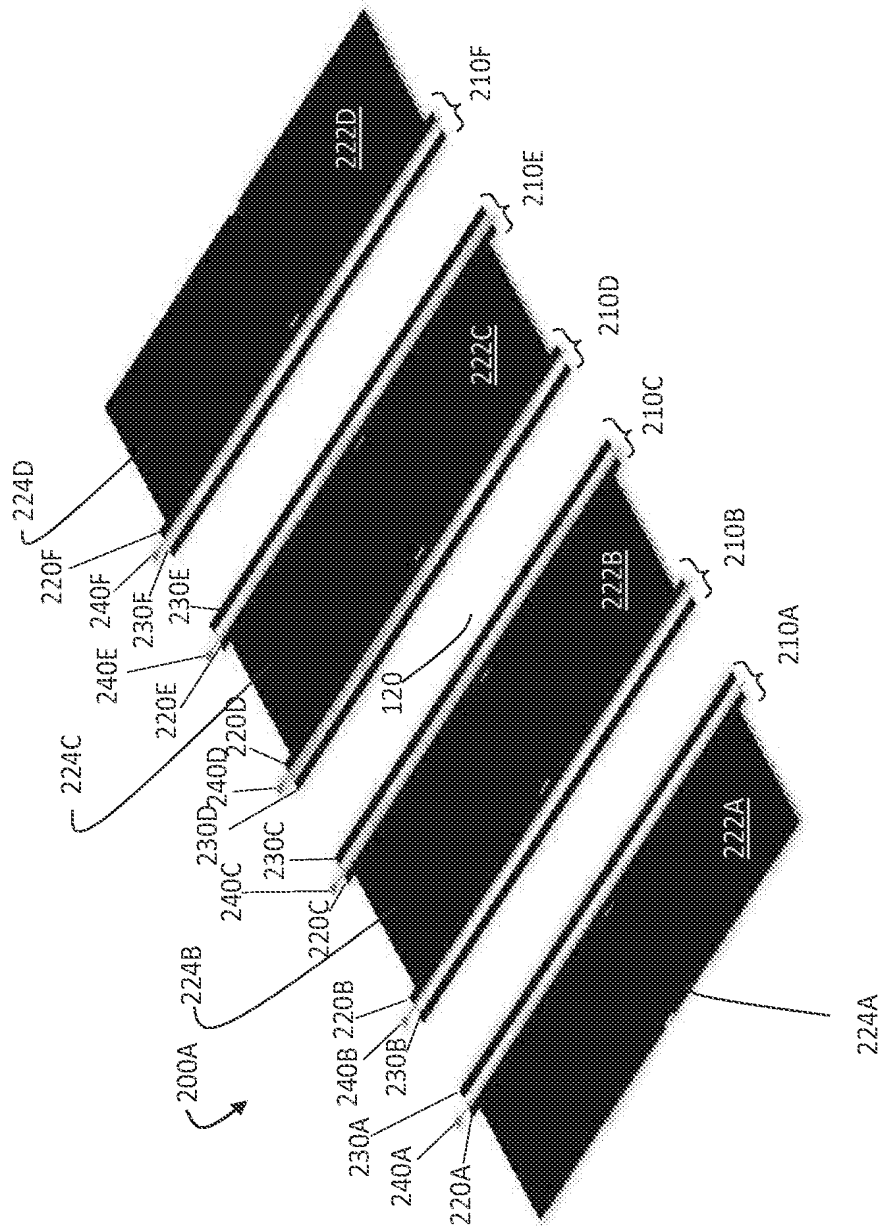


FIG. 3F



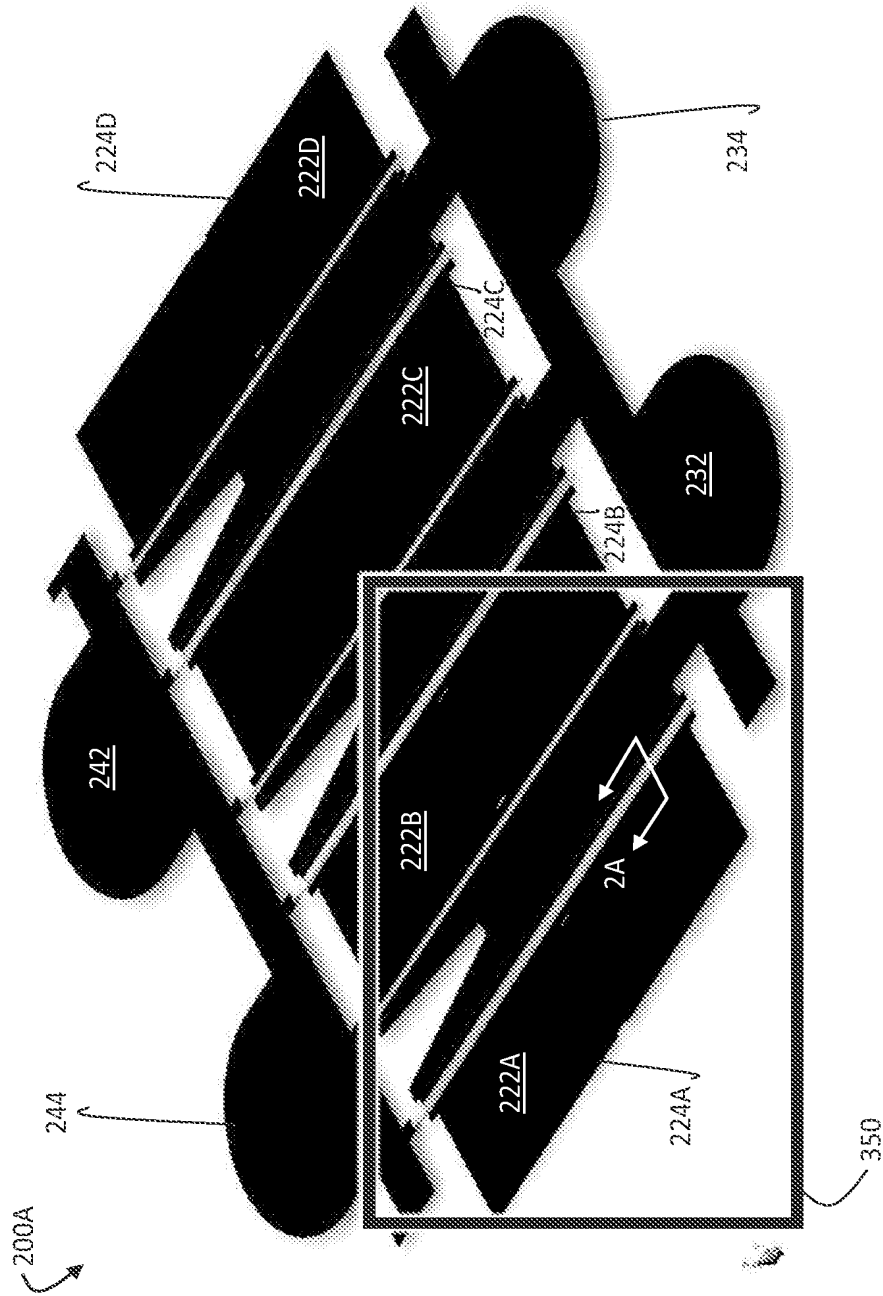


FIG. 3G

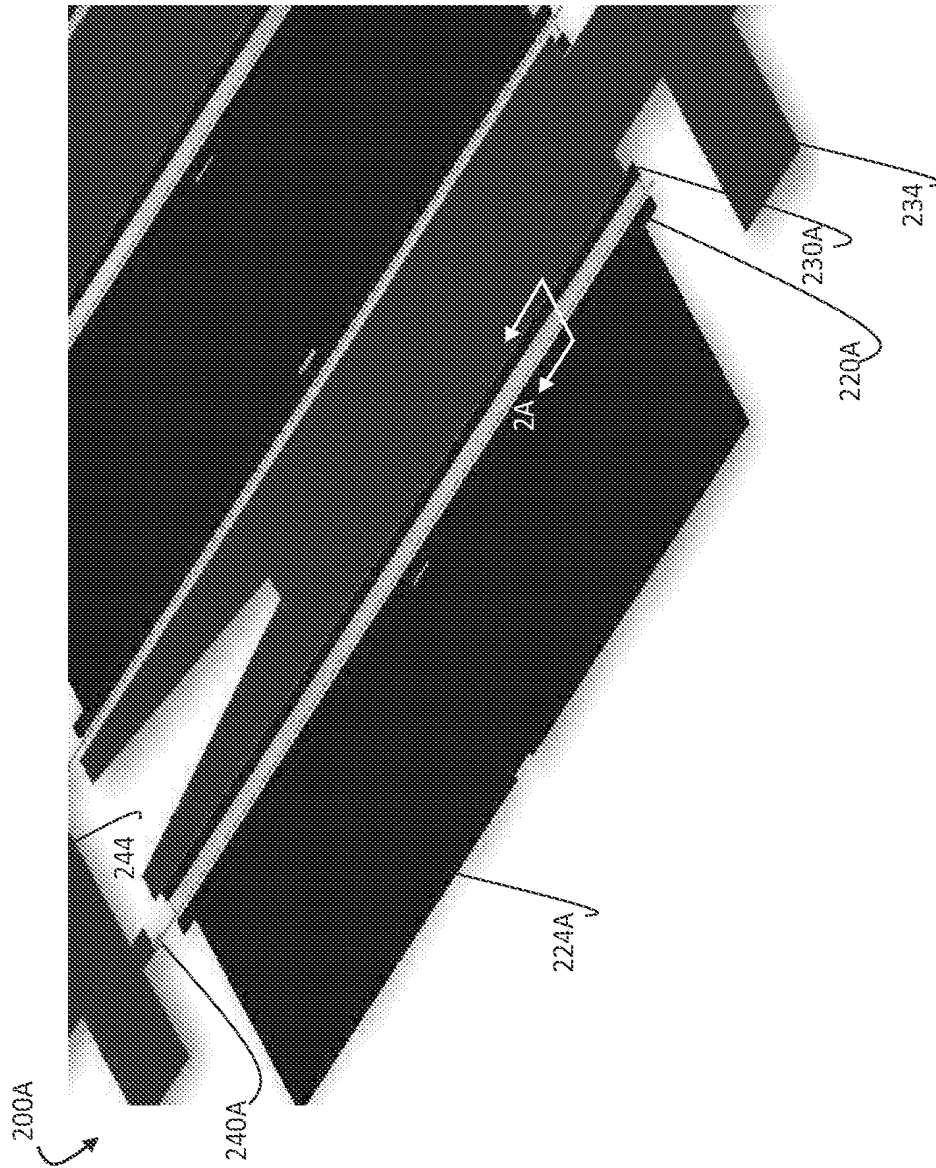


FIG. 3H

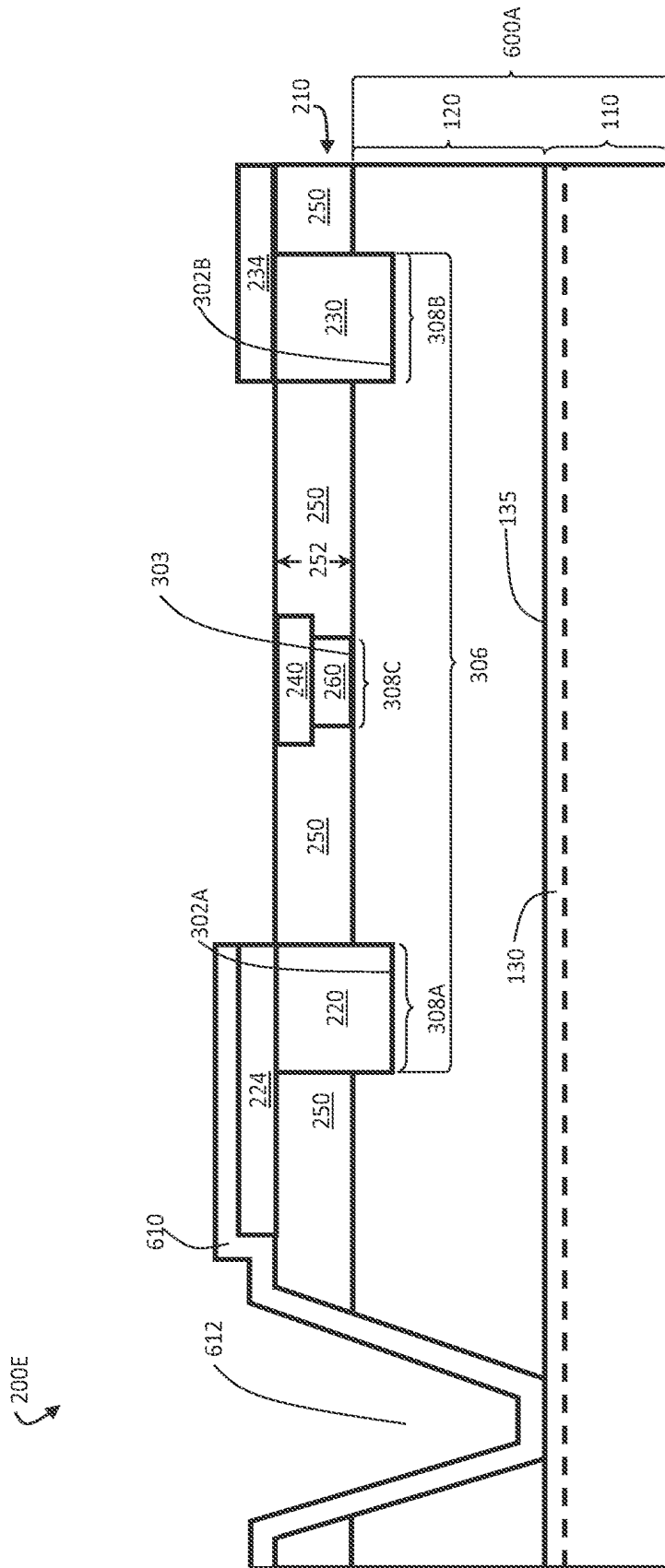


FIG. 4

PAE Versus Chuck Temperature (F=2.5GHz)

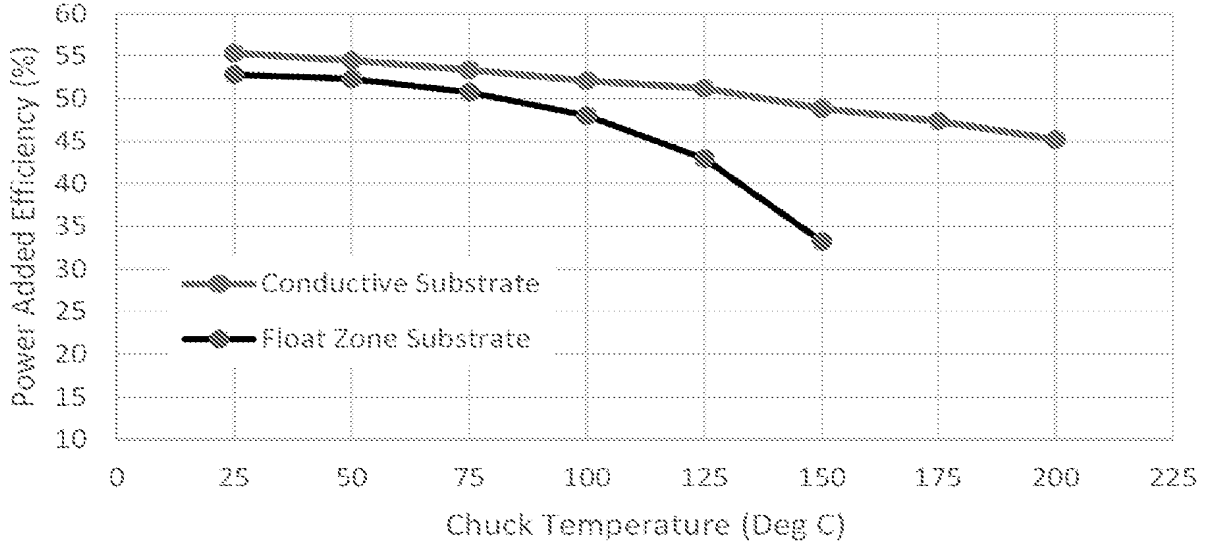


FIG. 5A

RF Pout (Vds=30v) Versus Chuck Temperature (F=2.5GHz)

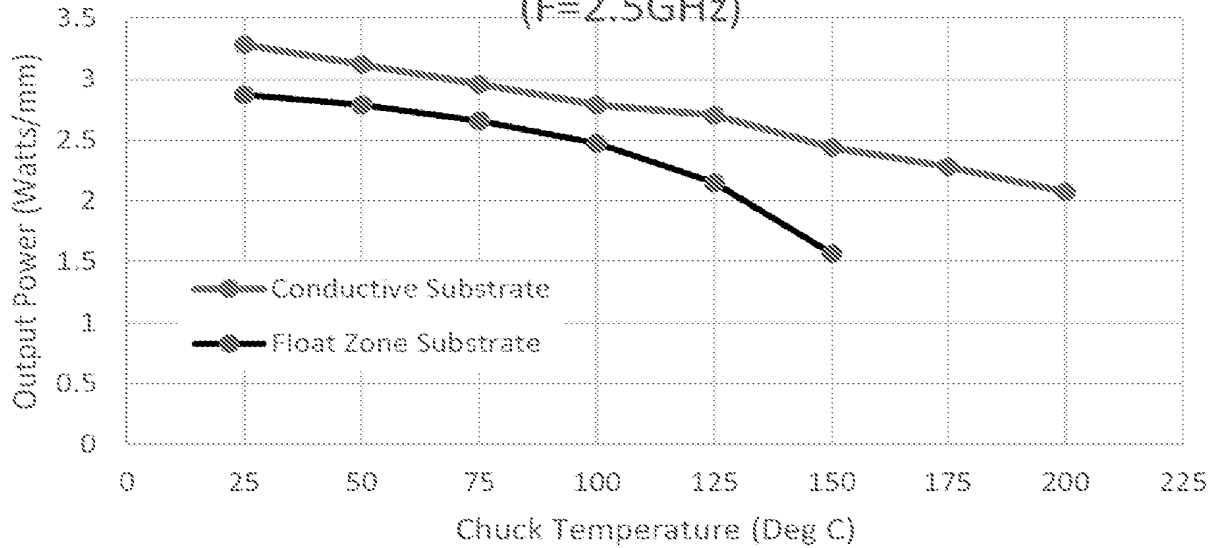


FIG. 5B

Si Substrate Pdiss Due to RF vs Bulk Resistivity

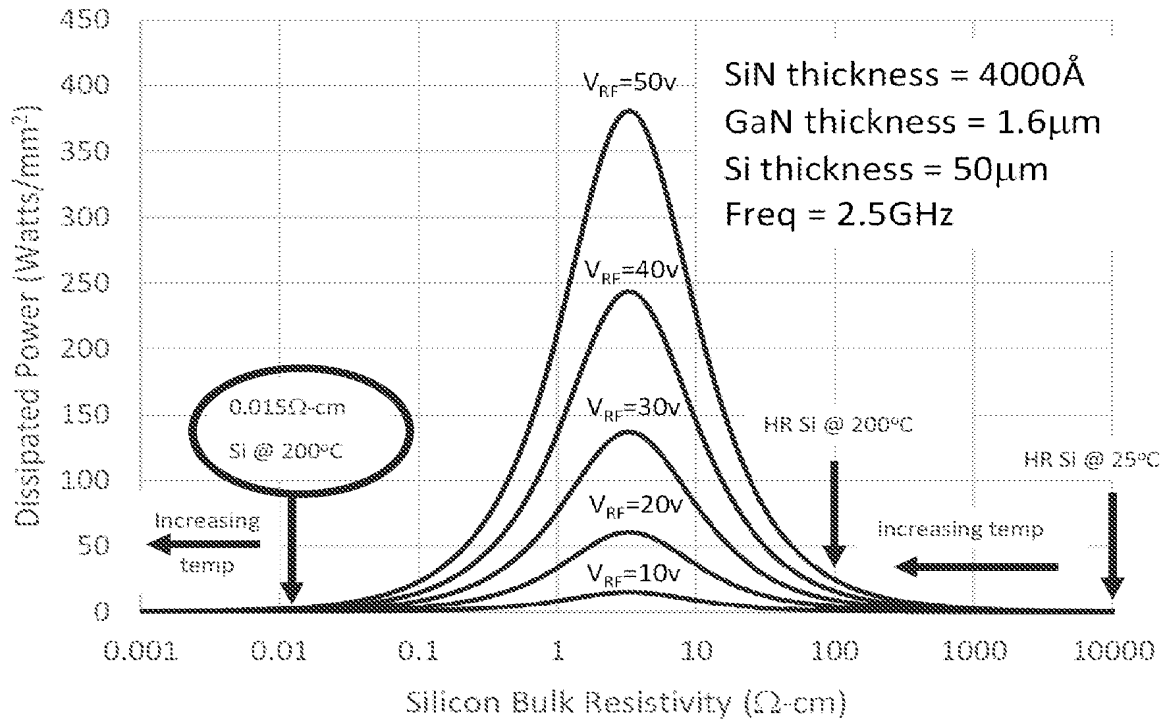
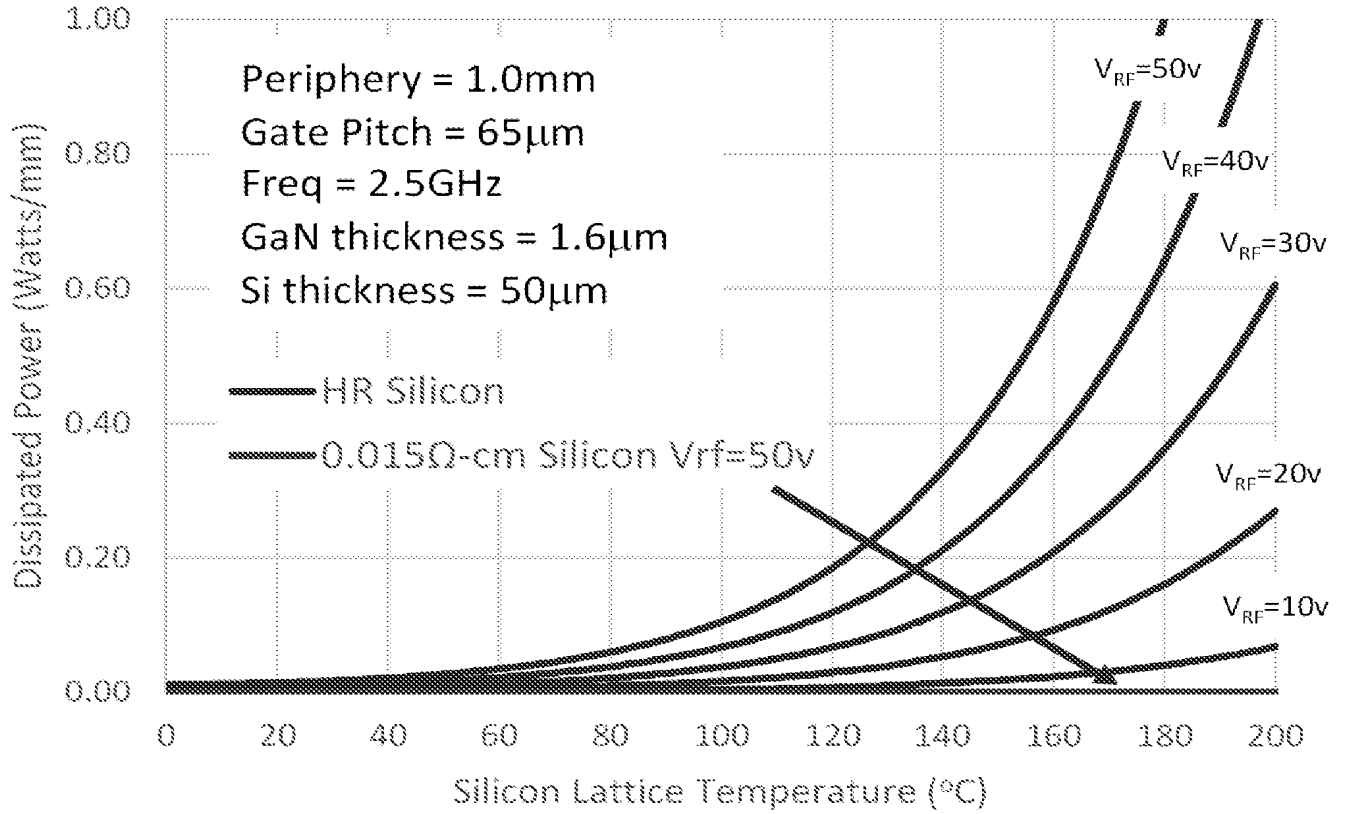


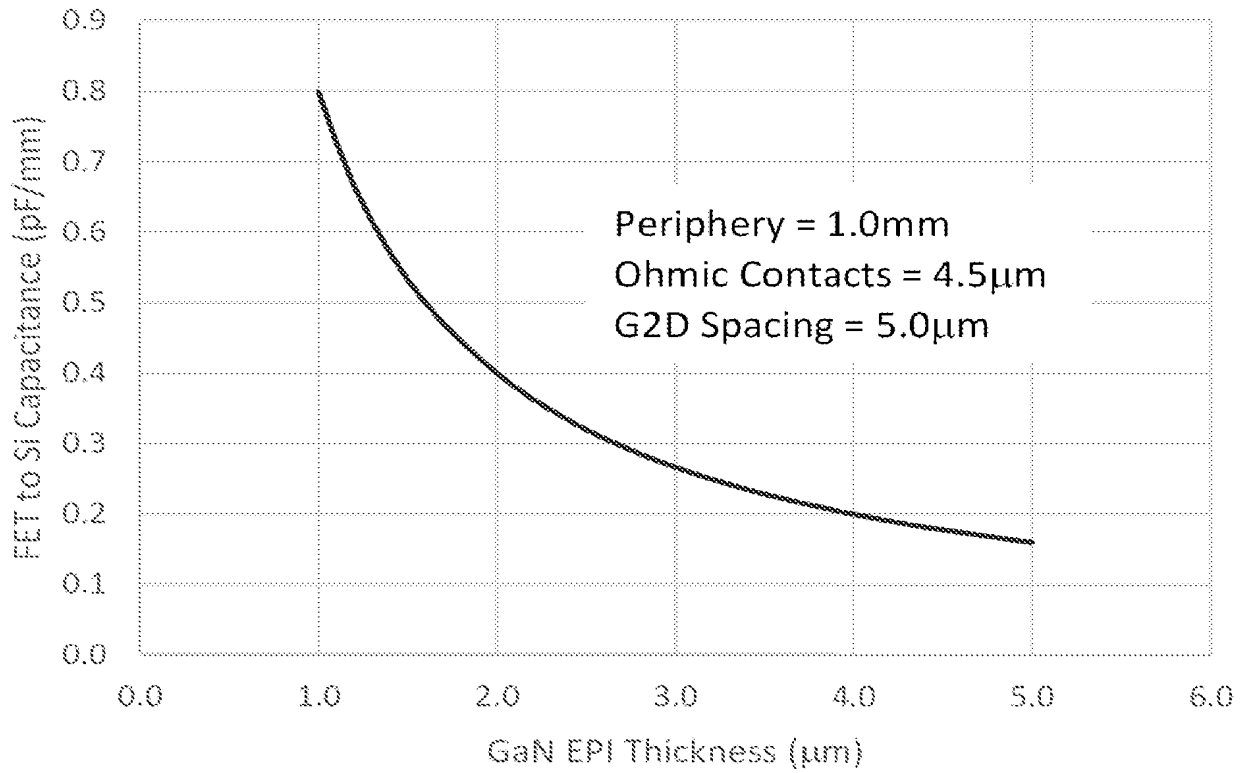
FIG. 6

### Si Substrate P<sub>diss</sub> Due to RF vs Lattice Temp



**FIG. 7**

### FET to Silicon Capacitance vs GaN Thickness



**FIG. 8**

INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2019/042623

A. CLASSIFICATION OF SUBJECT MATTER  
 INV. H01L29/778 H01L29/872 H01L29/417  
 ADD. H01L29/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
 EPO-Internal, WPI Data, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	TAKENAKA ISAO ET AL: "High-Efficiency and High-Power Microwave Amplifier Using GaN-on-Si FET With Improved High-Temperature Operation Characteristics", IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, PLENUM, USA, vol. 62, no. 3, March 2014 (2014-03), pages 502-512, XP011541890, ISSN: 0018-9480, DOI: 10.1109/TMTT.2014.2298381 [retrieved on 2014-03-03] abstract figures 8, 9, 12 and associated text ----- -/--	1,3,4, 6-18

Further documents are listed in the continuation of Box C.  See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance  
 "E" earlier application or patent but published on or after the international filing date  
 "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)  
 "O" document referring to an oral disclosure, use, exhibition or other means  
 "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention  
 "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone  
 "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art  
 "&" document member of the same patent family

Date of the actual completion of the international search  18 October 2019	Date of mailing of the international search report  31/10/2019
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer  Moehl, Sebastian
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## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2019/042623

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SAITO W ET AL: "Breakdown behaviour of high-voltage GaN-HEMTs", MICROELECTRONICS AND RELIABILITY, vol. 55, no. 9, 10 July 2015 (2015-07-10), pages 1682-1686, XP029294642, ISSN: 0026-2714, DOI: 10.1016/J.MICROREL.2015.06.126 figure 1 and associated text -----	1,3,4, 6-18
X	JP 2017 216257 A (SHARP KK) 7 December 2017 (2017-12-07) figure 1 paragraph [0038] -----	1,3,4, 6-18
X	US 2008/023706 A1 (SAITO YASUNOBU [JP] ET AL) 31 January 2008 (2008-01-31) figure 1 and associated text -----	1,3,4, 6-18

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2019/042623

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2017216257 A	07-12-2017	JP 2017216257 A	07-12-2017
		WO 2016059923 A1	21-04-2016
-----			
US 2008023706 A1	31-01-2008	JP 2008034411 A	14-02-2008
		US 2008023706 A1	31-01-2008
-----			

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US2019/042623

## Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.: 2, 5, 19-293  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:  
see FURTHER INFORMATION sheet PCT/ISA/210
  
3.  Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

## Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
  
2.  As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
  
3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

### Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

Continuation of Box II.2

Claims Nos.: 2, 5, 19-293

The present application contains 293 claims, of which 24 are independent. There is no clear distinction between the independent claims because of overlapping scope. There are so many claims, and they are drafted in such a way that the claims as a whole are not in compliance with the provisions of clarity and conciseness of Article 6 PCT, as it is particularly burdensome for a skilled person to establish the subject-matter for which protection is sought.

In particular, the following major points of non-compliance have been noted (note that this is a non-exhaustive list):

1 Lack of support:

It

is clear from page 2 lines 3-17 of the description that the problem addressed by the present application is to reduce the amount of resistive heating during operation of III-nitride-based devices, and that the key feature used in the present application to solve this problem is an electrically conductive substrate. An electrically conductive substrate as such is evidently not specific, well-known by the skilled person and in general not necessarily suitable for the formation of nitride-based devices thereon. In lines 21-24, the description therefore clarifies that the key feature of the present application is a substrate, at least a portion of which is made of bulk silicon having an electronic resistivity of less than 0.10  $\Omega$ -cm when the silicon is at 25 °C. Since this feature is indeed both suitable for the formation of a III-nitride-based device and for solving the above-mentioned problem, this feature is taken as (most) essential feature of the present invention. Since this feature is not claimed in any one of claims 19-91 and 186-199, said claims are not supported by the description as required by Article 6 PCT, as their scope is broader than justified by the description.

2 Lack of conciseness:

2.1 Independent claims 2, 92, 106, 120, 133, 146, 160, 173, 200, 214, 228, 242, 255, 268, 281 repeat in essence all features of claim 1.

2.2 The wording of independent claims 186, 200, 214, 228, 242, 255, 268, 281 is identical to that of one of the preceding independent claims, respectively.

3 Lack of clarity:

3.1 Independent claims 2, 36, 50, 146, 160, 173, 228, 255, 281 attempt to define the subject-matter in terms of the result to be achieved, which merely amounts to a statement of the underlying problem, without providing the technical features necessary for achieving this result. Moreover, at least in claim 36, the result to be achieved itself is unclear since the "ratio" is not defined.

3.2 In claims 92, 106, 120, 133, 146, 160, 173, 200, 214, 228, 242, 255, 268, 281, it is not clear if the "gate or anode" having a "peripheral length" is in the "device", in the "integrated circuit component", in the "structure", or in none of these features. Since these claims cover even gates or anodes

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

of any other structure, the defined ratios do actually not seem to impose any additional limitation on the claimed subject-matter. Moreover, in claims 120 and 242, it is not clear the peripheral length of which entity (electrode, pad, the combination of both) is actually meant.

3.3

In claim 2 it is not clear if the "integrated circuit component" is comprised in the claimed subject-matter or not: according to the wording "semiconductor structure for an integrated circuit component" it would not whereas according to the wording "wherein the integrated circuit component ..." it would.

3.4 The additional feature of claim 5 is fundamentally inconsistent in itself since a component is either "integrated", or "discrete", but not both.

The non-compliance with the substantive provisions is to such an extent, that the search was performed taking into consideration the non-compliance in determining the extent of the search (PCT Guidelines 9.19 and 9.25).

The search was based on the subject-matter that, as far as can be understood, could reasonably be expected to be claimed later in the procedure, and the corresponding claims, namely claim 1 and its dependent claims 3, 4 and 6-18. Indeed, claim 1 comprises all features being essential for the definition of the present invention (which can be identified in page 2 lines 3-24, as explained in above item 1), and no other features, so as to have a scope narrow enough to allow for a meaningful search, and broad enough to be representative for the disclosure of the present application.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guidelines C-IV, 7.2), should the problems which led to the Article 17(2) declaration be overcome.