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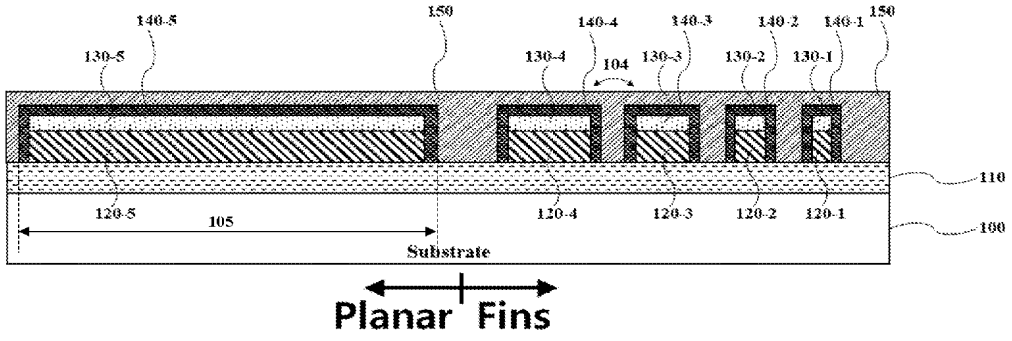
(54) **Title:** INSTRINSCALLY TUNABLE AND ULTRA-LINEAR MULTI-FIN MIS HEMT DEVICES

Figure 1A



(57) **Abstract:** Devices and methods of the invention use a plurality of Fin structures and or combine a planar portion with Fin structures to compensate for the first derivative of transconductance, gm. In preferred methods and devices, Fins have a plurality of widths and are selected to lead to the separate turn-on voltage thresholds for the largest, intermediate and smallest widths of the MIS HEMT fins to flatten the transconductance gm curve over an operational range of gate source voltage.

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INSTRINSCALLY TUNABLE AND ULTRA-LINEAR MULTI-FIN MIS HEMT DEVICES

PRIORITY CLAIM AND REFERENCE TO RELATED APPLICATION

[001] The application claims priority under 35 U.S.C. §119 and from all applicable statutes and treaties from prior provisional application serial number 62/579,677 which was filed October 31, 2017.

FIELD

[002] A field of the invention is semiconductor devices and semiconductor device fabrication. The invention particular concerns metal insulator semiconductor high electron mobility transistor (MIS-HEMT) devices.

BACKGROUND

[003] All known transistor technologies are intrinsically non-linear. This non-linearity leads to signal distortion and power loss. Non-linearity is embodied in a decrease of the transistor current gain cut-off frequency, f_T, and maximum oscillation frequency, f_{max}, with an increase in the drain current. Both f_T and f_{max} are directly proportional to the transistor's transconductance, g_m, which degrades at high drain currents. g_m degradation is material dependent, and is caused by (1)

mobility degradation due to interface roughness in Si devices; (2) real-space transfer of hot electrons into the barrier in GaAs and InGaAs based HEMTs; (3) self-heating effects, (4) scattering with nonequilibrium hot optical phonons, (5) emission of optical phonons, and (6) increase of the dynamic source access resistance in GaN based HEMTs. See, Palacios, T., Rajan, S., Chakraborty, A., Heikman, S., Keller, S., DenBaars, S. P., Mishra, U. K., "Influence of the dynamic access resistance in the g_m and f_T linearity of AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices* **2005**, 52 (10), 2117-2123. In GaN devices, it has been argued that the measured saturation velocities, the current, and g_m, are well below the theoretical limits. Recent results have shown that there is an unharnessed opportunity to dramatically improve linearity in GaN based devices

[004] Common circuit linearization techniques can inspire device layouts that enable intrinsically tunable ultra-wide band linear devices. The pioneering work of Barrie Gilbert in the late sixties and seventies outlined the use of differential pairs to obtain wideband linearity amplifiers. Gilbert, B., "A new wide-band amplifier technique," *IEEE Journal of Solid-State Circuits* **1968**, 3 (4), 353-365. The approach became known as the multi-tanh principle in which an offset voltage, V_j, at the base of an element of the differential pair leads to the summation of the tail current of each stage which turns on sequentially. The transconductance becomes a sech function which is flat as a function of input voltage. In practical circuits, the offset voltage is generally of the order of V_T in order to reduce the overall noise, and the wideband linearity cannot be sustained over a large input power without substantial increase of the amplifier's area.

[005] In MOSFETs, the derivative superposition technique [Webster, D., Haigh, D., Scott, J., Parker, A., Derivative superposition-a linearisation technique for ultra broadband systems. **1996**] and its variations [Kim, T. W., Kim, B., Lee, K., "Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors,"

IEEE Journal of Solid-State Circuits **2004**, 39 (1), 223-229] including the modified derivative superposition technique [Aparin, V., Larson, L. E., Modified derivative superposition method for linearizing FET low-noise amplifiers. *IEEE Transactions on Microwave Theory and Techniques* **2005**, 53 (2), 571-581] has been heavily utilized for linearizing RF circuits. It extends the V_{GS} bias range through the use of two or more parallel MOSFETs with different widths and gate biases. Similar to the multi-tanh approach, this technique is extrinsic, is costly for layout area, and cannot be extended to mm wave frequencies due to circuit patristics and bandwidth limitations of the impedance matching elements.

[006] Over the years, various approaches for enhancing the intrinsic linearity of transistors have been proposed. In 1992, D. R. Green of AT&T Bell Laboratories proposed FETs of multiple quantum well channels with different widths, depths, and carrier concentrations that have different threshold voltages. [Green, D. R., U.S. Patent 7852369, Method of making substantially linear field-effect transistor] The design predicts that different channels in different layers underneath the gate can turn on at different gate biases thereby leading to a g_m linearity. Alternative variations of this idea have been proposed for HMETs and even in vertically stacked Si nanowire channels with double or all-around gates. Practically, this concept is hard to implement because of the limited control over the threshold voltage shifts while maintaining adequate current that will synthesize to a linear device. Additionally, screening of 2D charge density at the topmost channel reduces the gate modulation efficiency to the underlying channels and control over charge carrier density in these channels. Furthermore, gate leakage currents are expected to kick in before other channels can be reliably turned on.

[007] Palacios WO2018/119037 discloses high-linearity transistors. Two gate controlled regions have different threshold voltages. FIG 7A shows a nanowire or fin configuration with varying widths. The fins are arranged according to the

magnitudes of the peaks and/or valleys or g”m, which is the second derivative of transconductance. This is known as the derivative superposition technique, previously used widely in communication circuits.

SUMMARY OF THE INVENTION

[008] A preferred MIS-HEMT includes a substrate, a buffer layer upon the substrate, and a plurality of multi-layer fins with channel and barrier material. The fins have a plurality of widths and are formed upon the buffer layer, gate insulator surrounds the fins and gate metal conformally covers the gate metal. The plurality of widths include largest, intermediate and smallest widths, selected to lead to the separate turn-on voltage thresholds for the largest, intermediate and smallest widths of the MIS-HEMT fins to flatten the transconductance g_m curve over an operational range of gate source voltage. Preferably, the planar channel comprises a width greater than 1 μm, and all of the plurality of widths are less than 500 nm. Preferably, the plurality of widths are selected such that the threshold voltages (V_T) and the peak point of transconductance g_m of single Fins from the plurality of Fins lift up a decreasing region of transconductance g_m at higher V_{GS} in larger Fins of the plurality of fins. The source and drain regions are preferably unetched. The channel and barrier materials can be Group III-V materials or silicon with different ion-implant doses. Preferably, the plurality of widths are uniformly separated by gate voltages in second derivative of transconductance g_m" curves to complement each other for reducing the first derivative of transconductance g_m' close to zero over the operational range.

[009] A preferred method of compensating for the first derivative of transconductance, $g_{m.}$, in a MIS-HEMT includes turning on a first Fin in response to a first gate source voltage. A second smaller Fin turns on in response to an increased gate voltage. A third Fin smaller than the second smaller Fin turns on in

response to a larger increased gate voltage, wherein the first, second smaller, and third Fin are sized such that smaller fin devices with quantitatively calculated weights replenish the negative region of the first derivative of transconductance g_m to reduce variation of g_m over an operational range of gate source voltage. The method preferably includes first turning on a planar channel in response to a gate source voltage that is smaller than the first gate source voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIGs. 1A-1C are respective fragmentary cross-sectional, side perspective and top views schematically showing a preferred architecture of combined planar and multi-fin MIS-HEMTs according to the present invention;

[0011] Figures 2A and 2B are schematic diagrams of a single Fin showing a threshold voltage calculation method for a preferred Fin MIS-HEMT according to the present invention.

[0012] Figures 3A and 3B are graphical views showing transistor linearization by the multi-Fin MIS-HEMTs according to the present invention;

[0013] Figure 4 is the process flow for a preferred fabrication method according to the present invention;

[0014] Figure 5 shows Silvaco Atlas simulations for the electron density in the cross-section of a planar strip (1μm wide) and different Fin widths

[0015] Figure 6: Line cut of carrier concentration 1nm below AlGaN barrier for planar and Fin structures

[0016] Figures 7A-7F illustrates measured characteristics of a conventional planar device (Figures 7A, 7C, and 7E) and the linearization provided by the invention (Figures 7B, 7D, and 7F)

[0017] Figure 8 are g''_m-V_G characteristics of experimental fabricated devices with a planar and different fin widths;

[0018] Figure 9 are g'_m-V_G characteristics of fabricated devices with a planar and different fin widths and synthesized devices with reduced Δg_m;

[0019] Figure 10 includes data showing an effect of factor F on Δg_m;

[0020] Figure 11 is plot of the number of transistors at each threshold voltage;

[0021] Figure 12 is a top-view SEM image of a fabricated multi-fin MIS-HEMT device;

[0022] Figures 13A – 13D are data plots of device characteristics of a preferred embodiment multi-fin MIS-HEMT; and

[0023] Figure 14 includes a summary of g_m' at different V_G, illustrations present methods of linearization of g_m, and defining weights;

[0024] FIGs. 15A-15C are respective fragmentary cross-sectional, side perspective and top views schematically showing a preferred architecture of a multi-fin MIS-HEMT according to the present invention;

[0025] FIGs. 16A-16C are respective fragmentary cross-sectional, side perspective and top views schematically showing a planar MIS-HEMT that is combined with multi-fin FETs according to the present invention; and

[0026] Figure 17 is data plot of threshold voltages (V_T) as a function of fin widths (W_{Fin}).

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] A preferred transistor device architecture provides a capability of intrinsically tunable ultra-wide band linearity. Preferred embodiments overcome limitations of the prior approaches in the background by providing devices that permit tuning of the threshold voltage and synthesizing the linearity of transistors using parallel channels that are formed on the surface of the substrate with consistent and controllable gate-to-channel capacitance, and that provide a larger degree of flexibility in material selection such as low work function metal electrodes to push

the linearity to voltages that conventional HEMT-based devices cannot achieve. Preferred devices use a plurality of Fin structures and/or combine a planar portion with Fin structures to compensate for the first derivative of transconductance, g_m. .

[0028] Preferred devices enable linearization with a planar channel and multiple Fin channels whose threshold voltage can be individually tuned by width of the Fin-channel, W_{Fin}. For a preferred planar and multi-Fin device, one can write: $I(V_{GS}) = \alpha_1 I_1(V_{GS}-V_{T1}) + \alpha_2 I_2(V_{GS}-V_{T2}) + \cdots + \alpha_n I_n(V_{GS}-V_{Tn})$, and $g_m(V_{GS}) = \alpha_1 g_{m1}(V_{GS}-V_{T1}) + \alpha_2 g_{m2}(V_{GS}-V_{T2}) + \cdots + \alpha_n g_{mn}(V_{GS}-V_{Tn})$, where α_n is the number of channels for a family of Fins, n, with width W_{Fin-n}, and threshold voltage, V_{Tn}, where $V_{Tn} > V_{Tn-1}$. Therefore, two simple "engineering knobs" are present in the current device architecture to control the device linearity: W_{Fin} which controls the shift in the threshold voltage, V_T, and the amplitude α_n which controls the current output beyond a V_T point. A planar channel device having a more negative V_T than any fin devices broadens the flat g_m region much further meaning a more intrinsically linear transistor. As can be seen in Figure 9, g_m' of planar device is negative after V_G of -4 V, which provides a room that can be replenished by fin devices with higher V_T, to make a preferred device have a very broad flat g_m region.

[0029] While some prior approaches have sought to use Fin HEMT devices to reduce the source access resistance and enhance the linearity, such approaches do not provide linearity that is accessible at gate voltages beyond those at which the gate Schottky diode turns on (~2 V). In contrast, preferred combined planar and Fin MIS-HEMT devices permit flexible engineering of the device threshold voltage and attaining linearity over a wider V_{GS} range.

[0030] Preferred embodiments achieve an objective of intrinsically tunable high linearity GaN multi-Fin MIS-HEMT devices that can deliver wideband linearity at low DC bias with potential to exceed OIP3/PDC of 1000. The intrinsic device characteristics as a function of gate-source voltage in preferred embodiment devices

can be controllably synthesized in order to provide the desired linearity, along with high f_t, f_{max} and low noise performance. Preferred MIS Fin HEMTs provide linear transfer characteristics, through the synthesis of I_{DS} currents from Fin HEMTs that turn on sequentially from large to small and therefore eliminate the usually reduced slope of I_{DS} as a function of Vgs when Vgs increases beyond the 'linear regime'. In other words, the transconductance of the device usually decreases rapidly with gate voltages above VT, but preferred devices provide a flat transconductance which leads to a constant gain, large bandwidth, and lower jitter. Preferred HEMTs provide a large ΔV_{GS} over which the device is linear. The large range is dependent on the number of families of FinFETs that can be integrated into the device. There are also limitations on how much the threshold voltage can be tuned for a particular device that depend upon with (1) size and (2) metal work function. HEMTs of preferred embodiments can provide linearity over a large ΔV_{GS} up to 10 V, as indicated by simulations. A largest range reported in literature known to the inventors is half or less than half of the 10V range, e.g. only from about 4.5 to 5V, which can also be lower depending upon size and metal work function, and most ranges are far less than that in reported and commercial devices.

[0031] The invention has been demonstrated with reference to, but is not limited thereby to GaN material. GaN was selected to demonstrate the present device architecture because of its well-known superior physical properties of high electron mobility and saturation velocity, high sheet carrier density and high breakdown fields. These properties make GaN a preferred choice to meet the goals of high linearity and high-power mm wave devices when used with the present architecture. GaN material is also a preferred material choice for scalable and economical production of high linearity transmitters. The present HEMT device architecture can work for any amplifier material system, including GaAs, InP, InGaAs, InGaN and others. Other materials that are suitable also have 2-dimensional electron gas

(2DEG) at the interface between a barrier layer, and the side-gate effect will be the same for all this type of these heterostructures meaning that they will have the similar VT shift phenomena when the fin width is narrowed. Such transistor channel materials are remotely doped and there is less leverage on the threshold voltage control except for dramatic changes in the device gate capacitance, such as in FinFETs or nanowire FETs, to achieve tunable threshold voltages and therefore linear devices. The concept can also be applied to junction-less transistors including Si. Additionally, for Si, an adjustment of the threshold-voltage can be made by implanting the surface of the channel under the gate. As such, different ion-implant doses in parallel channels in a single Si device can achieve linear device characteristics but cannot offer the gain and speed of that for III-V materials.

[0032] Example embodiments will now be discussed to illustrate the invention. Artisans will appreciate broader aspects of the invention from the example embodiments.

[0033] Figures 1A-1C illustrate an example embodiment combined planar and multi-Fin MIS-HEMTs semiconductor device architecture in an example AlGaN/GaN material, which provides for intrinsically tunable ultra linear millimeter wave devices. The basic structure includes a substrate **100**, a buffer **110**, AlGaN/GaN multi-fin layers including a planar region **120-n**, **130-n** having fin to fin distances **104**, gate insulator **140-n** and gate metal **150**. In the example embodiment according to the present invention, the multi-Fin MIS-HEMT includes gate metal **150** and gate insulator **140-n**, e.g. Al_2O_3, HfO_2, etc., covering multiple AlGaN/GaN fins **130-n**, **120-n**, sitting on top of the GaN buffer layer **110** atop a substrate **100**, e.g. Si, SiC, sapphire, and GaN. The AlGaN/GaN fins **130-n**, **120-n** have a width of 40 nm - 1000 nm, and a height of 30 nm ~ 1 μm. Narrower fins can provide broader V_T range as long as making narrower fin is physically possible. Height should be higher than a barrier layer thickness, because gate metal should

cover the sidewall of 2DEG. The width of channel **105** can define the structure as a fin or a planar, and we define a planar MIS-HEMT when the width **105** is at least 1 μm, and preferably 1 μm to 100 μm, or a few hundred μm. We also define a fin MIS-HEMT when the width **105** is 500 nm or less, and preferably 40-500 nm. The width of planar region **105** can vary from one to few hundred micrometers depending on the actual device design with respect to a desired total drain current in circuit design. The number of fins with various widths can vary from one to thousands, and the fin edge-to-edge distance **104** can also vary from few nanometers to few microns depending on the actual device layout with respect to a targeted drain current density. Generally, smaller edge-to-edge distance **104** will lead higher current density, because 2DEG is not compromised in that region. As a practical matter, the limit on smallness of the edge-to-edge distance is fabrication related to the smallest distance that can be fabricated with a conformally deposited insulator and gate metal. Less than a nanometer distance is probably practical to fabricate, and more than few microns will be inefficient in terms of current density, because there will be no 2DEG at this region. The thickness of gate insulator **140-n** and AlGaN barrier layer **130** can also vary from few nanometers to few tens of nanometers. The thickness of gate insulator **140-n** and AlGaN barrier layer **130** can also vary from few nanometers to few tens of nano meters. Usually, around 5~10 nm of a barrier layer is optimal in terms of a 2DEG density and a gate capacitance. This can be optimized for particular designs. The gate insulator **140-n** and gate metal **150** covers the fins conformally for a fine control of the 2-dimensional electron gas channel as well as the electron channel at the metal-insulator-semiconductor interface. "Conformally" means that insulator and gate metal cover the sidewall and the top region without thickness changes or material property changes. The cross-sectional-view, side-view, and top-view schematics in Figures 1A-1C illustrate how the planar region and nano-fins **120-n, 130-n** are constructed

with gate insulators **140** and gate metals **150**, and connected to unetched AlGaN/GaN layers for the source **170** and drain region **180**, and ohmic metal **160, 190**. Unetched source 170 and drain 180 regions reduces access resistance for source and drain, resulting in a lower on-resistance and a lower DC power. No complex fabrication is required, instead patterns are created during fabrication that simply expose regions between fins (140) in Figure 1C. Fins having the same width will be turned on at the same gate bias, because V_T of them are the same. As the gate bias increases, the planar region will be turned first, and the family of Fins with larger width will turn on, then another family of Fins with narrower width will turn on sequentially, so that the current keeps on increasing linearly with gate bias, and therefore, the device becomes linear. In Figure 1B, conduction channels will be formed at the interface between 1) 130-n and 120-n, and 2) 140-n and 120-n. 2DEG will be formed at 130-n and 120-n, and the channel will be formed at 140-n and 120-n.

[0034] The analysis of threshold voltage in Fin structures is illustrated in Figures 2A and 2B. Figure 2A shows a single Fin. Accurate analytical equations were utilized, for the determination of parasitic capacitances in 3-dimensional CMOS device structures, to determine the capacitive coupling of the side Fin MOS structure **206**, **207** to the 2DEG charge density in the MIS-HEMT structure **205** and develop an intuitive model that captures the physics of threshold voltage shift in Fin MIS-HEMT devices. The side Fin structure consists of gate metal **201**, insulator **202**, and GaN channel layer **204**. On the other hand, the top MIS-HEMT structure consists of gate metal **201**, insulator **202**, AlGaN barrier layer **203**, and GaN channel layer **204**. For an Al_2O_3 gate dielectric, it is reasonable to assume for simplicity that the dielectric constant (ε) of Al_2O_3, AlGaN, and GaN, because of similar values of their permittivity; $\varepsilon_{Al_2O_3} \cong \varepsilon_{AlGaN} \cong \varepsilon_{GaN}$. The side-gates of the Fin structure induce a

shift in the charge density in the Fin channel, ΔQ_{side}, according to; $\Delta Q_{side} = C_{side} \cdot V_g$; $C_{side} = 2 \cdot C_{side1}$; $C_{side1} = L_G \cdot C_1 + C_2$, where,

C_1

$$= \begin{cases} \frac{2\varepsilon_{GaN}}{\pi}\left[\sinh^{-1}\left[\frac{t_{ox}^2 + H_{Fin}^2 + 2(t_{ox}+d)H_{Fin}}{\sqrt{(t_{ox}+d)^2 - t_{ox}^2}}\right] - \sinh^{-1}\left[\sqrt{\frac{t_{ox}}{\sqrt{(t_{ox}+d)^2 - t_{ox}^2}}}\right]\right] \\ for\ H_{Fin} < W_{Fin} \\ \frac{2\varepsilon_{GaN}}{\pi}\left[\sinh^{-1}\left[\frac{t_{ox}^2 + W_{Fin}^2 + 2(t_{ox}+d)W_{Fin}}{\sqrt{(t_{ox}+d)^2 - t_{ox}^2}}\right] - \sinh^{-1}\left[\sqrt{\frac{t_{ox}}{\sqrt{(t_{ox}+d)^2 - t_{ox}^2}}}\right]\right] \\ for\ W_{Fin} < H_{Fin} \end{cases}$$

And

$$C_2 = 0.35\frac{L_G\varepsilon_{GaN}}{2\pi}\ln\left(\frac{\pi L_G}{\sqrt{(t_{ox}+d)^2 - t_{ox}^2}}\right)$$

[0035] This allows us to incorporate the effect of the side gate into the boundary conditions for the electric field at the channel side of the structure as follows

$$\xi_{GaN|d} = \frac{qn_s - \Delta Q_{side}}{\varepsilon_{GaN}}$$

[0036] The electric field in the AlGaN layer at the AlGaN/GaN interface can then be expressed as

$$\xi_{AlGaN|d} = \frac{qn_s - \Delta Q_{side} - \sigma_{pol}}{\varepsilon_{AlGaN}}$$

[0037] where n_s is the 2DEG sheet density and $\sigma_{pol} = \sigma_{sp} + \sigma_{pz}$ is the polarization charge density due to spontaneous and piezoelectric charges. Solving Poisson's equation in the AlGaN barrier with the proper potential boundary conditions yields a threshold voltage equation that can be expressed as

$$V_T = \varphi_b - \frac{\Delta E_C}{q} - \frac{qn_{th}}{\varepsilon_{AlGaN}} \cdot (d + t_{ox}) + \frac{\sigma_{pol}}{\varepsilon_{AlGaN}} \cdot (d + t_{ox}) + \frac{\Delta Q_{side}}{\varepsilon_{AlGaN}} \cdot (d + t_{ox})$$

[0038] where n_{th} is the threshold 2DEG density, conventionally used as $5 \cdot 10^{10}\ cm^{-2}$. Therefore, the threshold voltage shift as a function of Fin width can be expressed as:

[0039] $$\Delta V_T = \frac{C_{side}}{C_{barrier}}\left[\varphi_b - \frac{\Delta E_C}{q} - \frac{qn_{th}}{\varepsilon_{AlGaN}} \cdot (d + t_{ox}) + \frac{\sigma_{pol}}{\varepsilon_{AlGaN}} \cdot (d + t_{ox})\right]$$

[0040] which indicates, a stronger threshold voltage shift for larger sidewall capacitance C_{side} (that is taller Fin) compared to $C_{barrier} = \frac{\varepsilon_{AlGaN} W_{Fin} L_G}{d} + t_{ox}$.

[0041] Transistor linearization over wide V_{GS} by the synthesis of multi-Fin MIS-HEMTs is shown in Figure 3A and Fig. 3B, which show typical non-linear I_{DS} (V_{GS}) characteristics for individual Fins, consisting of the characteristics of the multi Fin device **301, 311** and a planar device ($W_{Channel}$ of 1000 nm) **302, 312**, single Fin devices with Fin width of 300 nm **303, 313**, 100 nm **304, 314**, 50 nm **305, 315**, but a linearized transfer characteristics when a combination of Fins with different widths. As demonstrated in Figure 2, by decreasing the width of the Fin, the threshold voltages (V_T) and the peak point of g_m of single Fin MIS-HEMTs shift to positive direction of V_{GS}. g_m is transconductance, $\frac{dI_D}{dV_G}$ which is the first derivative of I_D by V_G. By utilizing this V_T and $g_{m,peak}$ shift phenomenon, the plateau of g_m can be widened by lifting up the decreasing region of g_m at high V_{GS} in the larger Fin devices by compensating of small Fin devices which have still increasing g_m at high V_{GS}. The characteristics of the multi Fin device **301, 312** is the sum of 3, 1, 3, and 8 Fins with the channel width of 1000 nm **302, 312**, 300 nm **303, 313**, 100 nm **304, 314**, and 50 nm **305, 315**, respectively. The weight of this sum can vary based on the real device characteristics. Noting that the I_{DS} does not saturate beyond the g_m roll-off voltage, especially for Fins, linearization can be achieved, for example, with a planar FET, multiple elements of larger current carrying Fins (wide-largest width), a few Fins with intermediate current capacity (intermediate width), and the largest number of small current capacity Fins (smallest width). This situation is illustrated

in Figure 3B where such a combination can lead to linearization of the g_m curve over ΔV_{GS} = 8V. The decrease of drain current is mainly due to small Fin width, and it should be noted that the normalized drain current density of small Fin width devices by the Fin widths were similar or slightly higher than large Fin width devices. In example preferred devices, a width range is 130~200 nm for the widest fin, 70~130 nm for the middle fins, and less than 70 nm for the narrow fins. However, the ranges are affected by epitaxial layer structures and 2DEG density. The selection of the number of Fins and the Fin widths, depends primarily on the threshold voltage and the current carrying capacity. Dimensions can also change with particular material specifications, such as the thickness of the AlGaN barrier layer.

[0042] A preferred fabrication process flow is described in Figure 4. AlGaN/GaN epitaxial layer growth **401** is conducted. For the ohmic contact first process, patterning, deposition, and annealing of ohmic contact **404** is performed, and GaN Fin etching **405**, surface smoothening by TMAH- or KOH-based wet chemicals and gate dielectric deposition **406**, and gate metallization and passivation **407** follows. On the other hand, for the GaN Fin etching first process, patterning and GaN Fin etching **402** and regrowth of AlN and AlGaN layers on the Fin sidewalls **403** is performed prior to the ohmic contact formation **404**. Then, the surface treatment and gate dielectric deposition **406** and gate metallization and passivation **407** steps is performed. Generally, the method improves intrinsic linearity of transistors by using lithographical changes to provide the preferred structures.

[0043] Silvaco Atlas simulations that capture the 3D electrostatics of tri-gate Fin-MIS-HEMTs can be utilized to gain further insights into the device performance and extract the DC characteristics of the device for utility in the mm-wave simulations. Figure 5 shows the effect of the sidewall gate on the electron density in the Fin-MIS-HEMT in the cross-section under the gate, for different Fin widths, at thermal equilibrium (V_{GS}=V_{DS}=0 V). The sidewall gates significantly reduce the

electron density in the channel for the same gate bias. A line cut taken at 1nm below the AlGaN barrier (d=5nm) in the GaN layer to display the carrier concentration is shown in Figure 6. The Fin-MIS-HEMT reduced the electron concentration in the channel by nearly two orders of magnitude. This reduction of carrier concentration is enhanced for narrower Fins.

[0044] In an important aspect of the invention, the benefits offered by conventional planar MIS-HEMTs are combined with narrow Fin-HEMTs for much wider-range tuning of threshold voltages (V_T) as well as a linearized drain current (I_D). In order to widen the g_m plateau much further for higher linearity, we designed a synthesized multi-Fin MIS-HEMT with weights of 1, 0.22, 0.39, 0.25 and 0.19 for planar, 160, 100, 80, and 50 nm fins, respectively, (see straight lines in Figure 7B and 7D(Figure 7B shows I_D-V_G curves and 7D shows gm-V_G curves. Both figures are illustrating linearized characteristics)). The detailed method of this linearization is discussed below.

[0045] In order to quantitatively approach gm compensation method, we can express the I_D, g_m, and g'_m for the multi-Fin device with different W_{Fin} as

$$I_{D,total}(V_{GS}) = \alpha_1 I_{D,1}(V_{GS} - V_{T,1}) + \alpha_2 I_{D,2}(V_{GS} - V_{T,2}) + \cdots + \alpha_n I_{D,n}(V_{GS} - V_{T,n}),$$

$$g_{m,total}(V_{GS}) = \alpha_1 g_{m,1}(V_{GS} - V_{T,1}) + \alpha_2 g_{m,2}(V_{GS} - V_{T,2}) + \cdots + \alpha_n g_{m,n}(V_{GS} - V_{T,n}),$$

$$g'_{m,total}(V_{GS}) = \alpha_1 g'_{m,1}(V_{GS} - V_{T,1}) + \alpha_2 g'_{m,2}(V_{GS} - V_{T,2}) + \cdots + \alpha_n g'_{m,3}(V_{GS} - V_{T,n}),$$

where α_n is the weight of nth channels for a family of Fins with a $W_{Fin,n}$, and a $V_{T,n}$. Therefore, there are two options to control the drain current of the multi-Fin device to control its linearity, since $W_{Fin,n}$ determines $V_{T,n}$ and $g_{m,n}$, so we can use W_{Fin} and α_n to engineer the shape of $I_{D,total}$ for a flat g_m. To demonstrate an example, we chose

a planar device and 4 different Fin devices with W_{Fin} of 160, 100, 80, and 50 nm, because they are uniformly separated by gate voltages in g_m" curves, see Figure 8, meaning that fins will complement each other for making g_m' close to zero. (The notation ' means derivative. So, g_m' is the first derivative of g_m, and g_m" is the second derivative of g_m). Plotted g_m' curves in Figure 9 are smoothened one-time by 7-points averaging to see their characteristic shapes clearly. Only experimental data are presented in Figure 7 onwards. The planar device had negative g_m' values for V_G > -4 V and didn't go back to positive values signifying that g_m keep only decreasing. Therefore, we focused on making the integral of the g_m' of the planar device zero for V_G from -4 V to 2 V. To replenish this negative g_m', we can use other positive g_m' curves for such V_G regions with Fin devices having higher V_T. To simply minimize the negative g_m' of the planar device, we determined α_n=R×F, where R is defined as dividing the g_m' value of the overall device we want to linearize by that of the specific Fin component at a certain gate voltage for the g_m' peak, see Table 1, and F is an elevating factor to minimize the integration of g_m' from -4 V to 2 V which corresponds to Δg_m. Using the expected synthesized device result, this g_m compensation was performed total 4 times for each Fin component with higher V_T. Given that R is fixed based on the synthesized data, on the other hand, F was varied to minimize Δg_m, and the optimum F of 1.35 was achieved, see Fig. 10. Finally, the optimized weights were 1, 0.22, 0.39, 0.25, and 0.19 for a planar, W_{Fin} of 160, 100, 80, and 50 nm, respectively, resulting in the expected Δg_m of -0.7 μS with respect to V_G from -4 V to 2 V for the 4-Fin synthesized device which is more than 4 orders of magnitude reduction from that of the planar device.

[0046] The actual numbers of fins in the device layout were determined by multiplying the weight (α_n) and the original number of fins in the individual device (N_{Fin}), for example we multiplied α of 0.22 and N_{Fin} of 50 for W_{Fin} of 160 nm and rounded it to obtain a natural number of 11, because the number of fins cannot be a

fractional number, see the table in Figure 14. Then, the total channel width including the gap between each fin (W_{gap} of 200 nm) was calculated and normalized to 20 μm for the same device dimension (W_G of 20 μm). As a result, the width of planar device was calculated to 10.3 μm, and the number of fins were 6, 11, 8, and 8 for W_{Fin} of 160, 100, 80, and 50 nm, respectively, and it is plotted in Figure 11. It should be noted that the present design works in practice as evidenced by our experimental results. With the described design, a multi-Fin MIS-HEMT was fabricated with the same process. In Figure 12, a top-view SEM image shows a planar region and a fin region with the given numbers of fins for each W_{Fin}, and they are integrated well in one device with the same W_G. Measured I_D-V_G and g_m-V_G characteristics are plotted in Figures 13A-13D. The characteristics illustrate significantly improved linearity of the fabricated device. I_D-V_D characteristics with extracted f_T, unity current gain frequency (frequency when the current gain becomes unity), contour plot in Figure 13 strongly suggest that the device have $f_T > 40$ GHz over most of the saturation region.

[0047] Figures 15A-15C illustrate an example embodiment multi-Fin MIS-HEMTs semiconductor device architecture. The structure includes a substrate **100**, a buffer **110**, multi-layer fins **120-n**, **130-n** having fin to fin distances **104**, gate insulator **140-n** and gate metal **150**. In the example embodiment according to the present invention, the multi-Fin MIS-HEMT includes gate metal **150** and gate insulator **140-n** covering multiple AlGaN/GaN fins **130-n**, **120-n**, sitting on top of the GaN buffer layer **110** atop a substrate **100**. The AlGaN/GaN fins **130-n**, **120-n** have a width of 40 nm - 500 nm, and a height of 30 nm ~ 1 μm. The fin edge-to-edge distance **104** can also vary from few nano meters to few microns._.

[0048] Figures 16A-16C illustrate an example embodiment planar MIS-HEMTs semiconductor device architecture that is used with multi-fin architectures described above. The structure includes a substrate **100**, a buffer **110**, a channel-layer **120**, a

barrier layer **130**, a gate insulator **140** and a gate metal **150**. In the example embodiment according to the present invention, the planar MIS-HEMT includes gate metal **150** and gate insulator **140** covering AlGaN/GaN layers **130**, **120**, sitting on top of the GaN buffer layer **110** atop a substrate **100**. The width of channel **105** is larger than 1000 nm, as it is a planar channel device. The thickness of gate insulator **140** and AlGaN barrier layer **130** can also vary from few nanometers to few tens of nano meters. In Figure 16B, conduction channels will be formed at the interface between 1) 130 and 120, and 2) 140 and 120. 2DEG will be formed at 130 and 120, and the channel will be formed at 140 and 120. In this planar device structure, the sidewall channel will be negligible, because the 2DEG is more conductive and the length is longer than the channel.

[0049] Preferred embodiment devices have a number of applications. One application is to replace conventional planar or Fin-HEMTs for mm-wave applications. Its intrinsically tunable capability with very wide V_{GS} ranges allows for wideband linearity, along with high f_T, f_{max} and low noise performance. The present multi-Fin MIS-HEMT device is expected to yield linearity over wider gate voltages through the utility of multiple Fin channels, open up the possibility of using low metal work function – due to absence of or minimal gate leakage currents in the MIS-HEMT devices compared to HEMT devices –as a gate thereby enabling additional control over threshold voltage engineering for the superposition of drain currents for linearization, scalability to extremely short gate lengths (20nm target) without risking substantial increases in series resistances due to the use of multi-Fin width devices.

[0050] While specific embodiments of the present invention have been shown and described, it should be understood that other modifications, substitutions and alternatives are apparent to one of ordinary skill in the art. Such modifications,

substitutions and alternatives can be made without departing from the spirit and scope of the invention, which should be determined from the appended claims.

[0051] Various features of the invention are set forth in the appended claims.

CLAIMS

1. A MIS-HEMT, comprising a substrate, a buffer layer upon the substrate, a plurality of multi-layer fins with channel and barrier material, wherein the fins have a plurality of widths and are formed upon the buffer layer, gate insulator surrounding the fins and gate metal conformally covering the gate metal, wherein plurality of widths include largest, intermediate and smallest widths, selected to lead to the separate turn-on voltage thresholds for the largest, intermediate and smallest widths of the MIS HEMT fins to flatten the transconductance g_m curve over an operational range of gate source voltage.

2. The HEMT of claim 1, further comprising a planar channel

3. The HEMT of claim 2, wherein the multi-layer fins are sized such that their current carrying capacity becomes larger than the planar channel to provide current linearization over the operational range.

4. The HEMT of claim 2, wherein the planar channel comprises a width greater than 1 μm, and all of the plurality of widths are less than 500 nm.

5. The HEMT of claim 1, wherein the channel comprise multiple AlGaN/GaN fins and the gate insulator comprises one of Al_2O_3, HfO_2

6. The HEMT of claim 1, wherein the plurality of multi-layer fins comprises families of largest, intermediate and smallest widths, each family including a plurality of fins, and each family is structured and sized to turn on at a different bias voltage

7. The HEMT of claim 1, wherein the number of Fins for each family is proportional to threshold voltage and current overdrive and varies from one Fin family to the other.

8. The HEMT of claim 1, wherein the plurality of widths are selected such that the threshold voltages (V_T) and the peak point of transconductance g_m of single Fins from the plurality of Fins lift up a decreasing region of transconductance g_m at higher V_{GS} in larger Fins of the plurality of fins.

9. The HEMT of claim 1, wherein the plurality of widths are selected such that threshold voltage V_T and $g_{m,peak}$ shift are balanced to flatten the plateau of transconductance g_m contributed by a larger Fin via compensation of smaller Fins that still have increasing g_m at high V_{GS}.

10. The HEMT of claim 1, comprising unetched source and drain regions.

11. The HEMT of claim 1, wherein the channel and barrier materials comprise Group III-V materials.

12. The HEMT of claim 1, wherein the channel and barrier materials comprise silicon with different ion-implant doses.

13. The HEMT of claim 1, wherein the plurality of widths are uniformly separated by gate voltages in second derivative of transconductance g_m'' curves to complement each other for reducing the first derivative of transconductance g_m' close to zero over the operational range.

14. A method of compensate for the first derivative of transconductance, g_m., in a MIS-HEMT, the method comprising:

turning on a first Fin in response to a first gate source voltage;

turning on a second smaller Fin in response to an increased gate voltage,

turning on a third Fin smaller than the second smaller Fin in response to a larger increased gate voltage, wherein the first, second smaller, and third Fin are sized such that smaller fin devices with quantitatively calculated weights replenish the negative region of the first derivative of transconductance g_m to reduce variation of g_m over an operatational range of gate source voltage.

15. The method of claim 14, further comprising first turning on a planar channel in response to a gate source voltage that is smaller than the first gate source voltage.

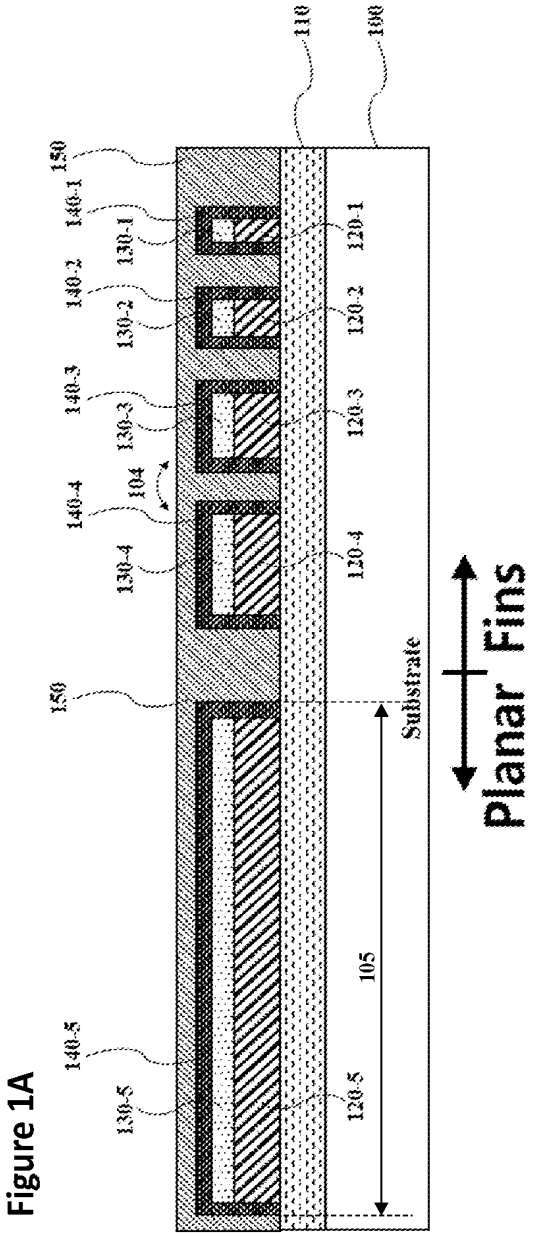

110
100
150
140-1
130-1
120-1
140-2
130-2
120-2
140-3
130-3
120-3
140-4
104
130-4
120-4
150
Substrate
Planar Fins
140-5
130-5
120-5
105

Figure 1A

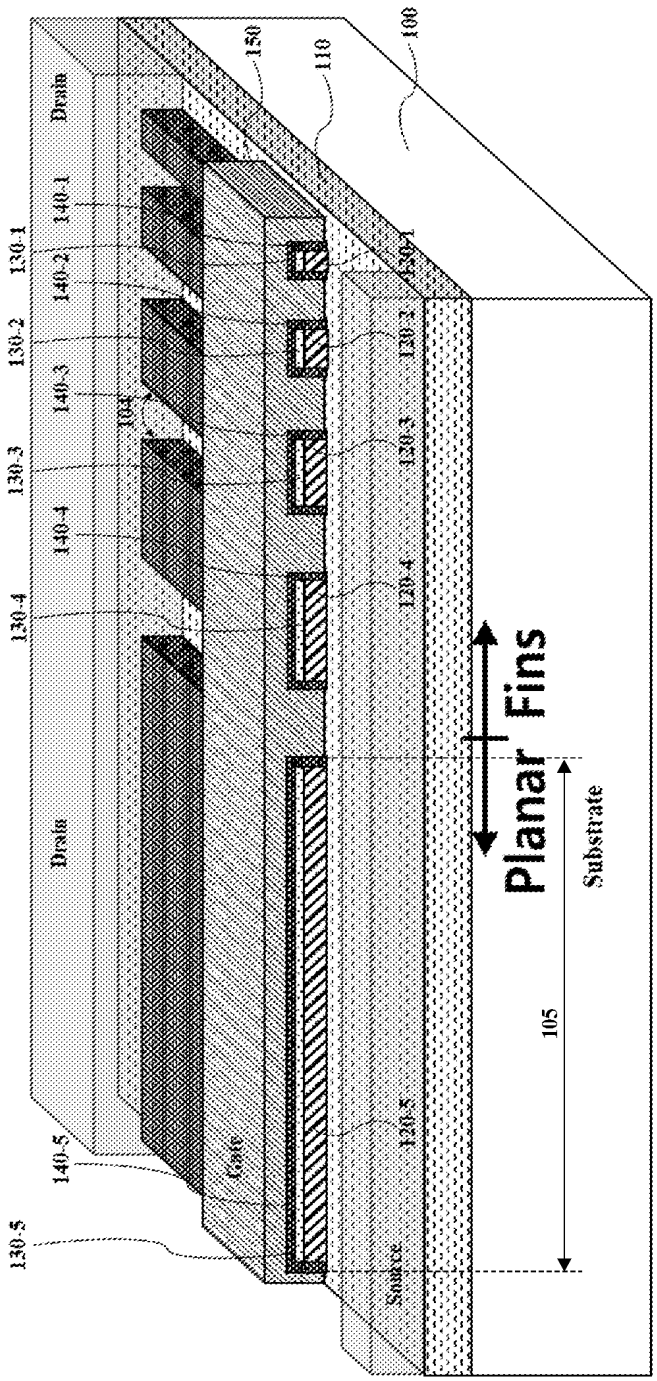

Drain
Drain
Gate
Source
Planar Fins
Substrate
105
104
150
110
100
140-1
140-2
140-3
140-4
140-5
130-1
130-2
130-3
130-4
130-5
120-1
120-2
120-3
120-4
120-5

Figure 1B

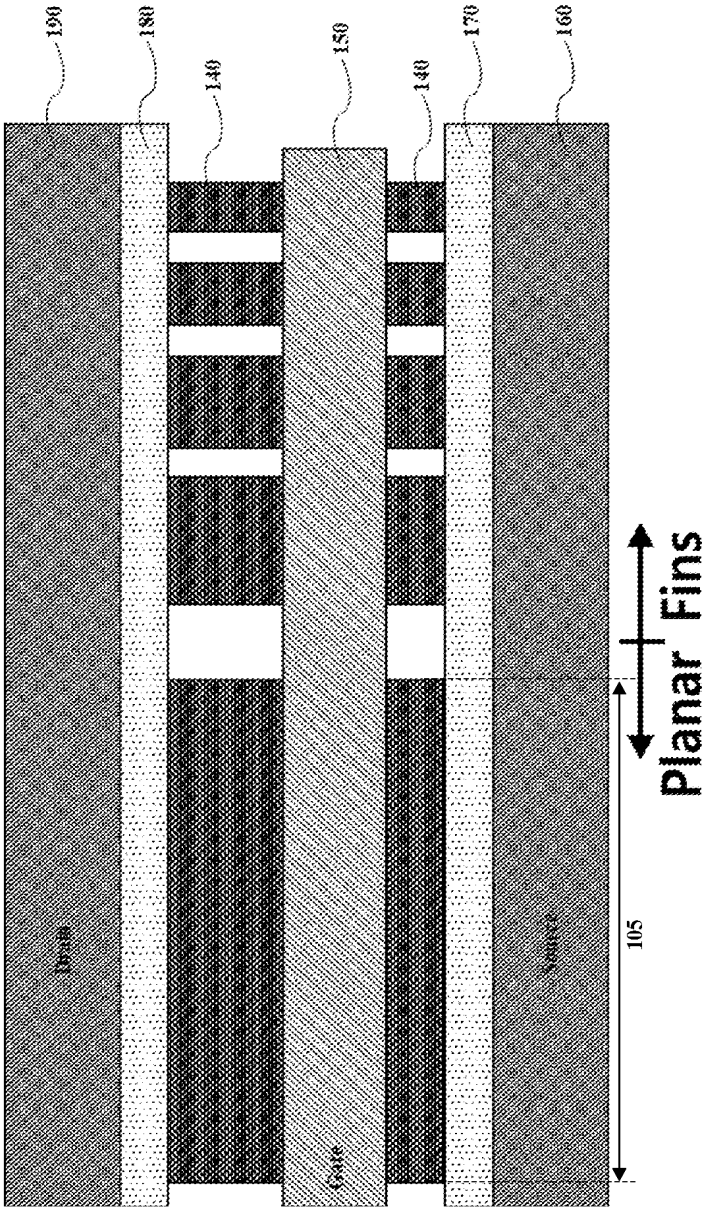


Figure 1C

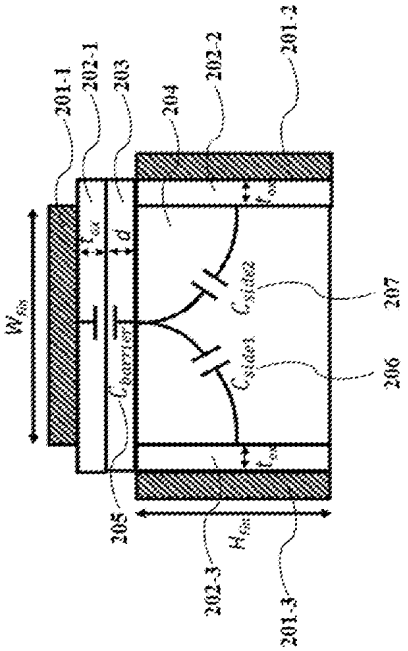


Figure 2A

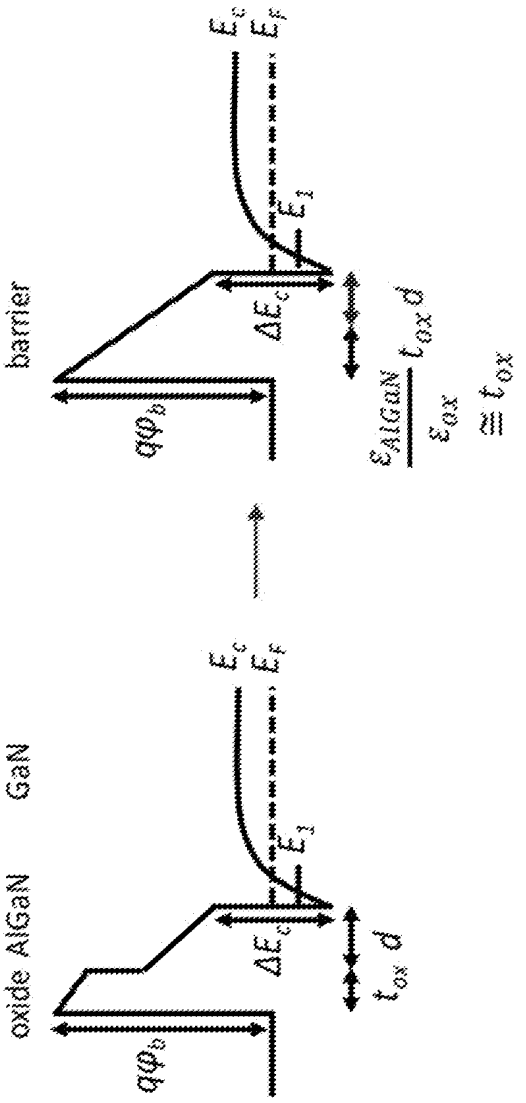


Figure 2B

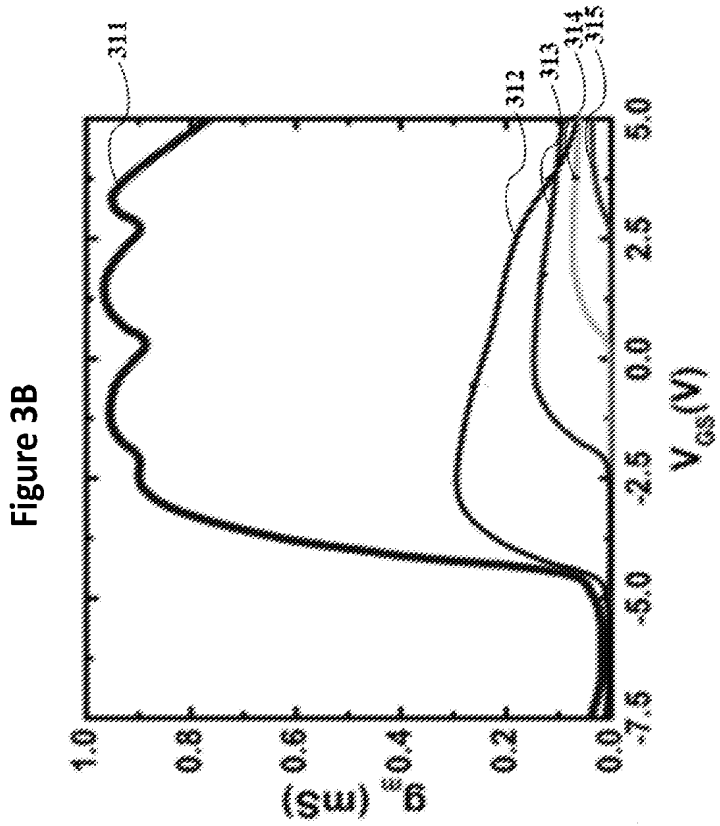


Figure 3B

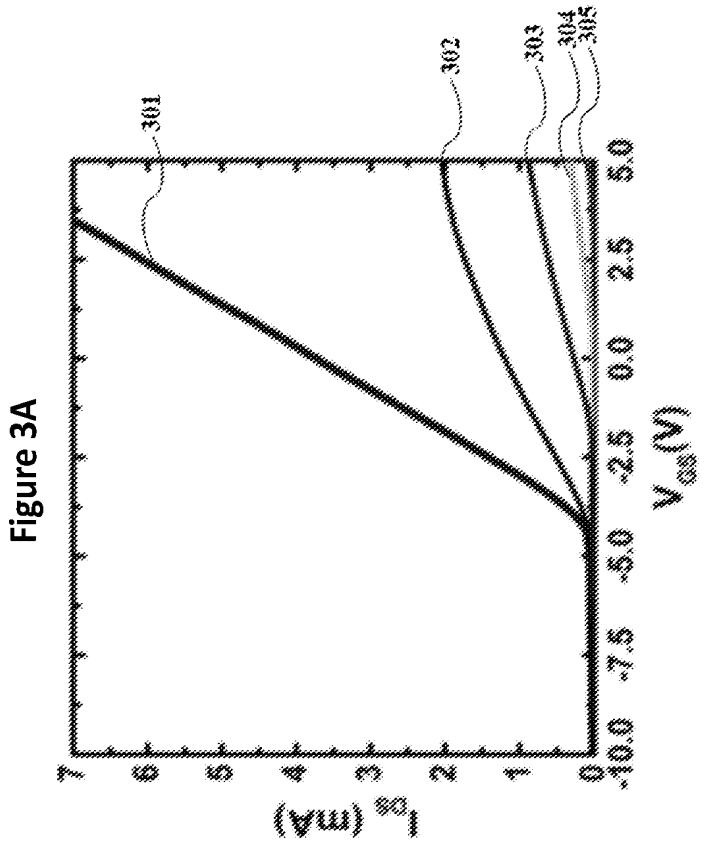


Figure 3A

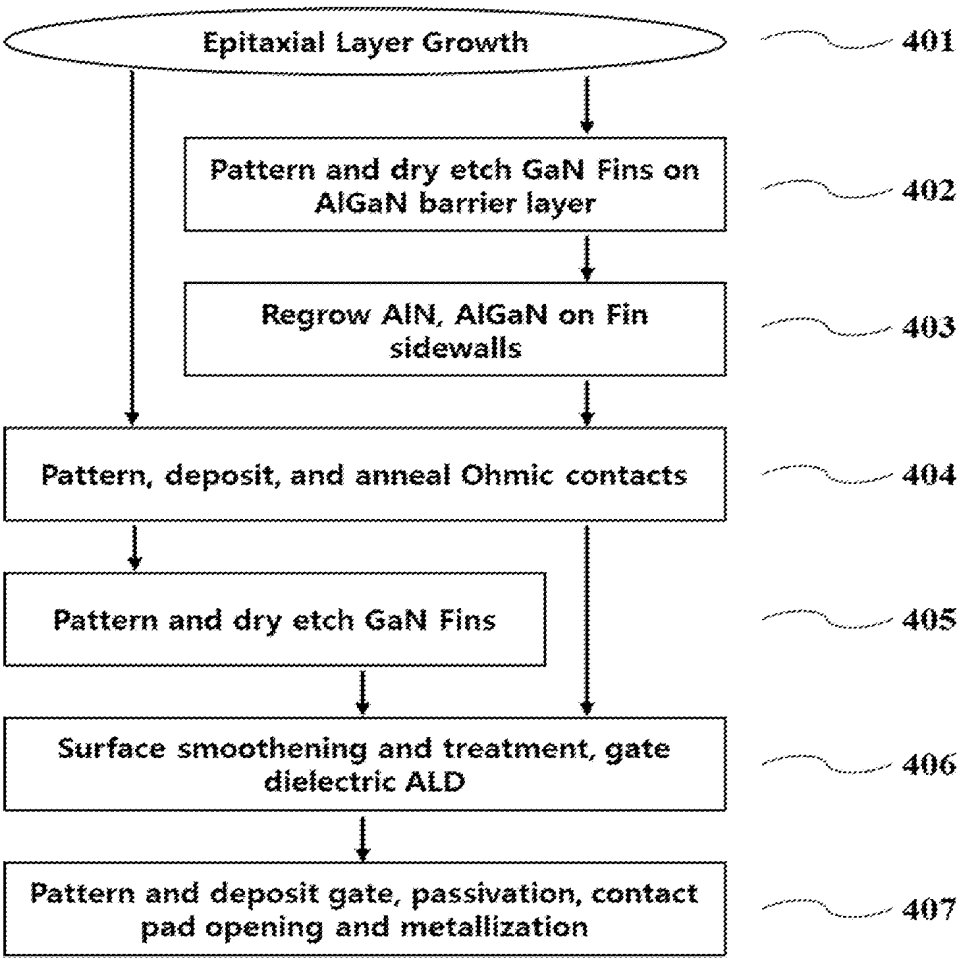

Epitaxial Layer Growth
401
Pattern and dry etch GaN Fins on AlGaN barrier layer
402
Regrow AlN, AlGaN on Fin sidewalls
403
Pattern, deposit, and anneal Ohmic contacts
404
Pattern and dry etch GaN Fins
405
Surface smoothening and treatment, gate dielectric ALD
406
Pattern and deposit gate, passivation, contact pad opening and metallization
407

Figure 4

Figure 5

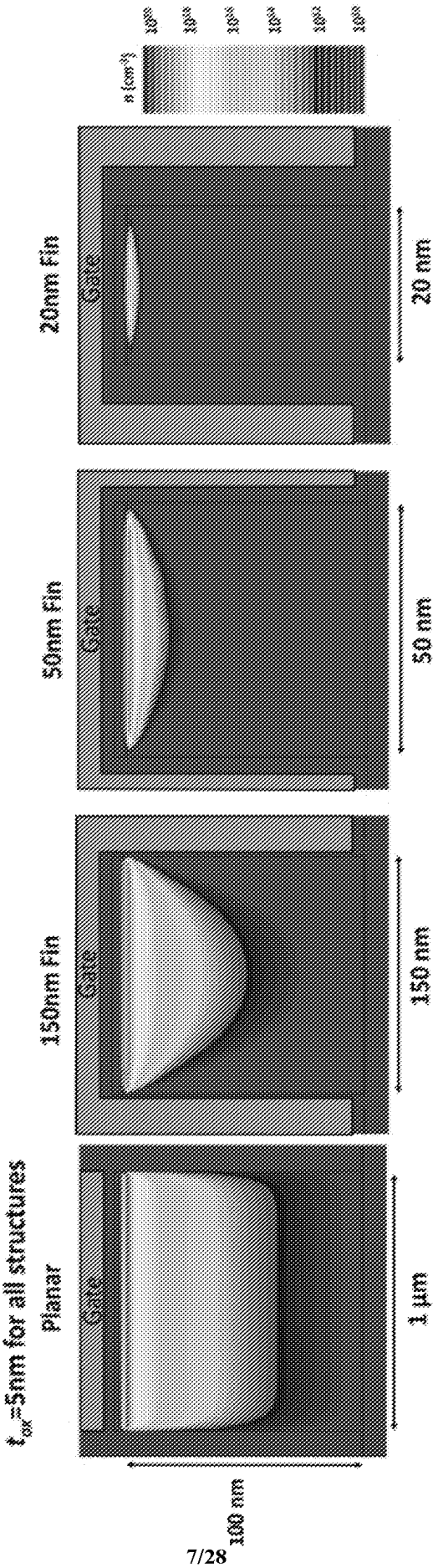
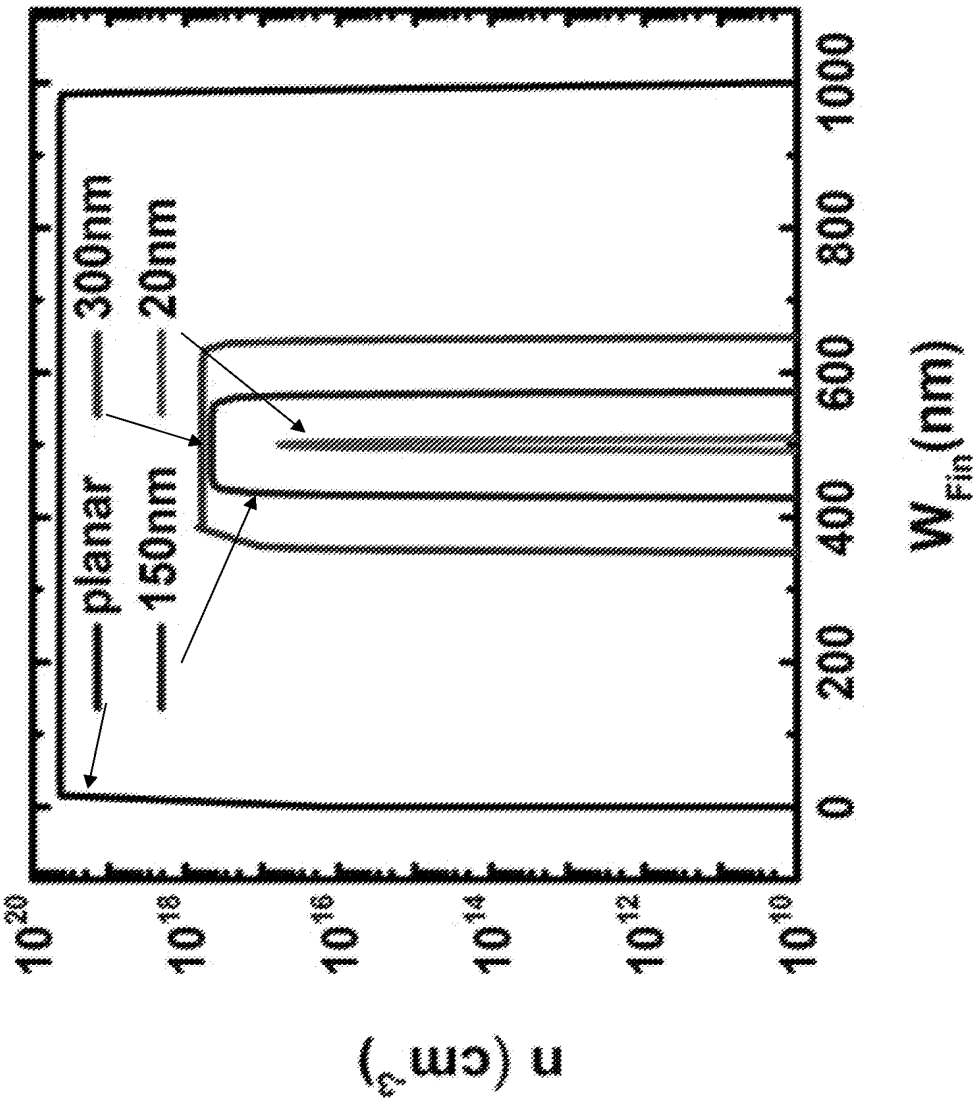

t_{ox}=5nm for all structures
Planar
Gate
1 µm
150nm Fin
Gate
150 nm
50nm Fin
Gate
50 nm
20nm Fin
Gate
20 nm
100 nm

Figure 6


n (cm^{-3})
10^{20}
10^{18}
10^{16}
10^{14}
10^{12}
10^{10}
0
200
400
600
800
1000
W_{Fin}(nm)
planar
150nm
20nm
300nm

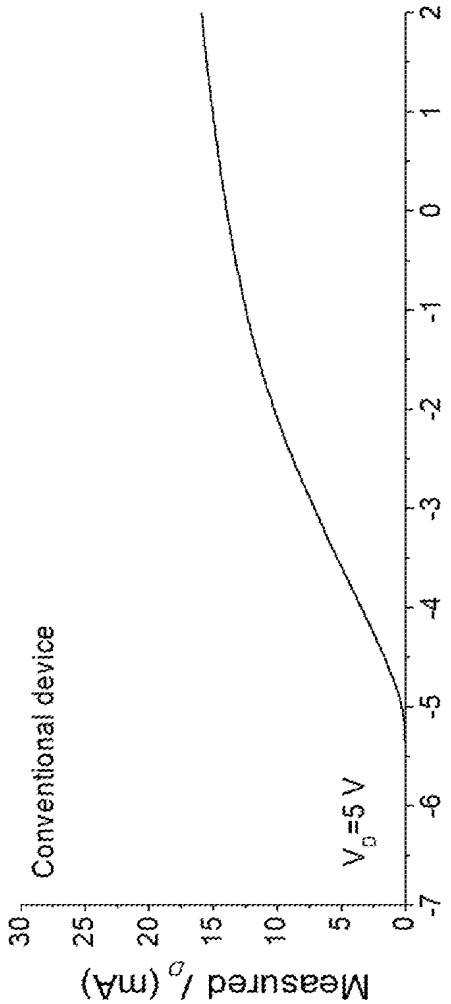


Figure 7A

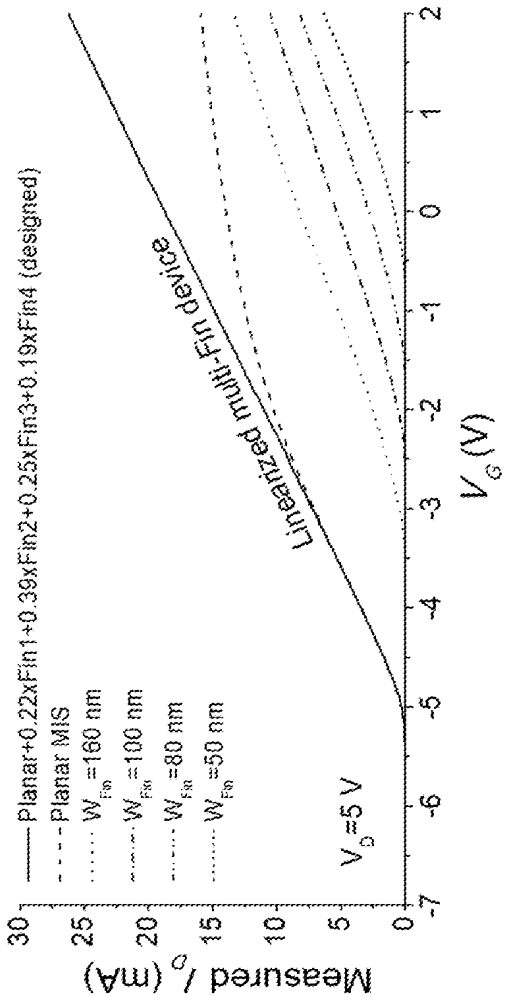


Figure 7B

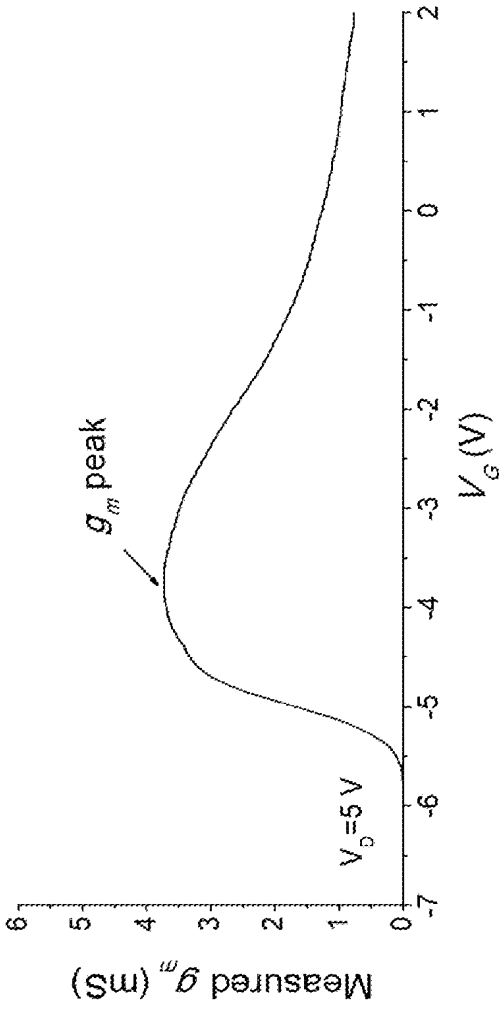


Figure 7C

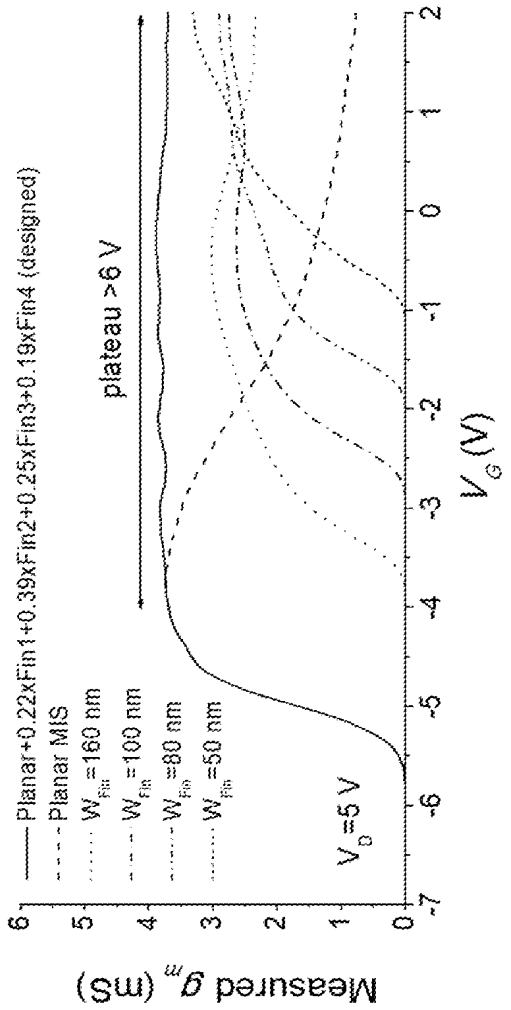


Figure 7D

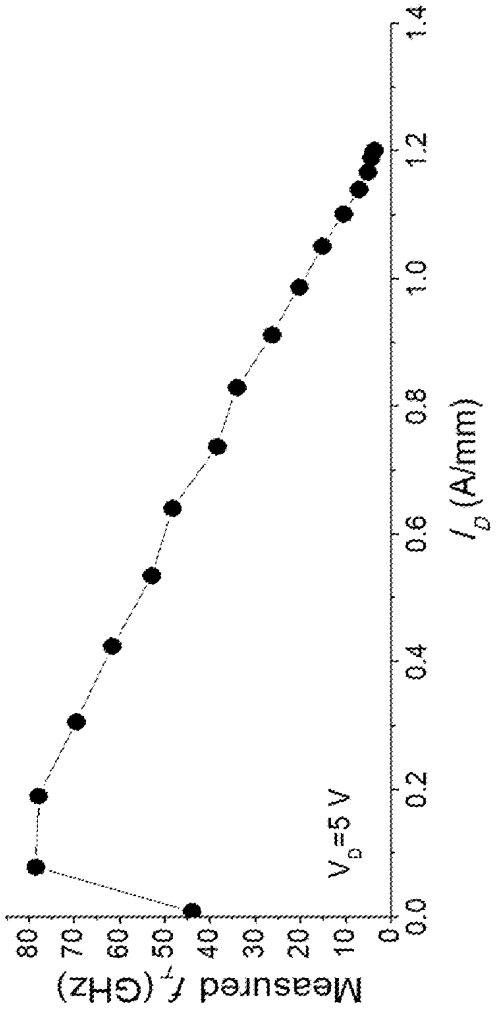


Figure 7E

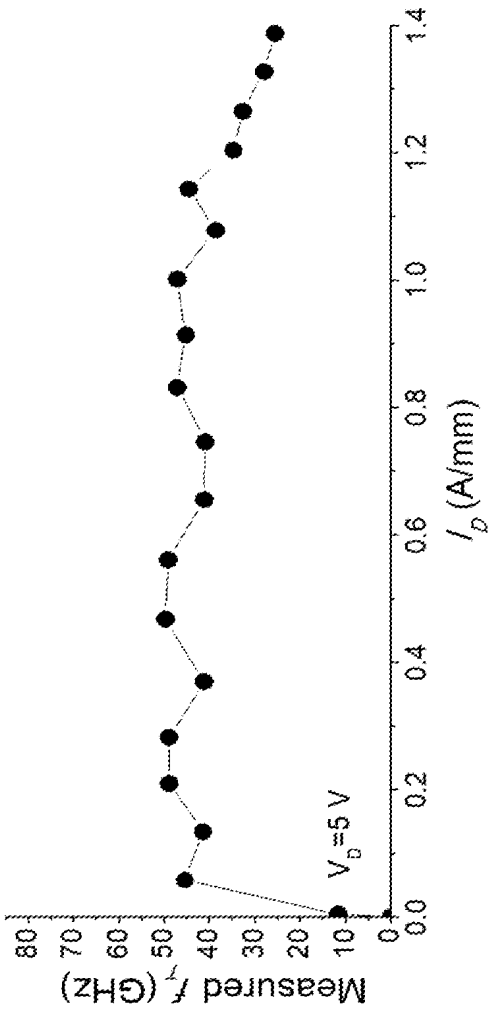


Figure 7F

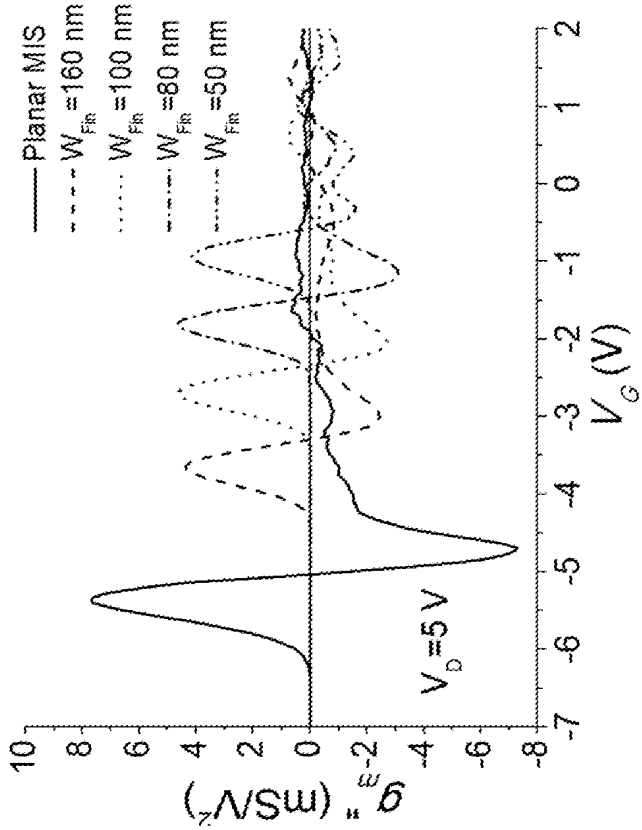

Planar MIS
W_Fin=160 nm
W_Fin=100 nm
W_Fin=80 nm
W_Fin=50 nm
V_D=5 V
g_m (mS/V)
V_G (V)
10
8
6
4
2
0
-2
-4
-6
-8
-7
-6
-5
-4
-3
-2
-1
0
1
2

Figure 8

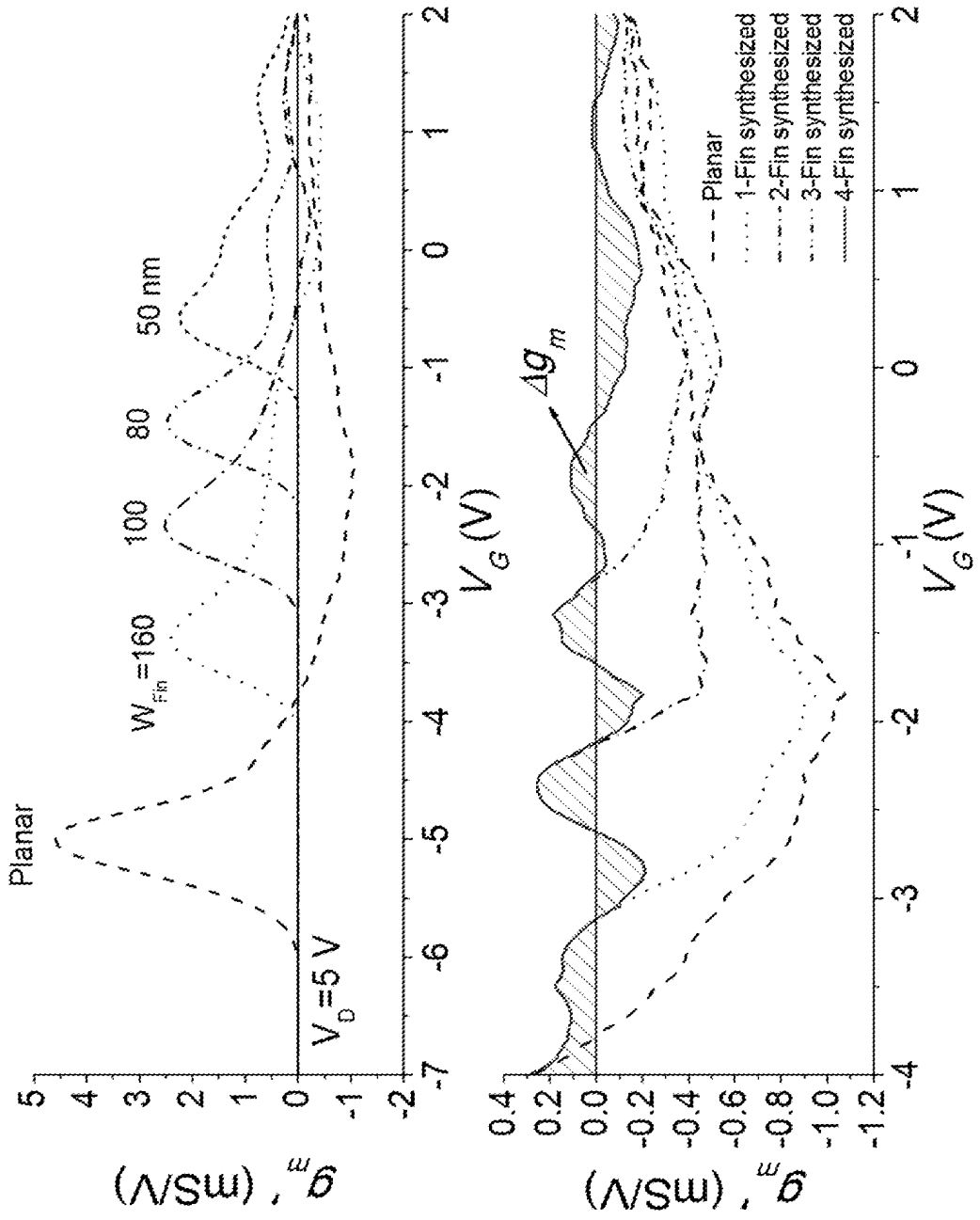

Planar
W_{Fin}=160
100
80
50 nm
V_D=5 V
g_m, (mS/V)
V_G (V)
Δg_m
Planar
1-Fin synthesized
2-Fin synthesized
3-Fin synthesized
4-Fin synthesized

Figure 9

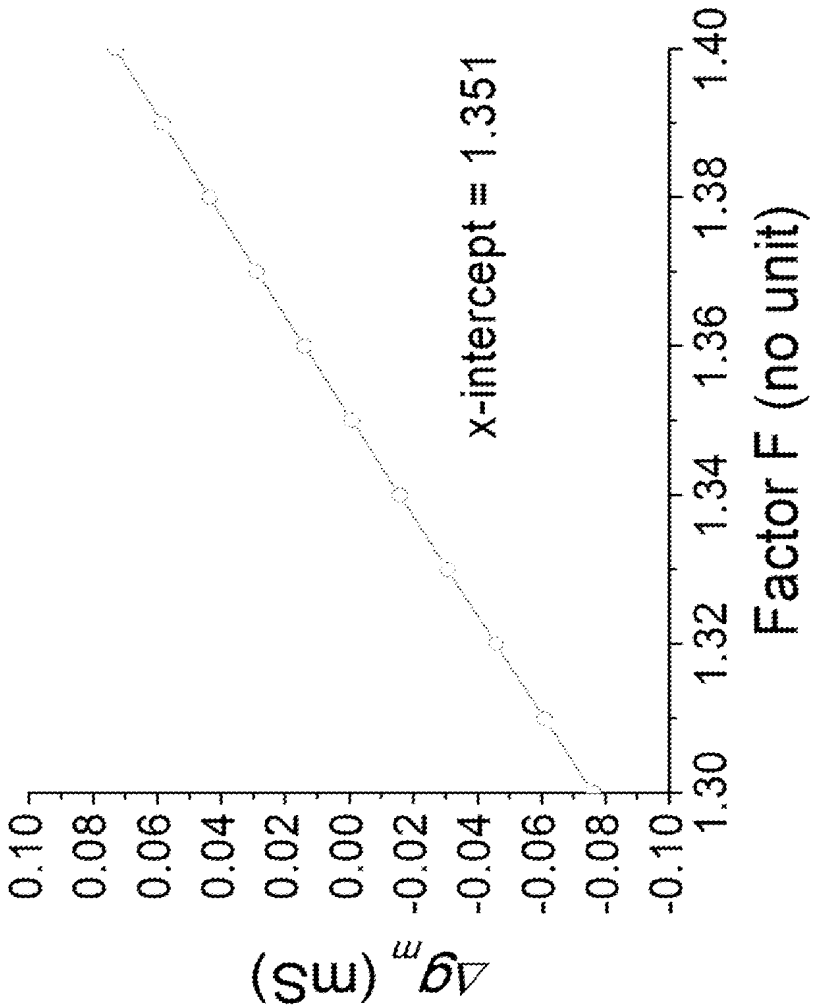

x-intercept = 1.351
Factor F (no unit)
Δg_m (mS)
0.10
0.08
0.06
0.04
0.02
0.00
-0.02
-0.04
-0.06
-0.08
-0.10
1.30
1.32
1.34
1.36
1.38
1.40

Figure 10

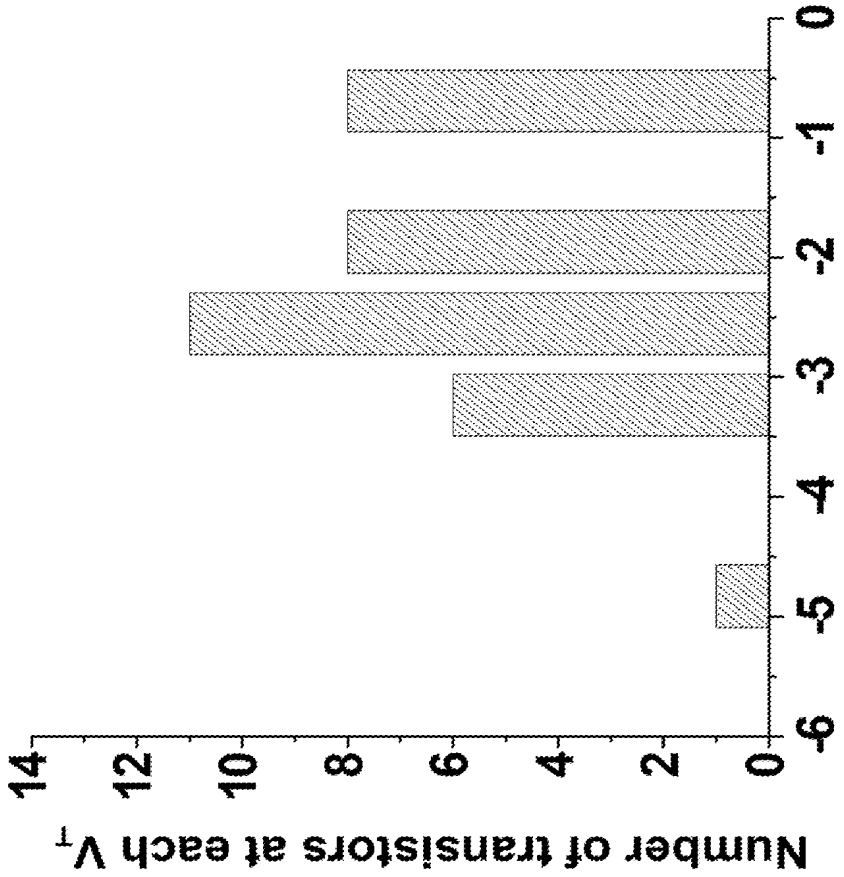


Figure 11

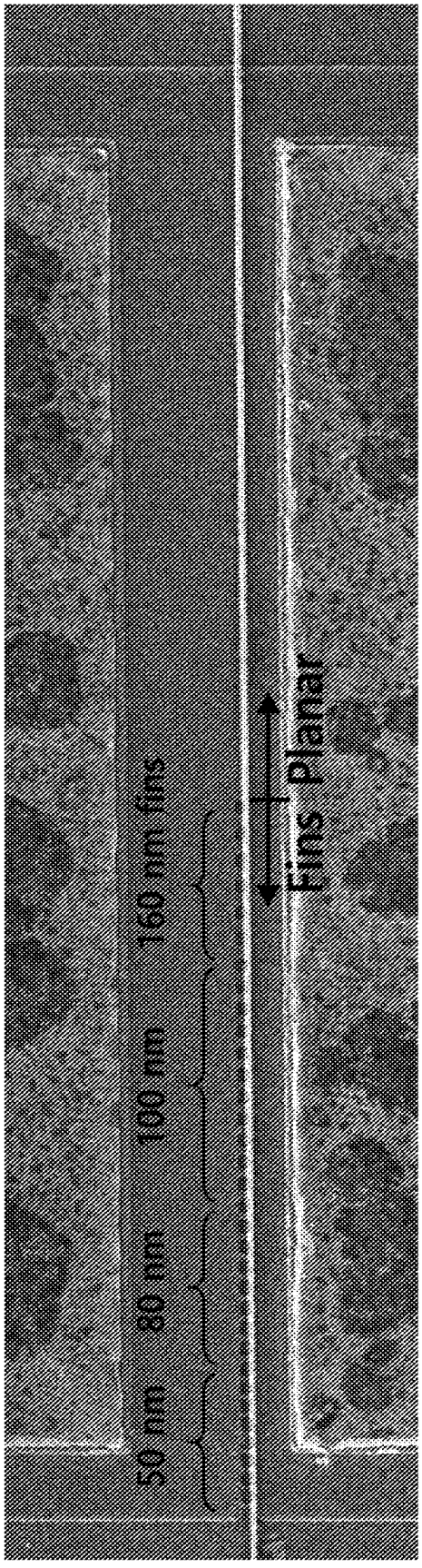


Figure 12

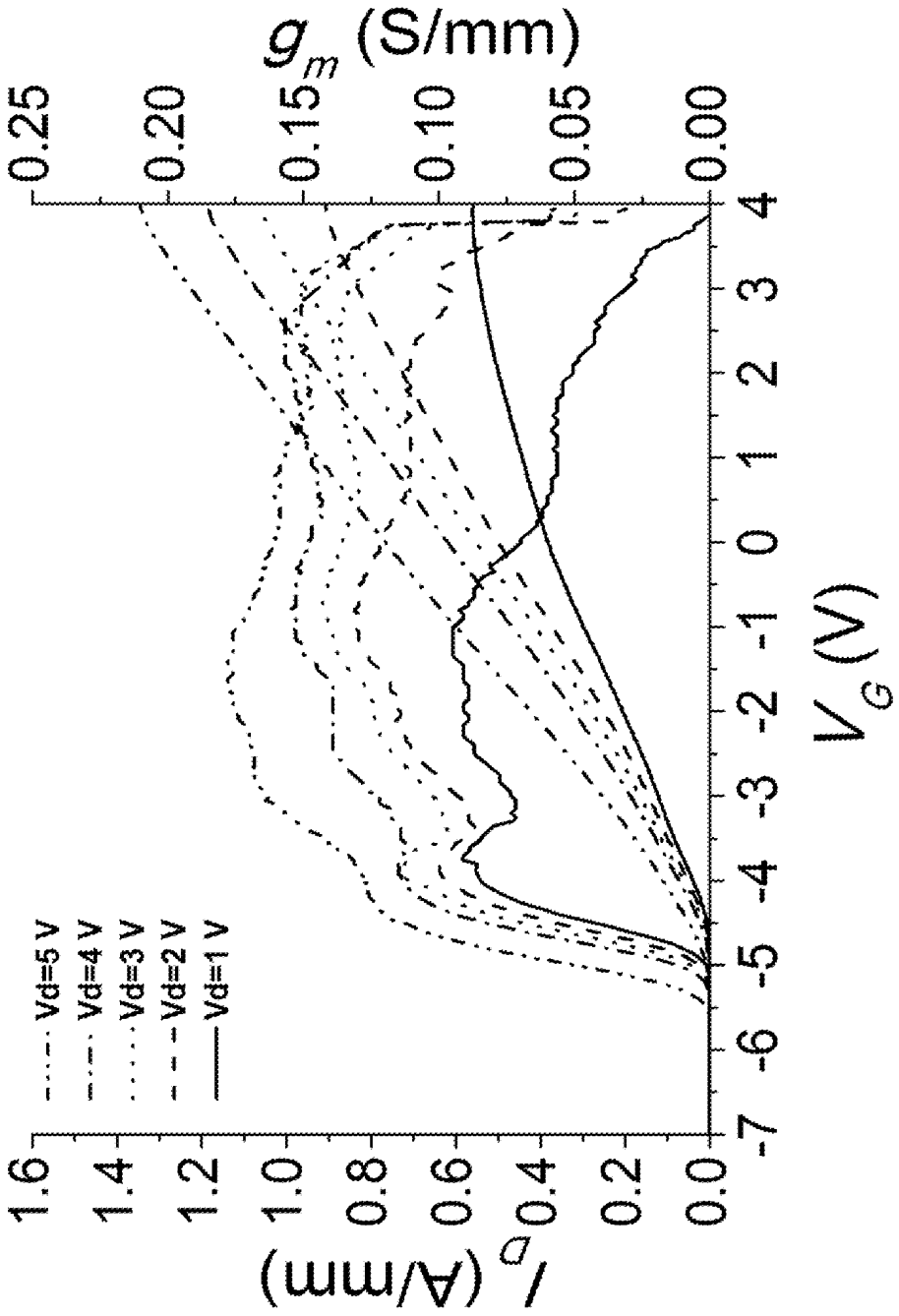

g_m (S/mm)
0.25
0.20
0.15
0.10
0.05
0.00
I_D (A/mm)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
V_G (V)
4
3
2
1
0
-1
-2
-3
-4
-5
-6
-7
Vd=5 V
Vd=4 V
Vd=3 V
Vd=2 V
Vd=1 V

Figure 13A

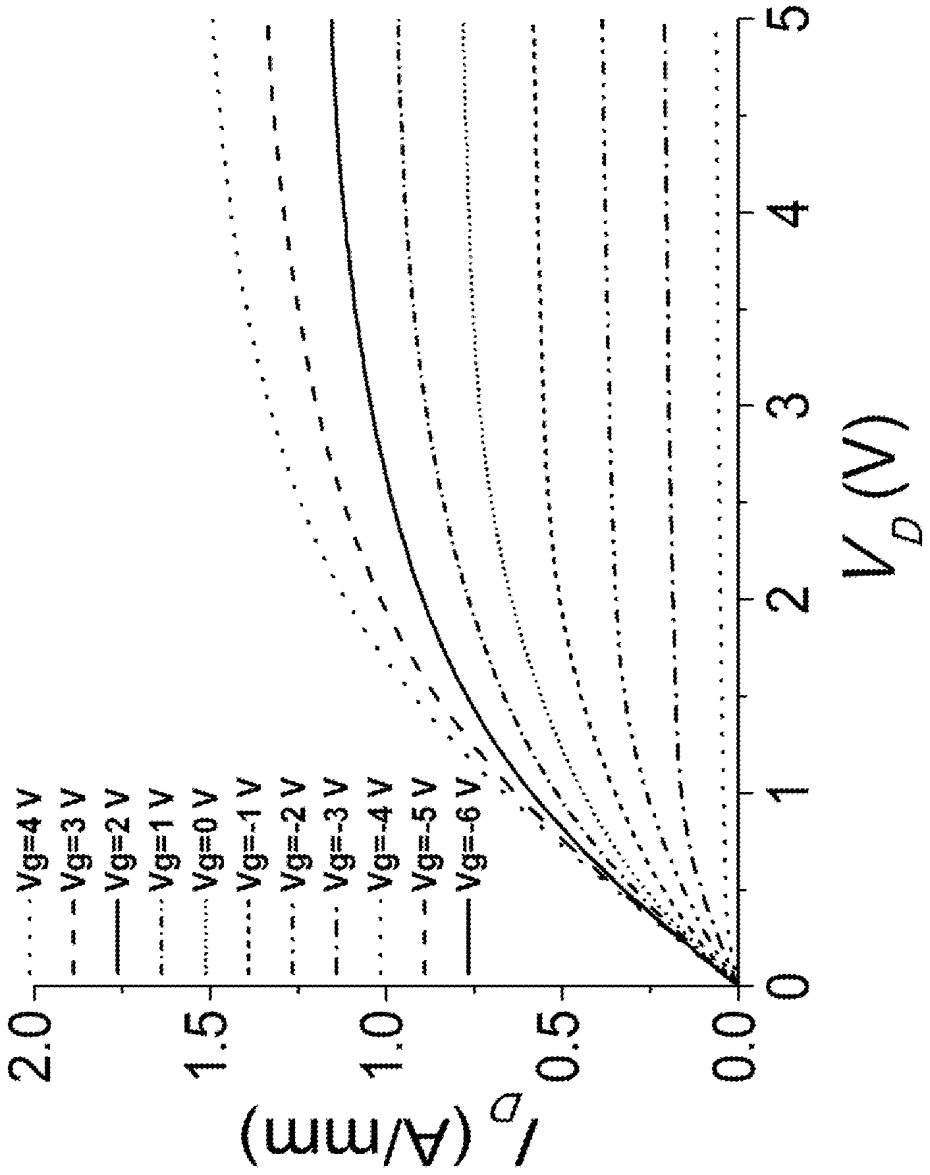

Vg=4 V
Vg=3 V
Vg=2 V
Vg=1 V
Vg=0 V
Vg=-1 V
Vg=-2 V
Vg=-3 V
Vg=-4 V
Vg=-5 V
Vg=-6 V
2.0
1.5
1.0
0.5
0.0
I_D (A/mm)
0
1
2
3
4
5
V_D (V)

Figure 13B

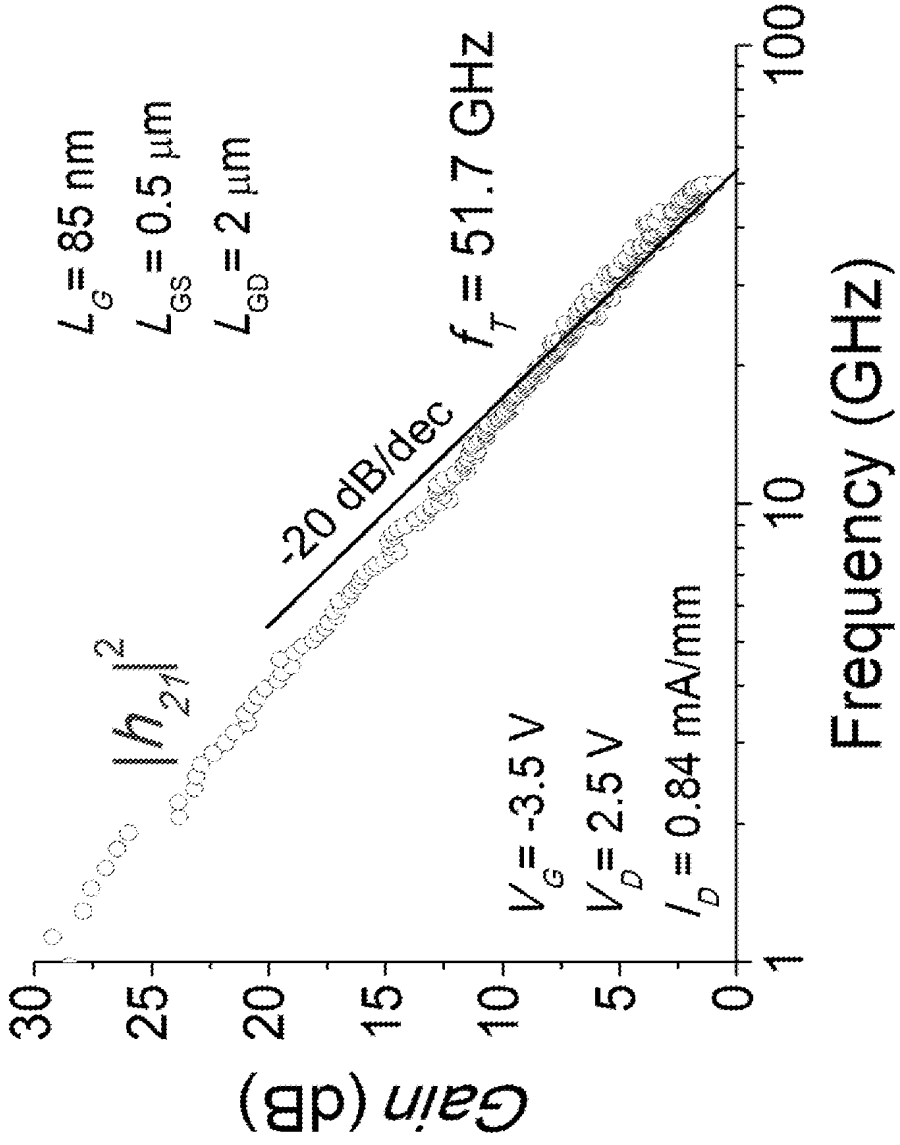

L_G = 85 nm
L_{GS} = 0.5 μm
L_{GD} = 2 μm
$|h_{21}|^2$
-20 dB/dec
f_T = 51.7 GHz
V_G = -3.5 V
V_D = 2.5 V
I_D = 0.84 mA/mm
Gain (dB)
Frequency (GHz)
30
25
20
15
10
5
0
1
10
100

Figure 13C

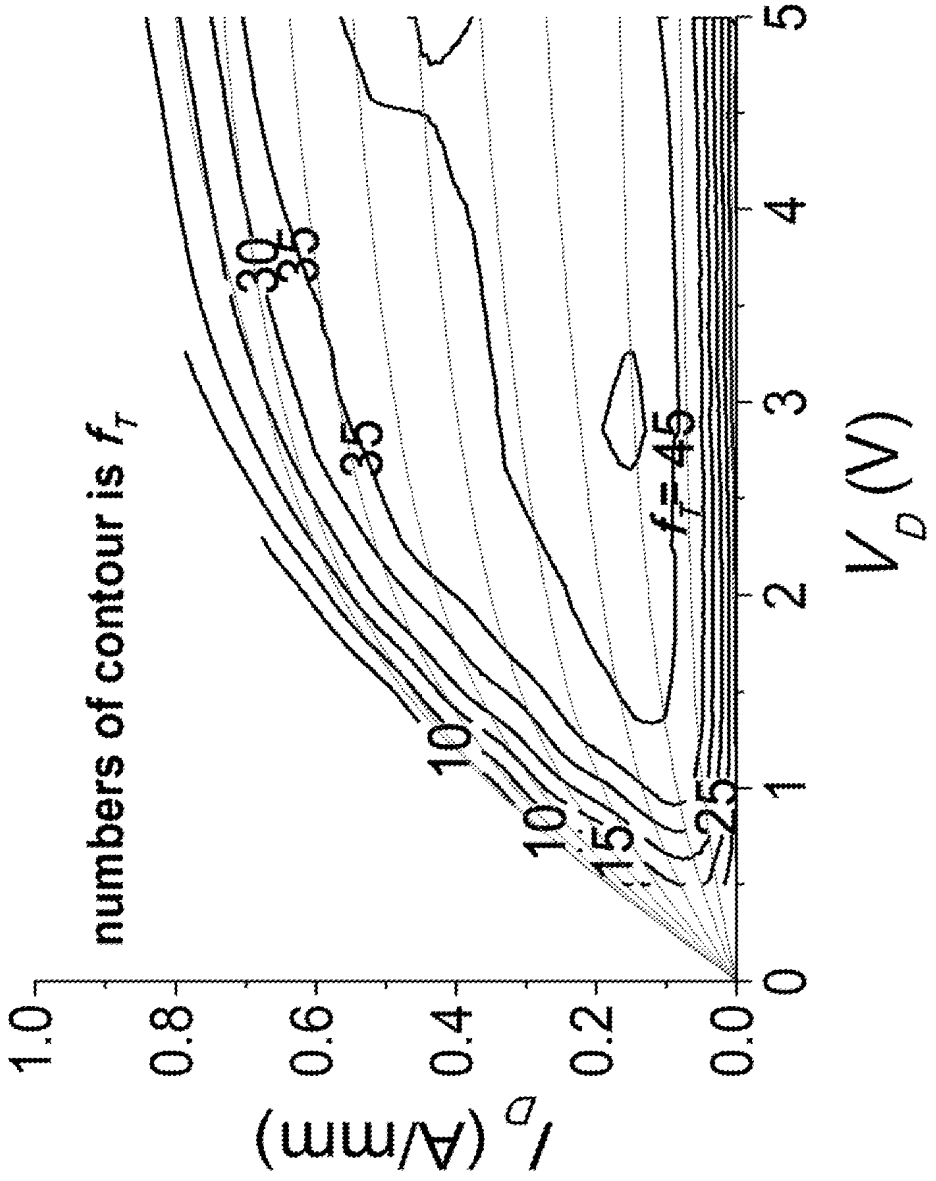

numbers of contour is f_T
I_D (A/mm)
V_D (V)
f_T=45
0.0
0.2
0.4
0.6
0.8
1.0
0
1
2
3
4
5
10
10
15
25
35
35
30

Figure 13D

	V_G (V)	-3.3	-2.35	-1.45	-0.6	|Ratio| (R)	Weight (α=R x F) (F=1.35)	# of fins (N_{Fin}) in individual devices (W_G=20 µm)	Product (α x N_{Fin}) (rounded)	Normalized # of fins in the synthesized de vice (W_G=20 µm)
g_m' (S/V)	Planar	-3.98E-04	-	-	-	1	1	1	1	10.3 µm
	160 nm	2.40E-03	-	-	-	0.17	0.22	50	11	6
	1-Fin synthesized	-	-7.34E-04	-	-	-	-	-	-	-
	100 nm	-	2.54E-03	-	-	0.29	0.39	55	21	11
	2-Fin synthesized	-	-	-4.52E-04	-	-	-	-	-	-
	80 nm	-	-	2.49E-03	-	0.18	0.25	66	16	8
	3-Fin synthesized	-	-	-	-3.09E-04	-	-	-	-	-
	50 nm	-	-	-	2.24E-03	0.14	0.19	80	15	8

Figure 14

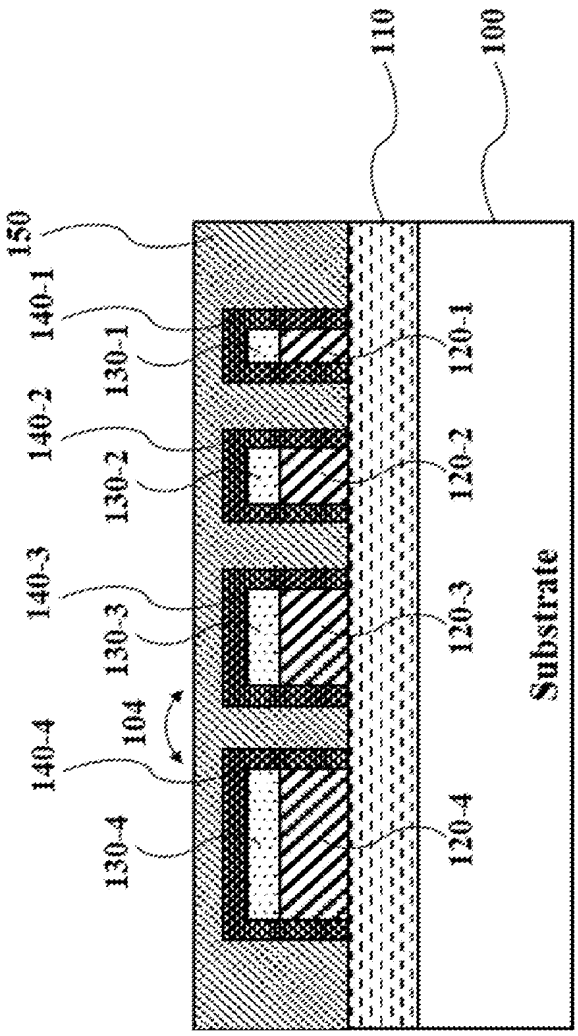

110
100
150
140-1
130-1
120-1
140-2
130-2
120-2
140-3
130-3
120-3
140-4
104
130-4
120-4
Substrate

Figure 15A

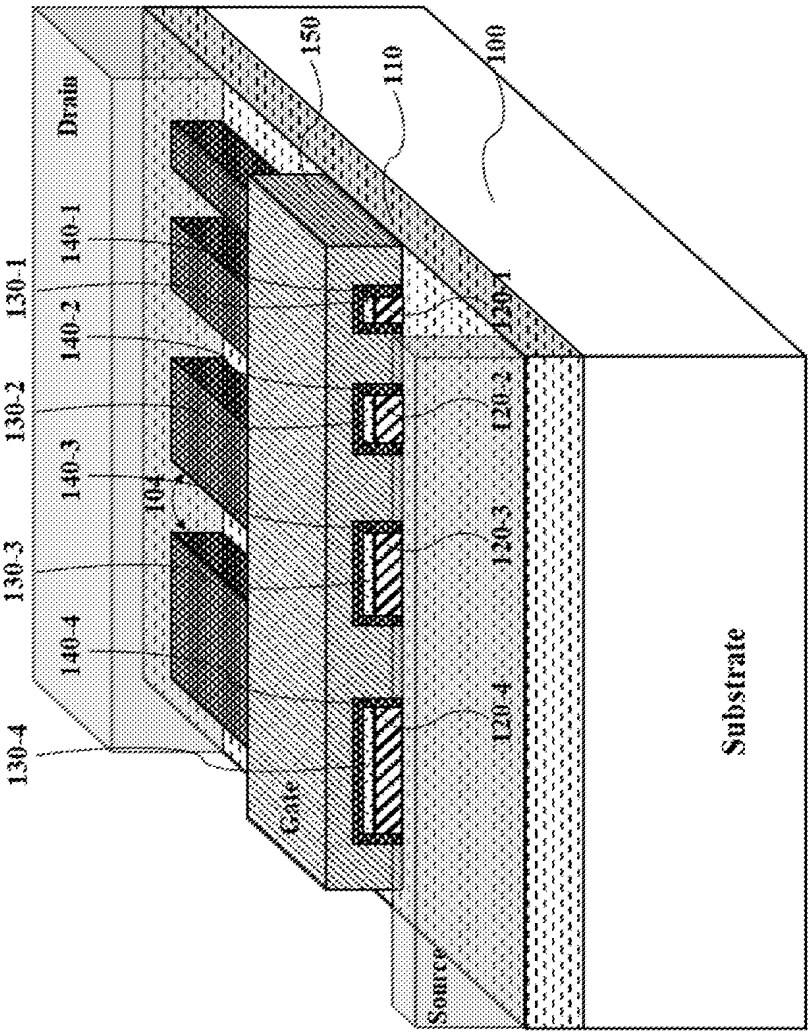

Drain
Gate
Source
Substrate
150
110
100
130-1
130-2
130-3
130-4
140-1
140-2
140-3
140-4
120-1
120-2
120-3
120-4
104

Figure 15B

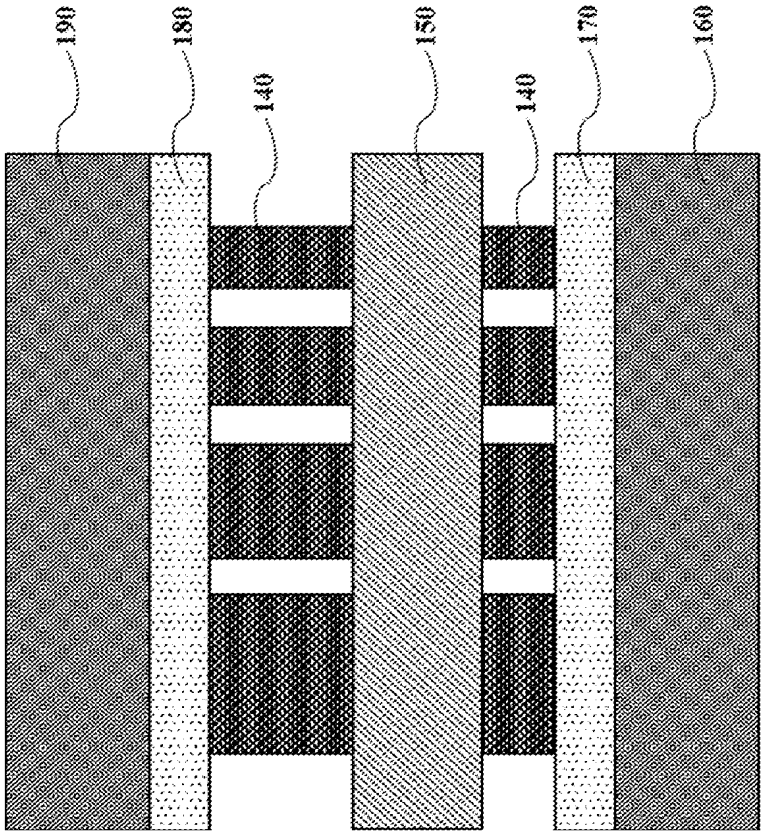


Figure 15C

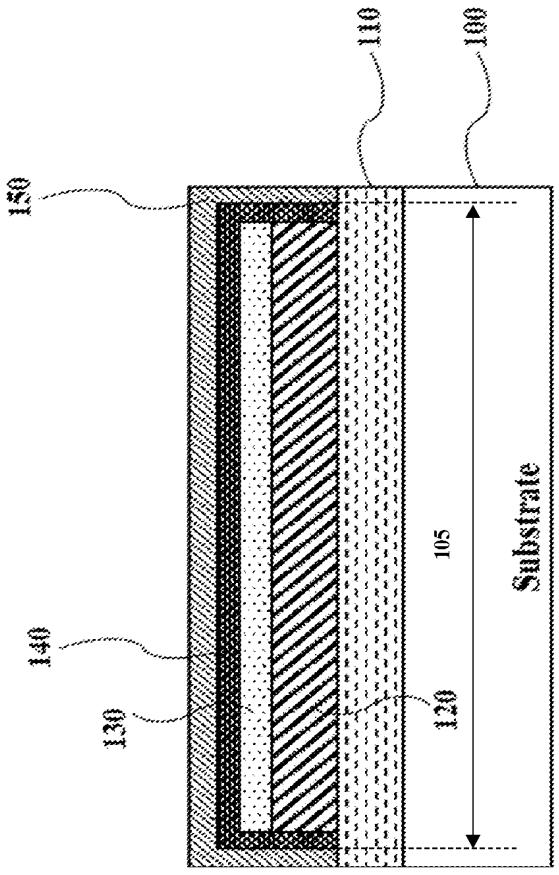


Figure 16A

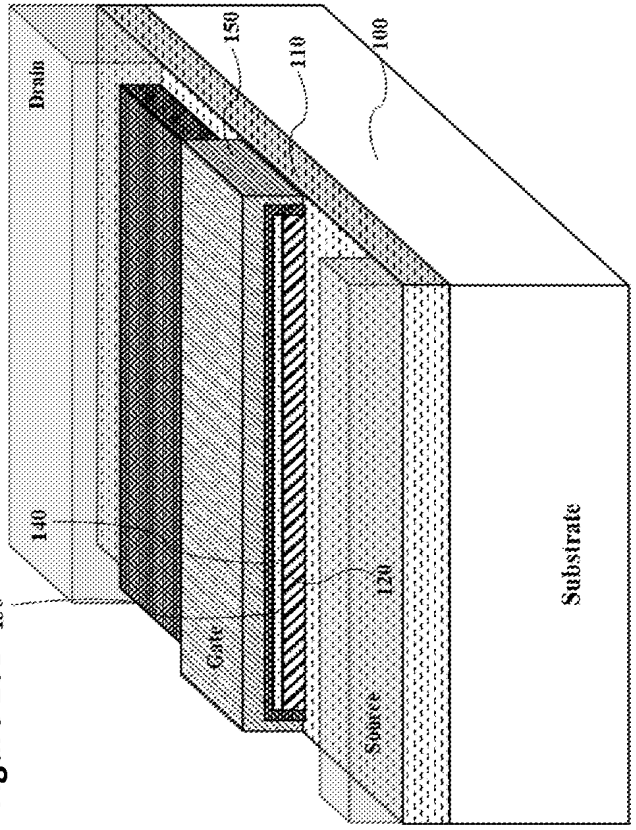


Figure 16B

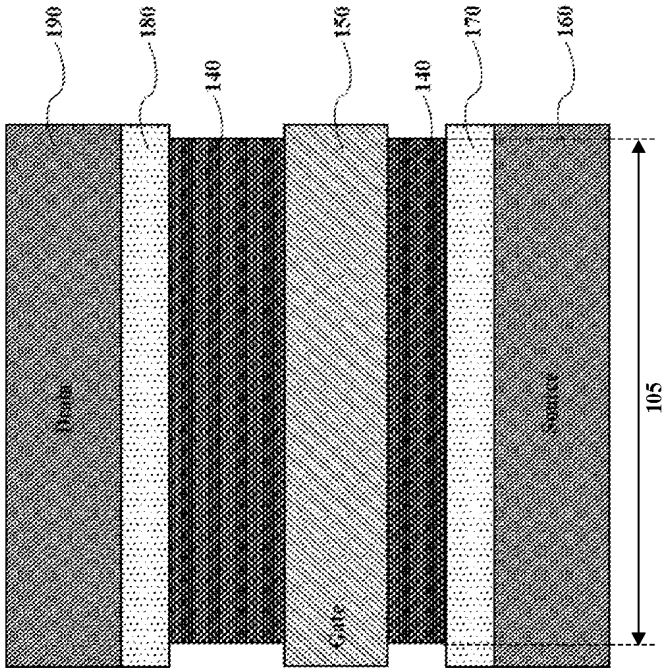


Figure 16C

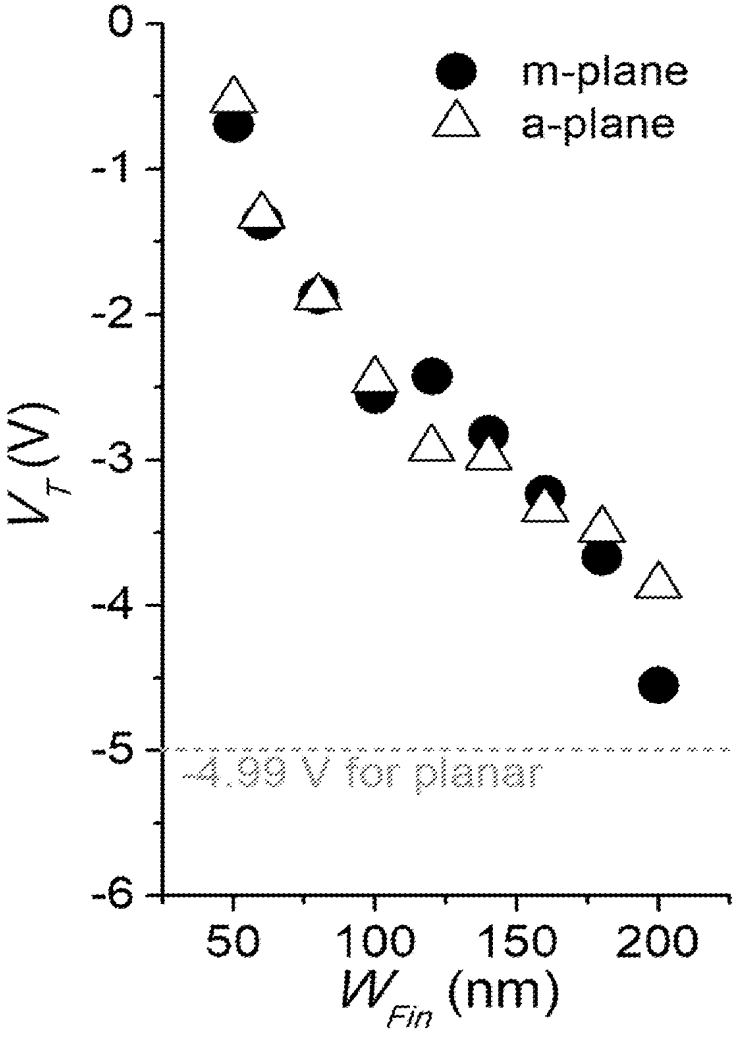

0
-1
-2
-3
-4
-5
-6
V_T (V)
m-plane
a-plane
-4.99 V for planar
50
100
150
200
W_{Fin} (nm)

Figure 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US18/58407

A. CLASSIFICATION OF SUBJECT MATTER
IPC - H01L 29/02, 29/778, 29/78, 27/092 (2018.01)
CPC - H01L 29/02, 29/66, 29/66045, 29/66462, 29/7786, 29/78, 21/823821, 27/0924, 27/0886

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/0066018 A1 (PARK, T et al.) 22 March 2007; the entire document	1-15
A	US 2014/0367796 A1 (TONER, B et al.) 18 December 2014; the entire document	1-15
A	US 2010/0187575 A1 (BAUMGARTNER, P et al.) 29 July 2010; the entire document	1-15
A	US 2015/0249134 A1 (INFINEON TECHNOLOGIES AUSTRIA AG) 3 September 2015; the entire document	1-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2018 (15.12.2018)	16 JAN 2019
Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)