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(71) Applicant: **THE REGENTS OF THE UNIVERSITY OF CALIFORNIA** [US/US]; 1111 Franklin Street, 12th Floor, Oakland, California 94607 (US).

(72) Inventors: **FORMAN, Charles**; 796 Juniper Walk, Apt. F, Golets, California 93117 (US). **LEE, SeungGeun**; 119 Dearborn Pl., Unit 138, Goleta, California 93117 (US). **YOUNG, Erin**; 1312 Robbins Street, Santa Barbara, California 93101 (US). **KEARNS, Jared**; 6520 El Colegio Rd., #2130, Santa Barbara, California 93106 (US). **DENBAARS, Steven P.**; 283 Elderberry Drive, Goleta, California 93117 (US). **SPECK, James S.**; 722 Monte Drive, Santa Barbara, California 93110 (US). **NAKAMURA, Shuji**; P.O. Box 61656, Santa Barbara, California 93160 (US).

(74) Agent: **SERAPIGLIA, Gerard B.**; GATES & COOPER LLP, 6060 Center Drive, Suite 830, Los Angeles, California 90045 (US).

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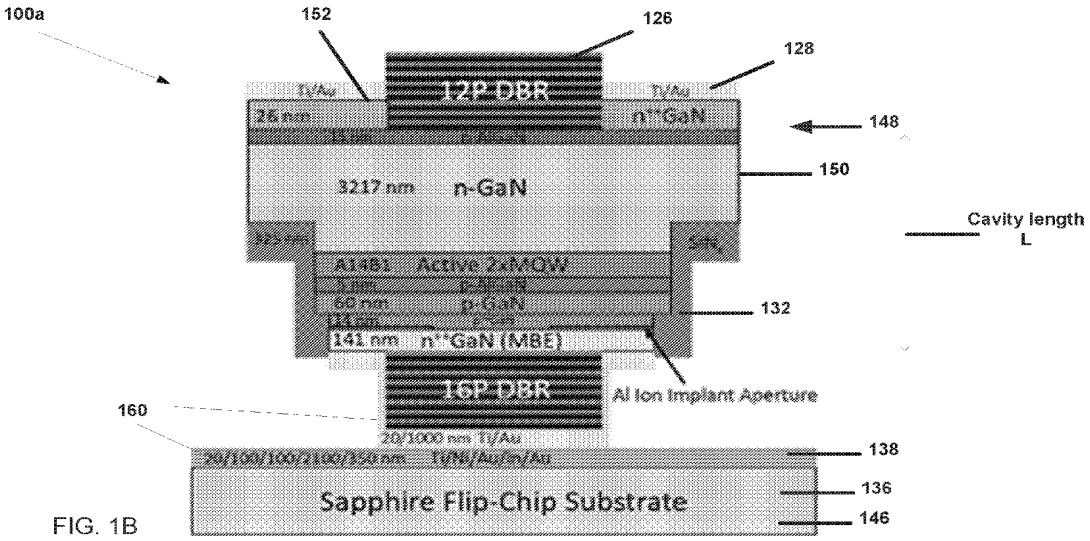

FIG. 1B

(57) Abstract: A Vertical Cavity Surface Emitting Laser (VCSEL) including a light emitting III-nitride active region including quantum wells (QWs), wherein each of the quantum wells have a thickness of more than 8 nm, a cavity length of at least 7λ *or* at least 20 λ, where lambda is a peak wavelength of the light emitted from the active region, layers with reduced surface roughness, a tunnel junction intracavity contact. The VCSEL is flip chip bonded using In-Au bonding. This is the first report of a VCSEL capable of continuous wave operation.

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III-NITRIDE SURFACE-EMITTING LASER AND METHOD OF FABRICATION

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit under 35 U.S.C. Section 119(e) of the following co-pending and commonly-assigned U.S. Provisional Patent Application No. 62/566,843, filed October 2, 2017, by Charles Forman, SeungGeun Lee, Erin Young, Jared Kearns, Steven P. DenBaars, James S. Speck, and Shuji Nakamura, entitled "III-NITRIDE SURFACE-EMITTING LASER AND METHOD OF FABRICATION," Attorney's Docket No. 30794.662-US-P1 (2018-250);

which application is incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to A Vertical Cavity Surface Emitting Laser (VCSEL) and a method of making the same.

2. Description of the Related Art.

(Note: This application references a number of different publications as indicated throughout the specification by one or more reference numbers within brackets, e.g., [x]. A list of these different publications ordered according to these reference numbers can be found below in the section entitled "References." Each of these publications is incorporated by reference herein.)

Vertical-cavity surface-emitting lasers (VCSELs) are semiconductor laser diodes that emit light normal to the substrate. This design has many advantages over edge-emitting lasers and light-emitting diodes, such as low threshold current, circular mode profile, high-speed direct modulation, ability for single longitudinal mode operation, and two-dimensional arraying capability [1]. As opposed to arsenide and phosphide-based

devices, electrically-injected III-nitride VCSELs have been relatively difficult to create, and only eight research groups have successfully demonstrated these devices in the past decade [2]–[26]. While most of the reports have been on *c*-plane, *m*-plane VCSELs have been demonstrated [4], [10], [12], [15], [24] and have many advantages, such as lack of the quantum confined Stark effect, higher material gain, and anisotropic gain that leads to 100% polarization ratio. III-nitride-based devices emit at wavelengths in the ultraviolet and visible spectrum which leads to novel applications in solid-state lighting, visible light communication, displays, projectors, and sensors. However, *m*-plane VCSEL devices have not been able to achieve continuous wave operation. The present invention satisfies this need.

SUMMARY OF THE INVENTION

To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding this specification, embodiments of the present invention disclose a VCSEL bonded to a flip chip substrate using Au-In solid-liquid interdiffusion (SLID) bonding. The SLID bonding solved a cracking problem discovered previous VCSEL devices formed using Au-Au thermocompression bonding and greatly improved VCSEL yield (as the SLID was conducted at lower temperatures and bonding forces). Furthermore, the SLID bonding enabled a much thicker metal pathway for heat transport so that continuous wave operation of the VCSEL could be achieved.

In further embodiments, the III-Nitride VCSEL included an active region that has thick quantum wells (QWs) (e.g., thickness > 8 nm or >9nm). Thicker QWs are possible on semipolar or nonpolar m-plane GaN, in contrast with standard c-plane GaN.

An embodiment of the invention was demonstrated and achieved continuous-wave (CW) operation at room temperature. The embodiment is a dual-dielectric DBR m-plane VCSEL with MBE-grown tunnel junction contact and ion implanted aperture

(similar to reference [5]), having an active region comprising a 2 period multi quantum well (MQW) with 14 nm QWs and a 1 nm barrier. Improved thermal performance and yield for this device structure was achieved using indium-gold flip-chip bonding (instead of gold-gold bonding). The embodiment has a longer cavity length (23λ instead of 7λ, where λ is the wavelength of light emitted by the VCSEL) and was fabricated using improved Molecular Beam Epitaxy (MBE) regrowth conditions and by removing an oxide residue after photoelectrochemical (PEC) etching.

However, the VCSEL can be embodied in many ways, including but not limited to, the following examples.

1. A VCSEL on a mount (e.g., flip chip substrate); and a thermally conductive bond between the mount and the VCSEL, the bond comprising a layer of metal having a thermal conductivity such that heat, generated during operation of the VCSEL, is transferred from the VCSEL to the mount and the VCSEL emits continuous wave electromagnetic radiation.

2. The device of example 1, wherein the thermally conductive bond comprises no cracks or fewer cracks than a bond between the VCSEL and the mount formed using Au-Au thermal compression bonding.

3. The device of one or any combination of the previous examples, wherein the thermally conductive bond comprises metal formed from a liquid metal phase.

4. The device of one or any combination of the previous examples, wherein the VCSEL is bonded to the mount by solid-liquid interdiffusion bonding (e.g., realized by short liquid phase of one low melting metal and immediate solidification caused by diffusion and intermixing with a second high melting point metal, generating the intermetallic phase).

5. The device of one or any combination of the previous examples, wherein the VCSEL comprises a first mirror and a second mirror defining a cavity for the

electromagnetic radiation, and the VCSEL is bonded to the mount by forming the bond comprising a metal layer, in a liquid state, around the first mirror.

6. The device of one or any combination of the previous examples, wherein: the VCSEL comprises a first mirror and a second mirror defining a cavity for the electromagnetic radiation, the bond comprises a metal layer, and one of the first mirror or the second mirror is embedded in the metal layer.

7. The device of one or any combination of the previous examples, wherein the VCSEL comprises a first mirror and a second mirror defining a cavity for the electromagnetic radiation, and the bond comprises a metal layer cast around the first mirror or the second mirror acting as a mold for the metal layer.

8. The device of one or any combination of the previous examples, wherein the bond comprises an intermetallic compound having a solid phase containing two or more metallic elements.

9. The device of one or any combination of the previous examples, wherein the bond comprises a first metal diffused into a second metal so as to intermix with a second metal, the first metal having a lower melting point than the second metal.

10. The device of one or any combination of the previous examples, wherein first metal comprises indium and the second metal comprises gold.

11. The VCSEL of one or any combination of the previous examples, comprising a light emitting III-nitride active region including quantum wells (QWs), wherein each of the quantum wells have a thickness of more than 8 nm.

12. The VCSEL of example 11, wherein the thickness of the quantum wells is in a range of 8-20 nm.

13. The VCSEL of one or any combination of the previous examples, wherein active region has a nonpolar or semipolar crystal orientation.

14. The VCSEL of one or any combination of the previous examples, wherein the VCSEL has a cavity length of at least 7 λ, where λ is a peak wavelength of light

emitted from the active region when the light is in the active region and the peak wavelength is the wavelength of the light having the highest intensity

15. The VCSEL of example 4, wherein the cavity length is in a range of $20\lambda - 100\lambda$.

16. The VCSEL of one or any combination of the examples 1-5, wherein the VCSEL further includes the active region between a first III-nitride n-type layer and a III-nitride p-type layer, a second III-nitride n-type layer forming a tunnel junction with the III-nitride p-type layer, a contact layer for the tunnel junction, and a top surface of the contact layer having a root mean square surface roughness (RMS) of less than 2 nanometers (nm) when the VCSEL is a nonpolar device or less than 1 nm when the VCSEL is a semipolar device.

17. The VCSEL of one or any combination of the previous examples, wherein the active region is between a III-nitride n-type layer and a III-nitride p-type layer, an n-side surface of the III-nitride layer is exposed after etching to at least partially remove the substrate on which the active region was grown, and the n-side surface is surface treated and has an RMS surface roughness less than 1 nm.

18. The VCSEL of examples 16 or 17, wherein the surface roughness is over a 5 μm x5 μm, a 1 μm x 1μm, or 10 μm x 10 μm area.

19. The VCSEL of example 16-17, wherein the surface treatment removes an oxide residue after the etching.

20. The VCSEL of one or any of the examples 1-19, further comprising: a mirror; a metal layer on the mirror; a flip chip substrate; a bonding layer including gold on the flip chip substrate; a bonded interface between the bonding layer and the metal layer, wherein the bonded interface includes indium bonded to the gold.

21. The device of any of the preceding examples, further comprising a first charge injection layers coupled to a light emitting active region, wherein the active region

emits the light in response to electrons and holes injected into the active region through charge injection layers.

22. A VCSEL comprising a light emitting III-nitride active region including quantum wells (QWs), wherein each of the quantum wells have a thickness of more than 8 nm.

23. The VCSEL of example 22, in combination with one or any combination of examples 1-10 or 11-21.

24. A method of fabricating a Vertical Cavity Surface Emitting Laser (VCSEL) structure, comprising growing a sacrificial layer on a semipolar or nonpolar III-nitride substrate; growing a III-nitride VCSEL structure including an active region between an n-type layer and a p-type layer, wherein the active region includes a quantum well having a thickness greater than 8 nm; at a temperature of less than 750°C, growing a tunnel junction structure on the p-type III-Nitride using an indium surfactant; depositing a mirror on a p-type side of the VCSEL structure; covering sidewalls of the active region with a dielectric layer; depositing metal on the mirror; flip chip bonding a flip chip substrate to the metal on the mirror using solid-liquid interdiffusion bonding, and photoelectrochemically etching the sacrificial layer so as to at least partially remove the nonpolar or semipolar III-nitride substrate; and removing, using a surface treatment, a rough residue on an n-type side of the VCSEL structure or on the surface of the n-type layer exposed during the etching.

25. The method of example 24, wherein the removing comprises treating the surface with Tergitol detergent or KOH.

26. The method of examples 24 or 25, wherein: the VCSEL structure is grown with a cavity length of at least 7 λ, where λ is a peak wavelength of light emitted from the active region when the light is in the active region; and the peak wavelength is the wavelength of the light having the highest intensity.

27. The method of examples 24, 25, or 26 wherein a surface of the n-type layer has a root mean square (RMS) surface roughness of less than 1 nm after the surface treatment.

28. The method of example 27, wherein the surface roughness is over a 5 μm x5 μm, a 1 μm x 1μm, or 10 μm x 10 μm area.

30. The method of any of the examples 24-28, wherein the VSCEL emits continuous wave electromagnetic radiation.

31. A VCSEL emitting continuous wave electromagnetic radiation.

32. The VCSEL of example 31, wherein the VCSEL comprises III-nitride.

33. A Vertical Cavity Surface Emitting Laser (VCSEL), comprising:

a light emitting III-nitride active region including quantum wells (QWs), wherein each of the quantum wells have a thickness of more than 8 nm.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIG. 1A. Schematic of the III-nitride VCSEL structure before the flip-chip bonding.

FIG. 1B. The complete structure after processing.

FIG. 2. Process flow for fabricating device of FIG. 1B.

FIG. 3. Example bonding process flow.

FIG. 4A Photodetector measurement of pulsed *I-V* and *I-L* curves of a VCSEL with a 6 μm aperture diameter and 23λ cavity length. The I_{th} was 12 mA (42.4 kA/cm^2) and the maximum output power was 700 μW.

FIG. 4B. *I-V* and *I-L* curves generated by integrating the spectrometer intensity. By aligning the spectrometer fiber optic to the lasing peak, the measured spontaneous emission below threshold is greatly reduced compared to the large-area photodetector measurement.

FIGs. 5A-5B. Spectrum under pulsed operation of a VCSEL with a 6 μm aperture diameter and 23λ cavity length (FIG. 5A) near the threshold current and (FIG. 5B) for currents up to 42.1 mA.

FIGs. 6A-6B. CW operation of a VCSEL with a 6 μm aperture diameter and 23λ cavity length showing (FIG. 6A) *I-V* and *I-L* curves and (FIG. 6B) the spectrum at different currents.

FIGs. 7A-7B. Optical microscope images of VCSEL aperture as a function of current at (FIG. 7A) low integration time and (FIG. 7B) higher integration time.

FIG. 8. Spectrum under CW operation for a VCSEL with a 6 μm aperture diameter and 23λ cavity length. The spontaneous emission envelope redshifts with increasing current.

FIG. 9. Thermal modeling of a VCSEL bonded to a flip-chip substrate using Au-Au thermocompression bonding.

FIG. 10. FIB cross-sectioning revealing cracks in the metal contact in the VCSEL bonded to a substrate using Au-Au thermocompression bonding.

FIG. 11A and FIG. 1B. Thermal modelling shows that cracks in that metal contact in the VCSEL bonded to substrate severely impairs the thermal performance.

FIG. 12. Image of VCSEL bonded to flip chip substrate using Au-In solid-liquid interdiffusion (SLID) bonding

FIG. 13. Au-In phase diagram.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Technical Description

The present disclosure describes a III-nitride VCSEL with a tunnel junction intracavity contact and ion implanted aperture, as shown in FIGs. 1(a)-1(b).

Fig. 1A illustrates the VCSEL structure 100 prior to flip chip bonding comprises a substrate 102, a sacrificial layer 104 on or above the substrate 102, an n-type layer 106 on or above the sacrificial layer 104, an etch stop layer 108 on or above the n-type layer 106, an n-type layer 110 on or above the etch stop layer 108, an active layer 112 on or above the n-type layer 110, an electron blocking layer 114 on or above the active layer 112, a p-type layer 116 on or above the electron blocking layer 114, a p^{++}-type layer 118 (having a higher p-type dopant concentration than the p-type layer 116) on or above the p-type layer 116, an n-type layer 120 on or above the p^{++}- type layer 118, a mirror 122 on or above the n-type layer 120, and a metal layer 124 on or above the n-type layer 120.

Fig. 1B illustrates the VCSEL 100b after processing, comprising a second mirror 126 on or above the etch stop layer 108, the etch stop layer 108 on or above the n-type layer 106, a second metal layer 128 on or above the n-type layer 106, the n-type layer 110 on or above the etch stop layer 112, the active layer 114 on or above the n-type layer 110, the electron blocking layer 114 on or above the active layer 112, the p-type layer 118 on or above the electron blocking layer 114, the p^{++}-type layer 118 (having a higher p-type dopant concentration than the p-type layer 120) on or above the p-type layer 116, the n-type layer 120 on or above the p^{++}- type layer 118, the first mirror 122 on or above the n-type layer 120, and the first metal layer 124 on or above the n-type layer 120.

Both the structure 100 and VCSEL 100b also include a current aperture 130 and dielectric layer 132 on the sidewall 134.

The following sections describe key design changes and main performance improvements enabled by the present invention, as compared to the *m*-plane VCSEL

reported in [10]. As a result, the present disclosure is the first report of an *m*-plane VCSEL that lases under continuous-wave (CW) operation at room temperature.

A. Improved active region design with thicker quantum wells

The present invention discloses the use of thicker quantum wells (e.g., 2xMQW: 14 nm QWs and 1 nm barriers) as compared to the 7xMQW with 3 nm QWs and 1 nm barriers) described in [10]. A key improvement resulting from the use of thicker QWs includes a higher gain enhancement factor: thicker QWs have more active gain medium aligned with the optical field, meaning that the modal gain is increased with the thicker QWs. Well thickness examples used herein are the widest QW thickness reported for III-nitride VCSELs because most reports are on *c*-plane which restricts the thickness because of the quantum confined Stark Effect (QCSE). *m*-plane oriented QWs allow for much thicker QWs due to the lack of QCSE.

B. Improved flip-chip bonding using indium-gold (In-Au) bonding instead of Au-Au bonding

In one or more embodiments, flip chip bonding using (In-Au) is used instead of Au-Au bonding as described in [10]. Prior *m*-plane VCSELs were not able to achieve CW operation due to poor thermal performance. The main pathway for heat transport is through the thin metal contact that goes around the bottom dielectric Distributed Bragg Reflector (DBR) to the flip-chip substrate. Cross-section SEM analysis of the Au-Au bonded device reveals that there are cracks and voids in the main metal pathway for heat transport, which likely prevents CW operation. Cracks and voids were caused by the high temperature and pressure required for Au-Au bonding.

Key improvements resulting from using In-Au bonding:

- In-Au bonding can be conducted at significantly lower force and temperature compared to Au-Au bonding.

- In-Au bonded devices have fewer cracks, and there is a much more robust pathway for heat transport in the In-Au bonded devices.

As a result, the use of In-Au bonding improves the thermal performance to enable CW VCSEL operation.

C. Longer cavity length

In one or more examples, the VCSEL has a cavity longer than 7λ (e.g., 23λ instead of 7λ).

Heat generated in the active region cannot flow directly down to the flip-chip substrate due to the thermally-insulating bottom dielectric DBR. The main pathway for heat flow is through the thin metal contact on the p-side that goes around the bottom DBR.

COMSOL thermal modeling shows that increasing the cavity length greatly improves the thermal performance. GaN has a thermal conductivity of 130W/mK, so increasing the cavity length aids heat distribution throughout the cavity and results in lower active region temperatures. Thicker cavity lengths also have a smaller resonant mode spacing, which ensures the alignment of a resonant mode with the gain spectrum. This is particularly helpful during CW operation as the gain spectrum redshifts considerably.

D. Improved MBE/MOCVD tunnel junction regrowth.

In one or more embodiments, the VCSEL includes an MBE tunnel junction regrowth with indium surfactant at a lower growth temperature (e.g., growth at less than 750°C). In one or more examples, the tunnel junction regrowth temperature is at 740°C. Reference [10] describes 750°C growth without indium surfactant.

Key improvements resulting from the growth with indium surfactant:

- Molecular Beam Epitaxy (MBE) regrowth optimization experiments show that slightly lower growth temperatures improved the electrical characteristics and the addition of an indium surfactant improved the surface morphology.
- The root mean square (RMS) roughness of the MBE tunnel junction regrowth was 1.5 to 2 nm for the demonstrated CW VCSEL

This design resulted in a lower series resistance and lower turn-on voltage, which is conducive for CW operation

Maintaining a smooth surface morphology is crucial for VCSELs to minimize scattering loss. In addition to scattering loss, roughness reduces the reflectance of the DBRs because the roughness propagates throughout the DBRs. Ideally, the RMS roughness should be less than 1 nm or at least less than 6 nm (devices having a 6 nm RMS roughness did not reach the threshold for lasing), e.g., over a 5 μm x5 μm, a 1 μm x 1μm, or 10 μm x 10 μm area.

MBE regrowth is relatively rough on m-plane, but it is much smoother on semipolar orientations. Therefore, semipolar orientated VCSELs could be fabricated. Another way to get a smooth surface on m-plane is metal organic chemical vapor deposition (MOCVD) tunnel junction regrowth.

E. Removal of oxide residue after PEC undercut etching

A rough oxide residue was discovered on the GaN surface after PEC undercut etching to remove the native *m*-plane GaN substrate. Conventional designs [10] did no treatment to remove residual oxide.

The presence of a rough oxide layer could explain some of the problems of previous designs [10].

- Previous devices [10] had a higher voltage, which could be attributed to the n-electrode contacting the oxide residue.

- Previous devices [10] exhibited filamentary lasing, which could be explained by the presence of a nonuniform oxide residue in the aperture.

The CW VCSEL described herein has less than 1 nm root mean square (RMS) roughness on the n-side after removing the PEC oxide residue. The most effective method to remove the residue was to submerge the sample in Tergitol detergent and gently swipe the sample with a foam swab.

This method was performed on the VCSEL described herein.

Other methods of residue removal include submerging the sample in (or treating the sample with) aqueous KOH (i.e. 45% KOH for 30 min). Lower molarity KOH can be used if it is heated. This removes most of the residue, which indicates that the residue is likely a form of gallium oxide remaining after PEC etching. Although most of the residue could be removed with KOH, there were remaining cube-like features that could not be removed using KOH. These features are likely indium oxide or indium hydroxide and could be removed by swabbing in Tergitol. Other methods of residue removal include treating the sample in HCl

Key improvements observed after removing the oxide residue include:

- Smooth surfaces on the n-side with less than 1 nm RMS roughness (e.g., over a 5 μm x5 μm, a 1 μm x 1μm, or 10 μm x 10 μm area).
- Improved (reduced) turn-on voltage and series resistance.
- Elimination of filamentary lasing and the observation of a well-defined lateral optical mode.

F. Steps to fabricate the device

a. Example method

FIG. 2 illustrates a method of fabricating a VCSEL, referring also to Fig. 1A and Fig. 1B.

Block 200 represents obtaining a substrate 102 (e.g., a III-nitride substrate such as a GaN substrate). For the devices 100b measured in the results section G, the substrate 102 comprising an *m*-plane GaN substrate with a miscut of 1° in the negative *c*-direction was used.

Block 202 represents optionally growing a template layer (e.g., GaN template) on or above the substrate 102. For the devices measured in the results section G, the template is a GaN layer having a thickness of 1264.6 nm.

Block 204 represents growth of one or more sacrificial layers 104 on the template. In one example, the sacrificial layer is a single quantum well. In another other example, the sacrificial layer comprises a multi quantum well (MQW). For the devices measured in the results section G, sacrificial 3 period MQW ($absorption\ \lambda = 415$ nm) including 5 nm QWs and 7 nm barriers were grown on the template.

Block 206 represents growth of the n-type layer 106 (e.g., n^{++}GaN or n^{++}-type III-nitride having higher n-type dopant concentration than n-type layer 110) on or above the sacrificial layer 104. For the devices 100b measured in the results section G, the n^{++}-GaN layer had a thickness of 26 nm.

Block 208 represents depositing the etch stop layer 108 (e.g., n-type AlGaN layer or n-AlGaN). For the devices 100b measured in the results section G, the etch stop layer 108 is an n-AlGaN layer having a thickness of 15 nm on the n^{++}-GaN layer of Block 206.

Block 210 represents depositing a first n-type III-nitride layer 110 (e.g., n-GaN or n-type GaN) on the etch stop layer 108 (e.g., n-AlGaN_.

Block 212 represents depositing an active region comprising a III-nitride active layer 112 on the first III-nitride layer 110. Examples include, but are not limited to, the III-nitride layer including one or more InGaN/GaN QWs. For the devices measured in the results section G, the active region is a two period InGaN/GaN MQW including 14 nm thick QWs and 1 nm barriers, and wherein the Indium and Gallium compositions are such that the QWs have a bandgap such that peak absorption of the QWs is at a wavelength of

405 nm. In one or more examples, the QWs have a thickness of at least 8nm, e.g., in a range of 8-20 nm.

Block 214 represents optionally depositing an electron blocking layer 114 (e.g., p-type AlGaN or p-AlGaN) on the active region (e.g., III-nitride layer 112). For the devices measured in the results section G, the electron blocking layer 114 is a p-AlGaN layer having a thickness of 5 nm.

Block 216 represents depositing a p-type layer 116 (e.g., p-type III-nitride layer such as p-GaN) on the electron blocking layer 114 (e.g., p-AlGaN). For the devices measured in the results section G the p-GaN layer has a thickness of 62 nm.

Block 218 represents depositing a p^{++}-type layer 118 (e.g., p^{++}-GaN layer) on the p-type layer 116 (e.g., p-GaN). For the devices measured in the results section G, the p^{++}-GaN layer has a thickness of 14 nm.

Block 220 represents optionally performing photoluminescence to check the wavelength and quality of the active region.

Block 222 represents annealing the grown structure to activate the p-GaN. For the results presented herein, the structure was thermally annealed at 600 °C for 15 min.

Block 224 represents optionally performing electroluminescence using soldered indium contacts to check the light output power, wavelength, full width at half maximum (FWHM), and voltage characteristics of the device structure.

Block 226 represents removing the indium contacts, if necessary. For the devices measured in the results section G, aqua regia was used to remove the indium contacts.

Block 228 represents etching to expose the sidewalls 134 of the active region (in order to later deposit dielectric 132 (e.g., SiN_x) on the sidewalls to protect the active region during PEC etching). For the devices measured in the results section G, a dry etch was performed to expose the sidewall 134 of the III-nitride active layer 112 comprising a MQW.

Block 230 represents depositing a mask defining a current aperture 130 in the device structure 100. For the devices 100b measured in the results section G, a Ti/Au

hardmask was deposited over the aperture and aluminum ion implantation was performed to serve as the current aperture.

Block 232 represents removing the mask. For the devices measured in the results section G, the Ti/Au hardmask was removed using aqua regia.

The layers deposited to this point were grown by MOCVD.

Block 234 represents growing a tunnel junction intracavity contact 120a by molecular beam epitaxy (MBE) (e.g., n^{+}-GaN layer between n^{++}-GaN layers). For the devices measured in the results section G, the following sequence of layers were grown by MBE: n^{++}GaN layer (1E19 cm^{-3} doping concentration, 39.5972 nm thick; followed by n^{+}GaN (2.5E18 cm^{-3} doping concentration, 61.7376 nm thick); followed by n^{++}GaN (1.1E20 cm^{-3} doping concentration 39.5972 nm thick), wherein the top most final layer is the contact layer (n^{++}GaN) for the tunnel junction.

Block 236 represents etching (e.g., dry etching) to remove the MBE regrown material deposited on the sidewall (when growing contact 120) to prevent a current leakage path. For the devices measured in the results section G, a dry etch was performed.

Block 238 represents depositing a protection layer 132 (e.g., dielectric such as SiNx, silicon nitride) on the sidewalls 134. For the devices measured in the results section G, Ion beam deposition (IBD) was used to deposit the protection layer 132 comprising SiN_x on the sidewall so as to protect the sidewall 134 of the active region (so that the active region does not etch during PEC etching during native *m*-plane GaN substrate removal).

Block 240 represents depositing a mirror 122 (e.g., distributed bragg reflector DBR) on the p-side/p-type side 170 of the device structure 100. For the devices measured in the results section G, IBD was used to deposit a 16-period (16P) SiO_2/Ta_2O_5 (66.8/45.6 nm) DBR on the p-side.

Block 242 represents etching to expose the sidewalls 140 of the sacrificial layer 104 comprising the MQW. For the devices measured in the results section G, a dry etch was performed to expose the sidewalls 142 of the sacrificial MQW.

Block 244 represents depositing a p-type contact (p-contact) 124 and cathode 144 for the PEC etching. For the devices measured in the results section G, 20nm/1000 nm Ti/Au was deposited to serve as both the p-contact 124 and as the cathode 144 for PEC etching.

Block 246 represents preparing the flip chip substrate 136 (e.g., sapphire). For the devices measured in the results section G, the metal layer 138 comprising 20nm/100nm/100nm/15000nm/100 nm Ti/Ni/Au/In/Au was deposited on double-side polished sapphire 146 to serve as the flip-chip substrate 136. The purpose of the uppermost 100 nm Au layer of the metal layer 138 was to prevent indium oxidation (indium readily diffuses into the gold layer to form $AuIn_2$ as-deposited).

Block 248 represents flip-chip bonding the flip chip substrate 136 to the grown epitaxial structure 100 under appropriate conditions. For the devices measured in the results section G, flip chip bonding was conducted with the following conditions: temperature of 210 °C, 30 Newtons force, for 300 seconds. The step may comprise selecting a metal alloy system that had a low melting temperature sufficient for the bonding process.

Block 250 represents native substrate 100 removal. For the example illustrated in FIG. 1B, the native GaN substrate was removed by performing PEC etching to selectively etch the sacrificial MQW. For the devices measured in the results section G, PEC etching was performed using 1M KOH and a 390 nm LED array.

Block 252 represents removing a rough residue (likely gallium oxide) that appears after PEC undercut etching. For the devices measured in the results section G, swabbing the sample in Tergitol detergent was performed to remove the rough residue from n-side surface(s) 150, 152 of the n-GaN. Submerging the sample in KOH can also remove most of the oxide.

Block 254 represents depositing the n-contact 128. For the devices 100a measured in the results section G, 10/500 nm Ti/Au was deposited to serve as n-contact.

Block 256 represents depositing a mirror 126 (e.g., DBR) on the n-side 148 of the device 100a. For the devices 100a measured in the results section G, a 12-period SiO_2/Ta_2O_5 (66.8/45.6 nm) DBR was deposited on the n-side 148 using IBD.

Block 258 represents the end result, a VCSEL 100a (e.g., as illustrated in FIG. 1B).

b. Exemplary Embodiments

Steps can be added or omitted so that the VCSEL 100 can be embodied in many ways including, but not limited to, the following examples (referring to FIG. 1A, FIG. 1B, and FIG. 12).

1. A VCSEL 100a on a mount (e.g., flip chip substrate 136); and a thermally conductive bond 160, 1200 between the mount and the VCSEL 100a, the bond 160, 1200 comprising a layer 138 of metal having a thermal conductivity such that heat, generated during operation of the VCSEL, is transferred from the VCSEL to the mount and the VCSEL emits continuous wave electromagnetic radiation.

2. The device 100a of example 1, wherein the thermally conductive bond 160, 1200 comprises no cracks or fewer cracks than a bond between the VCSEL and the mount formed using Au-Au thermal compression bonding.

3. The device 100a of one or any combination of the previous examples, wherein the thermally conductive bond 160, 1200 comprises metal formed from a liquid metal phase.

4. The device 100a of one or any combination of the previous examples, wherein the VCSEL 100a is bonded to the mount by solid-liquid interdiffusion bonding (e.g., realized by short liquid phase of one low melting metal (e.g., indium) and immediate solidification caused by diffusion and intermixing with a second high melting point metal (e.g., gold), generating the intermetallic phase).

5. The device 100a of one or any combination of the previous examples, wherein the VCSEL comprises a first mirror 122 and a second mirror 126 defining a

cavity for the electromagnetic radiation emitted from the VCSEL, and the VCSEL 100a is bonded to the mount by forming the bond 160, 1200 comprising a metal layer 138, in a liquid state, around the first mirror 122. In one or more examples, the metal layer 138 is conformal with the first mirror 122.

6. The device of one or any combination of the previous examples, wherein: the VCSEL 100a comprises a first mirror 122 and a second mirror 126 defining a cavity for the electromagnetic radiation, the bond 160, 1200 comprises a metal layer 138, and one of the first mirror 122 or the second mirror 126 is embedded in the metal layer 138.

7. The device 100a of one or any combination of the previous examples, wherein the VCSEL comprises a first mirror 122 and a second mirror 126 defining a cavity for the electromagnetic radiation emitted from the VCSEL, and the bond 160, 1200 comprises a metal layer 138 cast around the first mirror 122 or the second mirror 126 acting, the first mirror 122 or second mirror 126 as a mold for the metal layer 138.

8. The device 100a of one or any combination of the previous examples, wherein the bond 160, 1200 comprises an intermetallic compound having a solid phase containing two or more metallic elements.

9. The device 100a of one or any combination of the previous examples, wherein the bond 160, 1200 comprises a first metal diffused into a second metal so as to intermix with a second metal, the first metal having a lower melting point than the second metal.

10. The device 100a of one or any combination of the previous examples, wherein first metal comprises indium and the second metal comprises gold.

11. The VCSEL 100a of one or any combination of the previous examples, comprising a light emitting III-nitride active region 112 including quantum wells (QWs), wherein each of the quantum wells have a thickness of more than 8 nm (however, thicknesses of less than 8 nm are also possible and achieve continuous wave emission of electromagnetic radiation).

12. The VCSEL of example 11, wherein the thickness of the quantum wells is in a range of 8-20 nm.

13. The VCSEL 100a of one or any combination of the previous examples, wherein active region 112 has a nonpolar or semipolar crystal orientation.

14. The VCSEL 100a of one or any combination of the previous examples, wherein the VCSEL has a cavity length L of at least 7 λ, where λ is a peak wavelength of light/electromagnetic radiation emitted from the active region when the light/electromagnetic radiation is in the active region and the peak wavelength is the wavelength of the light/electromagnetic radiation having the highest intensity.

15. The VCSEL 100a of example 14, wherein the cavity length L is in a range of $20\,\lambda - 100\lambda$.

16. The VCSEL 100a of one or any combination of the examples 1-15, wherein the VCSEL further includes the active region 112 between a first III-nitride n-type layer 110 and a III-nitride p-type layer 116, a second III-nitride n-type layer 120 forming a tunnel junction with the III-nitride p-type layer, the second III-nitride n-type layer including a contact layer for the tunnel junction, and a top surface 162 of the contact layer (or top surface 162 of layer 120) having a root mean square surface roughness (RMS) of less than 2 nanometers (nm) when the VCSEL is a nonpolar device or less than 1 nm when the VCSEL is a semipolar device.

17. The VCSEL 100a of one or any combination of the previous examples, wherein the active region 112 is between a III-nitride n-type layer 110 and a III-nitride p-type layer 116, an n-side surface 150, 152 of the III-nitride n-type layer 110, 106 is exposed after etching to at least partially remove the substrate 102 on which the active region 112/VCSEL structure 100 was grown, and the n-side surface 150, 152 is surface treated and has an RMS surface roughness less than 1 nm.

18. The VCSEL 100a of examples 16 or 17, wherein the surface roughness of surface 162 and/or surface 150, 152 is over a 5 μm x5 μm, a 1 μm x 1μm, or 10 μm x 10 μm area, (μm is micrometers).

19. The VCSEL 100a of example 16-17, wherein the surface treatment removes an oxide residue after the etching.

20. The VCSEL 100a of one or any of the examples 1-19, further comprising: a mirror 122; a metal layer 124 on the mirror 122; a flip chip substrate 136; a bonding layer 160, 1200 including gold on the flip chip substrate 136; a bonded interface between the bonding layer 160, 1200 and the metal layer 124, wherein the bonded interface includes indium bonded to the gold.

21. The device 100a of any of the preceding examples, further comprising a charge injection layers 110, 116 coupled to a light emitting active region 112, wherein the active region emits the light in response to electrons and holes injected into the active region through charge injection layers 110, 116 (electrons through layer 110 and holes through layer 116).

22. A VCSEL 100a comprising a light emitting III-nitride active region including quantum wells (QWs), wherein each of the quantum wells have a thickness of more than 8 nm.

23. The VCSEL 100a of example 22, in combination with one or any combination of examples 1-10 or 11-21.

24. A method of fabricating a Vertical Cavity Surface Emitting Laser (VCSEL) structure, comprising growing a sacrificial layer on a semipolar or nonpolar III-nitride substrate; growing a III-nitride VCSEL structure including an active region between an n-type layer and a p-type layer, wherein the active region includes a quantum well having a thickness greater than 8 nm; at a temperature of less than 750°C, growing a tunnel junction intracavity contact 120a on the p-type III-Nitride using an indium surfactant; depositing a mirror on a p-type side of the VCSEL structure; covering

sidewalls of the active region with a dielectric layer; depositing metal on the mirror; flip chip bonding a flip chip substrate to the metal on the mirror using solid-liquid interdiffusion bonding, and photoelectrochemically etching the sacrificial layer so as to at least partially remove the nonpolar or semipolar III-nitride substrate; and removing, using a surface treatment, a rough residue on an n-type side of the VCSEL structure or on the surface of the n-type layer exposed during the etching.

25. The method of example 24, wherein the removing comprises treating the surface with Tergitol detergent or KOH.

26. The method of examples 24 or 25, wherein: the VCSEL structure is grown with a cavity length of at least 7 λ, where λ is a peak wavelength of light emitted from the active region when the light is in the active region; and the peak wavelength is the wavelength of the light having the highest intensity.

27. The method of examples 24, 25, or 26 wherein a surface of the n-type layer has a root mean square (RMS) surface roughness of less than 1 nm after the surface treatment.

28. The method of example 27, wherein the surface roughness is over a 5 μm x5 μm, a 1 μm x 1μm, or 10 μm x 10 μm area.

29. The method of any of the examples 24-28, wherein the VSCEL emits continuous wave electromagnetic radiation.

30. The method or device of one or any combination of the previous examples 1-29, wherein the mirrors 122, 126 are thermally insulating and/or comprise a dielectric.

FIG. 1A shows the device structure prior to the flip-chip bond stage. After flip-chip bonding to a sapphire substrate, the native *m*-plane GaN substrate was removed via PEC etching. FIG. 1(b) shows the fully completed device. Although this device used sapphire as the flip-chip substrate, sapphire is not a good heat sink. Better options for the flip-chip substrates are copper, SiC, diamond, AlN, and other materials with high thermal conductivity.

In one or more examples, the VCSEL has a cavity length of at least 7 λ, in a range of 7 λ – 100 λ, or in a range of 20 λ – 100 λ, where λ is a peak wavelength of the light in the active region and emitted from the active region. In one or more embodiments, a VCSEL having the cavity length of at least 7 λ is capable of emitting continuous wave electromagnetic radiation.

c. Further Exemplary bonding method embodiment

FIG. 3 illustrates a method of fabricating a VCSEL according to one or more examples, comprising bonding a VCSEL to a mount using metal. The bonding comprises the following steps.

Block 300 represents providing a metal layer on the mount, the metal layer comprising a first metal and a second metal.

Block 302 represents heating the metal layer so that the first metal is in liquid metal state.

Block 304 represents positioning the VCSEL on the metal layer including the first metal in the liquid state.

Block 306 represents allowing the metal layer to solidify and form a bond between the VCSEL and the mount.

Block 308 represents the end result, a VCSEL on a mount. The VCSEL/method on the mount can be embodied in many ways including, but not limited to, the following examples.

1. The method wherein the VCSEL comprises a first mirror and a second mirror defining a cavity for electromagnetic radiation emitted from the VCSEL, and the positioning comprises positioning the first mirror on the metal layer using a force or pressure when the first metal layer is in the liquid metal state, so that the first metal layer is embedded in the metal layer after the metal layer has solidified.

2. The method of Example 1 wherein the steps 300-308 are implemented so that the VCSEL is bonded to the mount by solid-liquid interdiffusion bonding, the first metal comprises indium, and the second metal comprises gold.

3. The method resulting in the VCSEL on a mount according to one or any combination of Examples 1-21 in section F part b above entitled "Exemplary Embodiments."

In one example, the bonding metal layer 160, 1200 thickness that worked best was ~2 micrometers thick indium on the flip-chip substrate (and ~1 micron of Au on the GaN device). In one or more examples, the bottom DBR mirror is ~1.8 microns thick, so in one or more examples as 2 to 3 microns thickness of bonding metal 160, 1200 would enable the bottom DBR 122 to become completely embedded within metal. Thinner bonding metal thicknesses may also work in some examples but might result in a thinner pathway for heat transport.

G. Results and Characterization

The *I-L*, *I-V*, and spectrum were measured under both pulsed and CW operation. For a light-emitting diode with equivalent active region design, the pulsed spectrum was obtained at stage temperatures up to 60 °C to obtain the peak emission wavelength shift with increasing temperature.

VCSELs achieved lasing under both pulsed and CW operation. Lasing was stable for over 20 minutes under CW operation. The following section presents the results during electroluminescence under pulsed and CW operation.

a. Pulsed Operation Measurement (10 kHz pulse repetition, 500 ns pulse width)

FIG. 4A illustrates the peak output power was 700 μW for the 6 μm aperture diameter VCSEL shown in Fig. 1. Although not shown, the highest peak output power

was 1 mW for a 10 μm aperture diameter device. The previous best m-plane VCSEL had a peak output power of 550 μW [10]

Lasing emission from the device (fabricated according to FIG. 1) was polarized along the a-direction with a polarization ratio of 100%.

FIG. 4B shows the threshold current was approximately 12 mA (42.4 kA/cm^2). The L-I kink at threshold in Fig. 2(a) at 12 mA is less pronounced because the large-area photodetector measures additional light that escapes the device from areas uncovered with metal, including the sidewall and top-side of the device. The L-I kink at threshold in Fig. 2(b) at 12 mA is much more well-defined because the spectrometer fiber optic was aligned to the lasing peak, which minimizes the measured spontaneous emission below threshold.

The differential efficiency of the device fabricated according to FIG. 1A-1B improves at currents greater than 30 mA due to the appearance of a dominating longer-wavelength longitudinal mode (differential efficiency below 30 mA: $\eta_d = 0.267\%$; differential efficiency above 30 mA: $\eta_d = 0.775\%$). This is more than twice the differential efficiency of previous m-plane VCSELs that had a value of $\eta_d = 0.26\%$ [10].

The device fabricated according to FIG. 1A-1B had a series resistance of $R_d = 27.38\ \Omega$. This series resistance is improved (smaller) compared to previous m-plane VCSELs that had a value of $R_d = 37\ \Omega$ [10].

FIGs. 5A-5B shows the onset of lasing occurs between 11.4 – 15.1 mA, which is consistent with the threshold current of 12 mA from the I-L curve in FIG. 4B. The 406 nm and 412 nm lasing modes both appear at 15.1 mA. The 406 nm lasing mode likely appears first at a lower current than the 412 nm mode. As current is increased, the increased temperature causes the peak gain wavelength to redshift. This results in longer-wavelength modes increasing in intensity as shorter-wavelength modes decrease in intensity.

FIG. 5A illustrates that at 17.7 mA, the 406 nm mode decreases in intensity while the 412 nm mode increases in intensity. The effect of temperature-induced emission redshifting was further studied by measuring the spectrum at various pulse widths. While FIGs. 5A-5B corresponds to a 500 ns pulse width, for a 100 ns pulse width, the peak emission wavelength was 412 nm instead of 419.3 nm. For a 1000 ns pulse width, the threshold current was lower than 11 mA. Longer pulse width causes more heating which redshifts the gain and lowers the threshold for the longer-wavelength mode.

As shown in FIG. 5B, a dominant lasing mode appears at 419.3 nm at 33.2 mA. Although the peak spontaneous emission wavelength is 402 nm, the longer-wavelength modes dominate in intensity. Possible explanations include longer wavelengths experiencing lower levels of optical loss because (1) longer wavelengths have much lower levels of loss from the ion implanted region, and (2) TMM models indicate that longer wavelengths have less mode overlap with the highly absorptive tunnel junction in this design.

b. Continuous Wave (CW) Operation

FIGs. 6A-6B illustrate the threshold current is approximately 10 mA and corresponds to a lasing wavelength of 412 nm. The *L-I* kink at 10 mA is obscured by the measurement of spontaneous emission power with the large-area photodetector, as described earlier.

Measuring the spectrum, as shown in FIG. 6B, provides further insight into, and verification of, the threshold for lasing. FIG. 6B shows the onset of lasing occurs at 11.5 mA, FWHM = 0.74 nm, the 412 nm mode increases in intensity until a current of 15.1 mA, at which a lasing mode appears at a wavelength of 420 nm. The lasing mode at 420 nm has a FWHM = 1.5 nm (spectrometer-limited).

Unlike the pulsed measurement, the lasing mode at 406 nm does not appear during CW operation due to the redshifted peak gain. For the longer-wavelength lasing

mode, the lasing wavelength is 419.69 nm at 15.1 mA and it redshifts to 420.44 nm at 19.9 mA. This corresponds to a shift in Fabry-Perot wavelength with temperature of approximately 0.016 nm/°C, which is comparable to reported values [15].

At 13.5 mA CW operation, the differential efficiency improves due to the emergence of a lasing mode at 420 nm (average differential efficiency $\eta_d = 0.4095\%$; peak differential efficiency $\eta_d = 1.11392\%$).

c. Mode Structure

The lateral mode structure of the device fabricated according to FIGs. 1A-1B is much improved compared to previous *m*-plane VCSELs that showed filamentary lasing (a stochastic distribution of lasing within the aperture) [10].

The lateral mode illustrated in FIG. 7A shows a well-defined lasing mode in the center of the aperture. The improved lateral mode profile could be attributed to the following:

- Optimization of the MBE regrowth, which could have improve the current spreading and uniformity;
- Removal of an oxide residue after PEC etching

FIG. 7B is an image of the mode taken at a higher integration time to show the spontaneous emission more clearly.

d. Thermal Impedance

Prior *m*-plane VCSELs were not able to achieve CW operation due to poor thermal performance. Under CW operation, the increased temperature redshifts the gain spectrum away from the cavity resonance, which prevents lasing. The poor thermal performance is mainly due to the thermally-insulating dielectric DBR on the p-side. Thermal modeling using COMSOL predicts that a negligible amount of heat flux occurs through the dielectric DBR. The main pathway for heat transport is around the dielectric

DBR through the metal contact to the flip-chip substrate. Cross-sectional SEM analysis revealed that there are cracks and voids in the main metal pathway for heat transport, which likely prevented CW operation.

As illustrated herein, CW VCSEL operation was achieved using a design that improves thermal performance:

- Longer cavity length (e.g., 23λ instead of 7λ).
- Improved flip-chip bonding using indium-gold bonding instead of Au-Au bonding. In-Au bonding can be performed at a much lower force and temperature compared to Au-Au bonding. This results in fewer cracks in the device, and there is a much more robust pathway for heat transport.

FIG. 8 illustrates the effect of heating by plotting the spectrum under CW operation. The spontaneous emission envelope redshifts with increasing current due to increased active region temperature. At 9 mA, the spontaneous emission is centered at 405.3 nm and redshifts to 416 nm at a current of 25 mA. The FWHM is 19.1 nm at 9 mA and broadens to a value of 29.9 nm at 25 mA. The shift in peak emission wavelength with increasing temperature was found to be 0.048 nm/°C by measuring the spectrum of an *m*-plane LED at stage temperatures up to 60 °C. Assuming a linear shift of 0.048 nm/°C, the VCSEL active region temperature can be estimated by its peak spontaneous emission wavelength. At 15 mA, the active region temperature is approximately 180 °C. At 19 mA, the active region temperature is approximately 226 °C. Based on these calculations, the thermal impedance is approximately 1500 °C/W. A similar analysis was conducted on a VCSEL with a 7λ cavity length which had a thermal impedance of approximately 3000 °C/W.

e. Solid Liquid Interdiffusion (SLID) Bonding

Prior GaN VCSELs could not lase under CW operation due to their poor thermal performance, which was notably due to the thermally-insulating dielectric DBR mirror on

the bottom sides of the devices. COMSOL Thermal modeling (FIG. 9) shows that the main pathway for heat transport was around the bottom DBR through a thin metal contact toward the flip-chip substrate. FIG. 10 shows FIB cross-sectioning revealing cracks in that metal contact. Thermal modeling illustrated in FIG. 11A and FIG. 11B shows that cracks in that metal contact severely impair the thermal performance.

Au-Au thermocompression bonding forms a bond through atomic diffusion, and requires a relatively high temperature and bonding force as the melting temperature for gold is 1064 °C. Cracking of entire VCSEL devices was caused by Au-Au compression bonding due to the high temperature and force required for Au-Au thermocompression bonding. However, Au-Au thermocompression bonding does not include a molten liquid phase during bonding because it is conducted below the melting temperature of Au and gold has a very high melting temperature.

A technique that incorporates a liquid metal phase during bonding, such as SLID bonding, enables flip-chip bonding at significantly lower bonding forces to help overcome several problems caused by Au-Au thermocompression bonding.

- The relatively soft bonding metal used for SLID can reduce cracking by providing cushioning as the bonding surfaces are pressed together.
- Utilizing a liquid metal phase during bonding to completely embed the p-DBR within metal, thereby creating a thicker metal pathway for heat transport. Unlike Au-Au thermocompression bonding, utilizing a liquid metal phase (as possible with Au-In SLID bonding) during bonding allows the bottom thermally insulating DBR (p-DBR) to be completely embedded within bonding metal. Embedding the thermally-insulating p-DBR within metal creates a much thicker metal pathway for heat transport, especially compared to an *m*-plane VCSELs in which heat flow was bottlenecked through a cracked 1-μm-thick gold contact along the sidewall of the bottom DBR (as fabricated using Au-Au thermocompression bonding).

FIG. 12 illustrates a VCSEL bonded to a flip chip substrate using SLLID, illustrating the SLID softens the bond to reduce cracking and enables a thicker metal pathway for heat transport.

FIG. 13 (Au-In phase diagram) illustrates the benefits of using Au-In SLID bonding because Au-In alloys have a unique low-temperature liquid phase above ~156 °C for In-rich alloys (above 54 wt.% In). This enables flip-chip bonding at much lower temperatures and forces compared to Au-Au or Au-Sn bonding while also incorporating a liquid metal phase. As seen in the phase diagram, Au-In alloys with In compositions above 54% consist of a mixture of an In phase and $AuIn_2$ intermetallic compound (53.8 wt.% In) with a solidus temperature of 156 °C. Above 156 °C, the mixture forms a liquid phase with $AuIn_2$ grains. The alloy becomes a mixture of AuIn (36.79 wt.% In) and $AuIn_2$ intermetallic compounds for compositions between 36.8-54 wt.% In, and the solidus temperature becomes much higher with a value of 495.4 °C. This considerable difference in solidus temperatures is a particularly useful feature because it enables a relatively low-temperature liquid phase above 156 °C during bonding (for > 54 wt.% In alloys) while the final alloy can be designed to have a lower In composition so it can withstand temperatures up to 495.4 °C without melting (for 36.8-54 wt.% In alloys).

Although other types of bonding could also work, such as Au-Sn, Au-Ge, and Au-Si eutectic alloys, Au-In alloys have the lowest temperature liquid phase. Pure indium bonding could also be employed, but the resulting bond is only stable up to ~156 degrees Celsius (melting temperature of indium). Au-In SLID bonding can be conducted so the Au-In alloy after bonding has a lower In composition so the bond is stable up to ~495 degrees Celsius.

Gold-tin (Au-Sn) alloys are another possible alternative as they have a fairly low melting temperature of 280 °C at the eutectic composition of 80% Au and 20% Sn. However, 280 °C is not much lower than the temperature used in the previous Au-Au bonding experiments, so cracking could remain a problem.

H. Advantages and Improvements

Nonpolar III-nitride VCSELs are very promising due to their unique properties, such as higher material gain and 100% polarization ratio. Thicker QWs are desirable for III-nitride VCSELs to maximize gain enhancement factor. Compared to c-plane, nonpolar and semipolar orientations enable thicker quantum wells, > 9 nm thick.

This disclosure details the fabrication process for the first m-plane VCSEL that achieved lasing under CW operation at room temperature. All previous *m*-plane III-nitride VCSELs were only able to lase under pulsed operation. Compared to the previous *m*-plane VCSEL design [10], the key performance improvements of the present invention are summarized in Table 1.

Table 1. Key performance improvements of the present invention

	Previous *m*-plane VCSEL [10]	The present invention
CW Operation	No	Yes
Peak Output Power	0.55 mW	1 mW
Differential Efficiency η_d	0.26%	0.78%
Series Resistance R_d	37 Ω	27.4 Ω
Lateral Mode Profile	Filamentary Lasing	Well-defined lateral mode

Further information on embodiments of the present invention can be found in [27-30].

Nomenclature

GaN and its ternary and quaternary compounds incorporating aluminum and indium (AlGaN, InGaN, AlInGaN) are commonly referred to using the terms (Al,Ga,In)N, III-nitride, III-N, Group III-nitride, nitride, $Al_{(1-x-y)}In_yGa_xN$ where $0 < x < 1$

and $0 < y < 1$, or AlInGaN, as used herein. All these terms are intended to be equivalent and broadly construed to include respective nitrides of the single species, Al, Ga, and In, as well as binary, ternary and quaternary compositions of such Group III metal species. Accordingly, these terms comprehend the compounds AlN, GaN, and InN, as well as the ternary compounds AlGaN, GaInN, and AlInN, and the quaternary compound AlGaInN, as species included in such nomenclature. When two or more of the (Ga, Al, In) component species are present, all possible compositions, including stoichiometric proportions as well as "off-stoichiometric" proportions (with respect to the relative mole fractions present of each of the (Ga, Al, In) component species that are present in the composition), can be employed within the broad scope of the invention. Accordingly, it will be appreciated that the discussion of the invention hereinafter in primary reference to GaN materials is applicable to the formation of various other (Al, Ga, In)N material species. Further, (Al,Ga,In)N materials within the scope of the invention may further include minor quantities of dopants and/or other impurity or inclusional materials. Boron (B) may also be included.

One approach to eliminating the spontaneous and piezoelectric polarization effects in GaN or III-nitride based optoelectronic devices is to grow the III-nitride devices on nonpolar planes of the crystal. Such planes contain equal numbers of Ga (or group III atoms) and N atoms and are charge-neutral. Furthermore, subsequent nonpolar layers are equivalent to one another so the bulk crystal will not be polarized along the growth direction. Two such families of symmetry-equivalent nonpolar planes in GaN are the {11-20} family, known collectively as a-planes, and the {1-100} family, known collectively as m-planes. Thus, nonpolar III-nitride is grown along a direction perpendicular to the (0001) c-axis of the III-nitride crystal.

Another approach to reducing polarization effects in (Ga,Al,In,B)N devices is to grow the devices on semi-polar planes of the crystal. The term "semi-polar plane" (also referred to as "semipolar plane") can be used to refer to any plane that cannot be

classified as c-plane, a-plane, or m-plane. In crystallographic terms, a semi-polar plane may include any plane that has at least two nonzero h, i, or k Miller indices and a nonzero l Miller index.

Some commonly observed examples of semi-polar planes include the (11-22), (10-11), and (10-13) planes. Other examples of semi-polar planes in the wurtzite crystal structure include, but are not limited to, (10-12), (20-21), and (10-14). The nitride crystal's polarization vector lies neither within such planes or normal to such planes, but rather lies at some angle inclined relative to the plane's surface normal. For example, the (10-11) and (10-13) planes are at 62.98° and 32.06° to the c-plane, respectively.

The Gallium or Ga face of GaN is the c^+ or (0001) plane, and the Nitrogen or N-face of GaN or a III-nitride layer is the c^- or (000-1) plane.

The prefix n- (e.g., n-GaN) represents n-type, the prefix n^{++}- (e.g., n++- GaN) represents higher n-type dopant concentration, the prefix p- (e.g., p-GaN) represents p-type, the prefix p^{++}- (e.g., p++- GaN) represents higher p-type dopant concentration.

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[30] The World's First CW Non-polar GaN VCSEL, The World's First CW Non-polar GaN VCSEL, by C. Forman et. al., Vol. 24 Issue 2, March 2018, article found at website "https://compoundsemiconductor.net/article/104228/The_World's_First_CW_Non-polar_GaN_VCSEL/feature."

Conclusion

This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has

been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A device, comprising:

a mount;

a Vertical Cavity Surface Emitting Laser (VCSEL) on the mount; and

a thermally conductive bond between the mount and the VCSEL, the bond comprising a layer of metal having a thermal conductivity such that heat, generated during operation of the VCSEL, is transferred from the VCSEL to the mount and the VCSEL emits continuous wave electromagnetic radiation.

2. The device of claim 1, wherein the thermally conductive bond comprises no cracks or fewer cracks than a bond between the VCSEL and the mount formed using Au-Au thermal compression bonding.

3. The device of claim 1, wherein the thermally conductive bond comprises metal formed from a liquid metal phase.

4. The device of claim 1, wherein the VCSEL is bonded to the mount by solid-liquid interdiffusion bonding.

5. The device of claim 1, wherein:

the VCSEL comprises a first mirror and a second mirror defining a cavity for the continuous wave electromagnetic radiation, and

the VCSEL is bonded to the mount by forming the bond comprising a metal layer, in a liquid state, around the first mirror.

6. The device of claim 1, wherein:

the VCSEL comprises a first mirror and a second mirror defining a cavity for the continuous wave electromagnetic radiation,

the thermally conductive bond comprises a metal layer, and

one of the first mirror or the second mirror is embedded in the metal layer.

7. The device of claim 1, wherein:

the VCSEL comprises a first mirror and a second mirror defining a cavity for the electromagnetic radiation, and

the thermally conductive bond comprises a metal layer cast around the first mirror or the second mirror acting as a mold for the metal layer.

8. The device of claim 1, wherein the thermally conductive bond comprises an intermetallic compound having a solid phase containing two or more metallic elements.

9. The device of claim 1, wherein the thermally conductive bond comprises a first metal diffused into a second metal so as to intermix with a second metal, the first metal having a lower melting point than the second metal.

10. The device of claim 9, wherein first metal comprises indium and the second metal comprises gold.

11. The device of any of the preceding claims, wherein:

the VCSEL includes a light emitting III-nitride active region emitting the continuous wave electromagnetic radiation in response to the current inputted into the active region,

the light emitting III-nitride active region includes quantum wells (QWs), and

each of the quantum wells have a thickness of more than 8 nm.

12. The device of claim 11, wherein the thickness is in a range of 8-20 nanometer (nm).

13. The device of any of the preceding claims, wherein the VCSEL has a nonpolar or semipolar crystal orientation.

14. The device of any of the preceding claims, wherein:

the VCSEL has a cavity length of at least 7 λ, where λ is a peak wavelength of the continuous wave electromagnetic emitted from the VCSEL's active region, as measured in the active region, and

the peak wavelength is the wavelength of the continuous wave electromagnetic radiation having the highest intensity.

15. The device of claim 14, wherein the cavity length is in a range of 20 λ – 100λ.

16. The device of any of the previous claims, wherein the VCSEL further includes:

the active region between a first III-nitride n-type layer and a III-nitride p-type layer,

a second III-nitride n-type layer forming a tunnel junction with the III-nitride p-type layer,

a contact layer for the tunnel junction, and

a top surface of the contact layer having a root mean square surface roughness (RMS) of less than 2 nanometers (nm) when the VCSEL is a nonpolar device or less than 1 nm when the VCSEL is a semipolar device.

17. The device of any of the previous claims, wherein:

the active region is between a III-nitride n-type layer and a III-nitride p-type layer,

an n-side surface of the III-nitride layer is exposed after etching to at least partially remove the substrate on which the active region was grown, and

the n-side surface is surface treated and has an RMS surface roughness less than 1 nm.

18. The device of claims 16 or 17, wherein the surface roughness is over a 5 μm x5 μm, a 1 μm x 1μm, or 10 μm x 10 μm area.

19. The device of claim 17, wherein the surface treatment removes an oxide residue after the etching.

20. A VCSEL comprising:

a first mirror and a second mirror defining a cavity for electromagnetic radiation emitted from the VCSEL;

a flip chip substrate;

a metal layer between the VCSEL and the flip chip substrate, wherein:

the metal layer includes indium and gold, and

the first mirror or the second mirror is embedded in the metal layer.

21. The VCSEL of claim 20, wherein the mirrors comprise a distributed bragg reflector including dielectric layers.

22. A method of fabricating a Vertical Cavity Surface Emitting Laser (VCSEL) structure, comprising:

bonding a VCSEL to a mount using metal, wherein the bonding comprises:

providing a metal layer on the mount, the metal layer comprising a first metal and a second metal, and

heating the metal layer so that the first metal is in liquid metal state,

positioning the VCSEL on the metal layer including the first metal in the liquid state, and

allowing the metal layer to solidify and form a bond between the VCSEL and the mount.

23. The method of claim 22, wherein:

the VCSEL comprises a first mirror and a second mirror defining a cavity for electromagnetic radiation emitted from the VCSEL, and

the positioning comprises positioning the first mirror on the metal layer using a force or pressure when the first metal layer is in the liquid metal state, so that the first metal layer is embedded in the metal layer after the metal layer has solidified.

24. The method of claims 22 or 23, wherein the VCSEL is bonded to the mount by solid-liquid interdiffusion bonding, the first metal comprises indium, and the second metal comprises gold.

25. A method of fabricating a Vertical Cavity Surface Emitting Laser (VCSEL) structure, comprising:

growing a sacrificial layer on a semipolar or nonpolar III-nitride substrate;

growing a III-nitride VCSEL structure including an active region between an n-type layer and a p-type layer, wherein the active region includes a quantum well having a thickness greater than 8 nm;

at a temperature of less than 750°C, growing a tunnel junction structure on the p-type III-Nitride using an indium surfactant;

depositing a mirror on a p-type side of the VCSEL structure;

covering sidewalls of the active region with a dielectric layer;

depositing metal on the mirror;

flip chip bonding a flip chip substrate to the metal on the mirror using solid-liquid interdiffusion bonding, and

photoelectrochemically etching the sacrificial layer so as to at least partially remove the nonpolar or semipolar III-nitride substrate; and

removing, using a surface treatment, a rough residue on an n-type side of the VCSEL structure or on the surface of the n-type layer exposed during the etching.

26. The method of claim 25, wherein the removing comprises treating the surface with Tergitol detergent or KOH.

27. The method of claims 25 or 26, wherein: the VCSEL structure is grown with a cavity length of at least 7 λ, where λ is a peak wavelength of light emitted from the active region when the light is in the active region; and the peak wavelength is the wavelength of the light having the highest intensity.

28. The method of claims 25-27 wherein a surface of the n-type layer has a root mean square (RMS) surface roughness of less than 1 nm after the surface treatment.

29. The method of claim 28, wherein the surface roughness is over a 5 μm x5 μm, a 1 μm x 1μm, or 10 μm x 10 μm area.

30. The method of any of the claims 25-29, wherein the VSCEL emits continuous wave electromagnetic radiation.

31. A VCSEL emitting continuous wave electromagnetic radiation.

32. The VCSEL of claim 31, wherein the VCSEL comprises III-nitride.

33. A Vertical Cavity Surface Emitting Laser (VCSEL), comprising:
a light emitting III-nitride active region including quantum wells (QWs), wherein each of the quantum wells have a thickness of more than 8 nm.

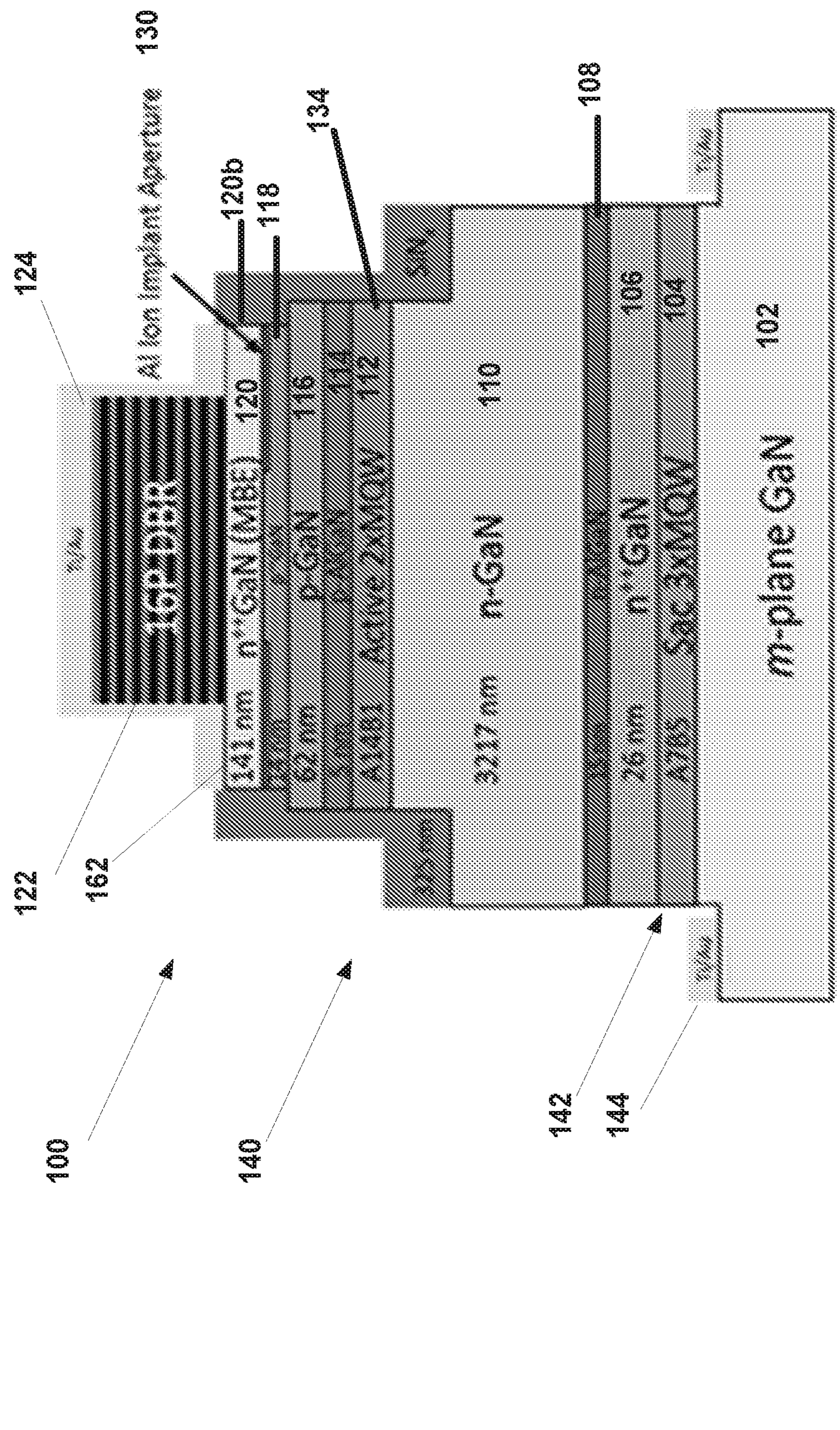
100
140
142
144
122
162
124
Al Ion Implant Aperture
130
120b
118
134
108
16P DBR
141 nm
n++GaN (MBE)
120
62 nm
p-GaN
116
114
A1491
Active 2xMQW
112
3217 nm
n-GaN
110
26 nm
n++GaN
106
A765
Sac 3xMQW
104
m-plane GaN
102

FIG. 1A

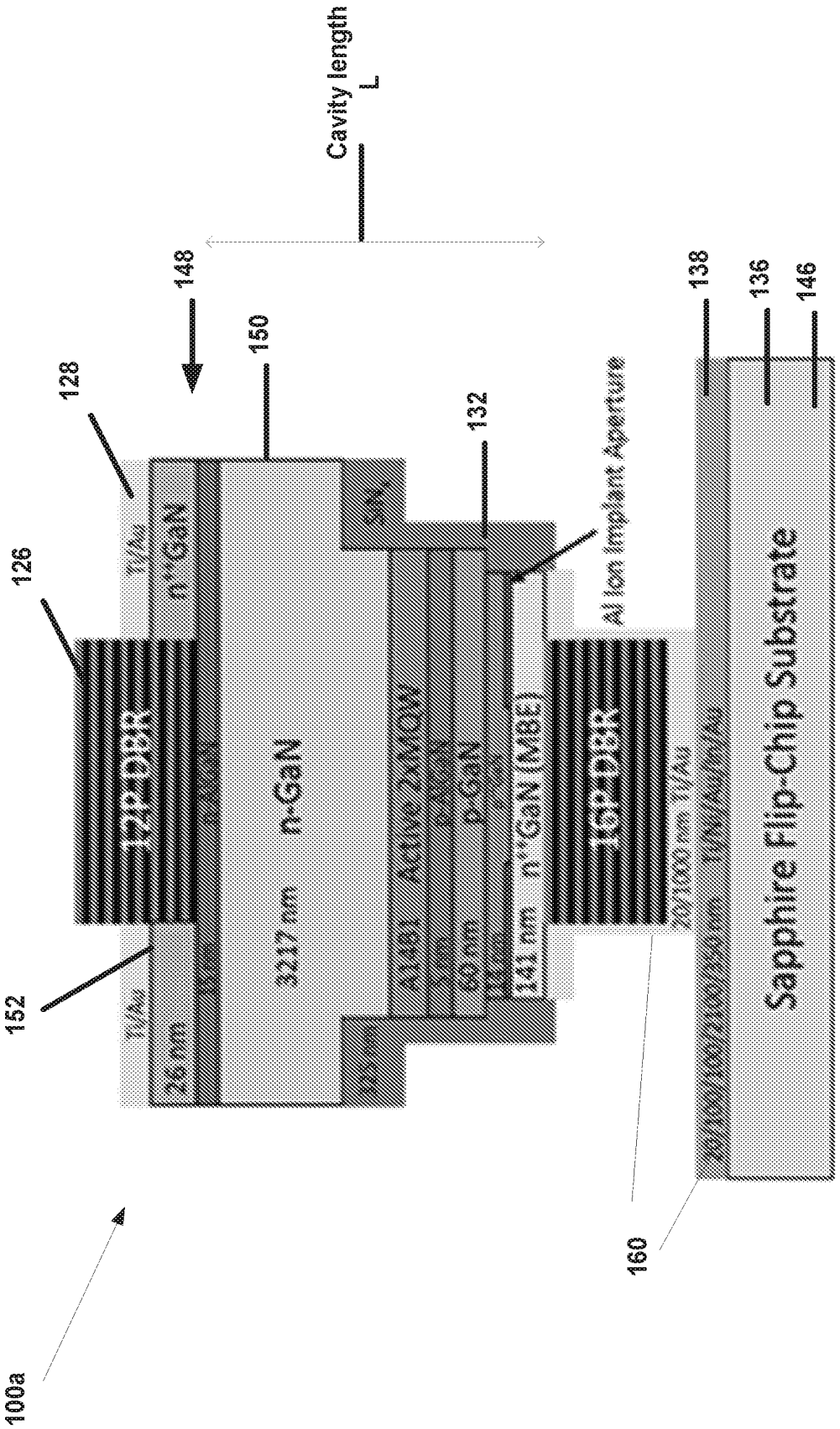
Cavity length
L
148
150
128
132
138
136
146
126
152
160
100a
Al Ion Implant Aperture
Ti/Au
n+GaN
n-GaN
3217 nm
SiN
AlGaN
InGaN
MQW
p-GaN
60 nm
141 nm
n+GaN (MBE)
T2P:DBR
10P:DBR
Sapphire Flip-Chip Substrate

FIG. 1B

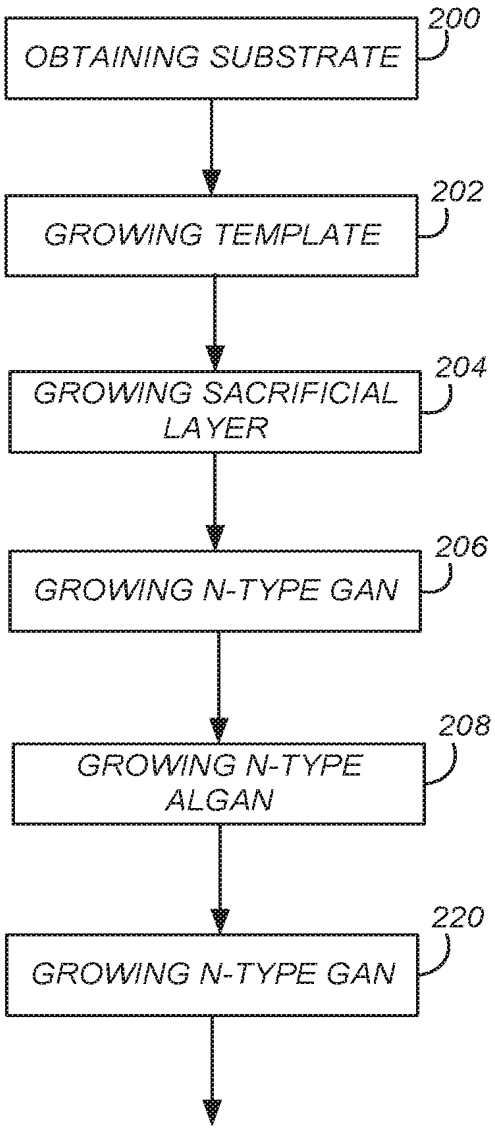
OBTAINING SUBSTRATE
200
GROWING TEMPLATE
202
GROWING SACRIFICIAL LAYER
204
GROWING N-TYPE GAN
206
GROWING N-TYPE ALGAN
208
GROWING N-TYPE GAN
220

FIG. 2

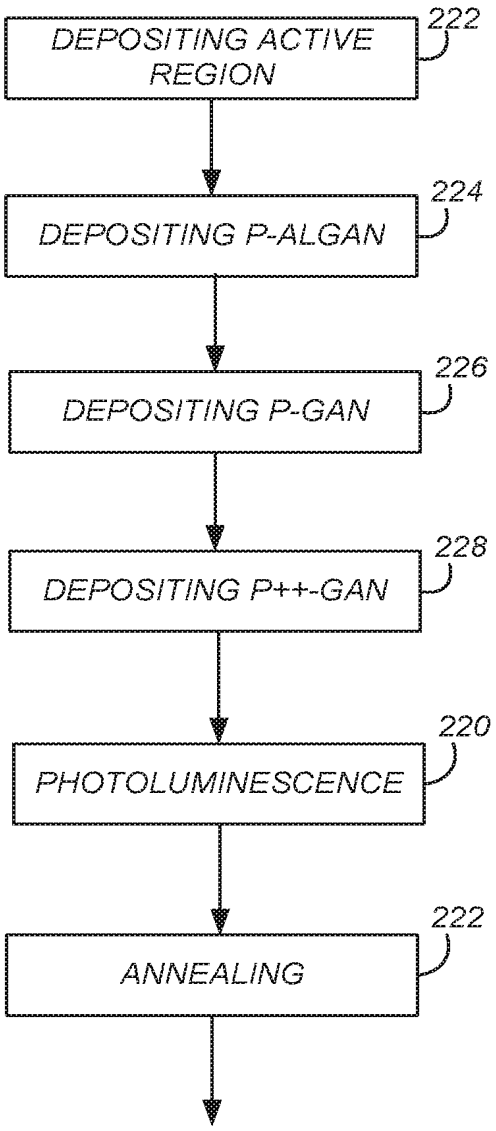
DEPOSITING ACTIVE REGION
222
DEPOSITING P-ALGAN
224
DEPOSITING P-GAN
226
DEPOSITING P++-GAN
228
PHOTOLUMINESCENCE
220
ANNEALING
222

FIG. 2 cont'd

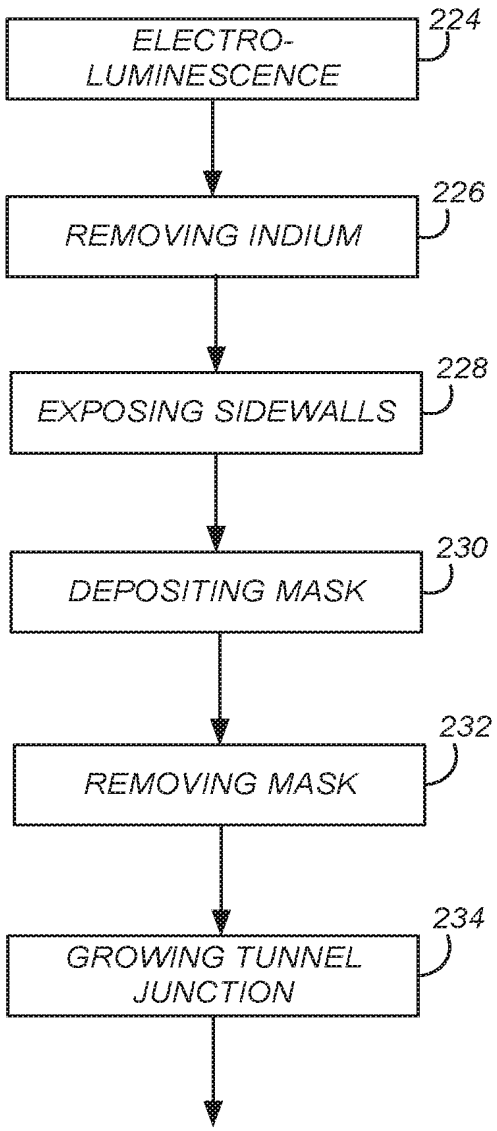
ELECTRO-LUMINESCENCE
224
REMOVING INDIUM
226
EXPOSING SIDEWALLS
228
DEPOSITING MASK
230
REMOVING MASK
232
GROWING TUNNEL JUNCTION
234

FIG. 2 cont'd

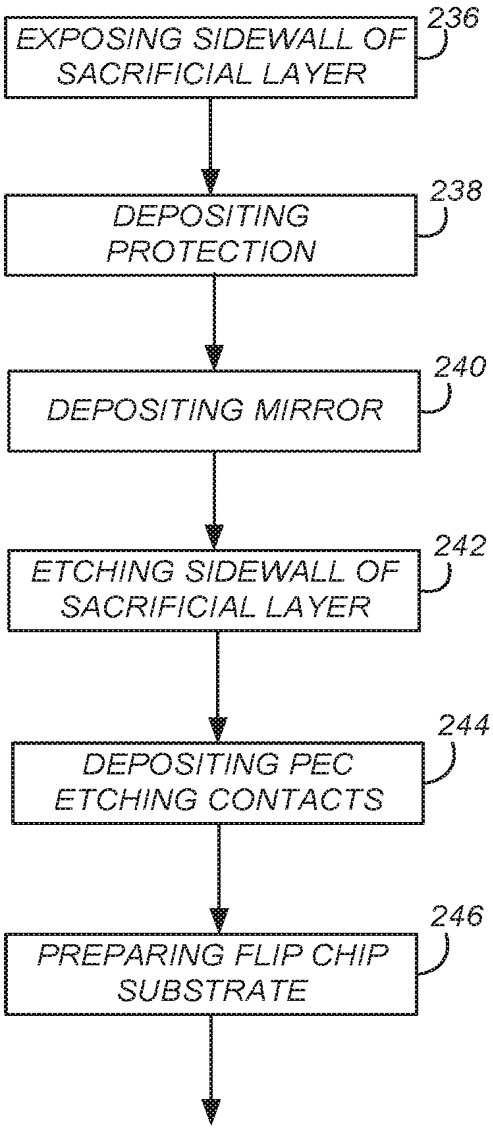
EXPOSING SIDEWALL OF SACRIFICIAL LAYER
236
DEPOSITING PROTECTION
238
DEPOSITING MIRROR
240
ETCHING SIDEWALL OF SACRIFICIAL LAYER
242
DEPOSITING PEC ETCHING CONTACTS
244
PREPARING FLIP CHIP SUBSTRATE
246

FIG. 2 cont'd

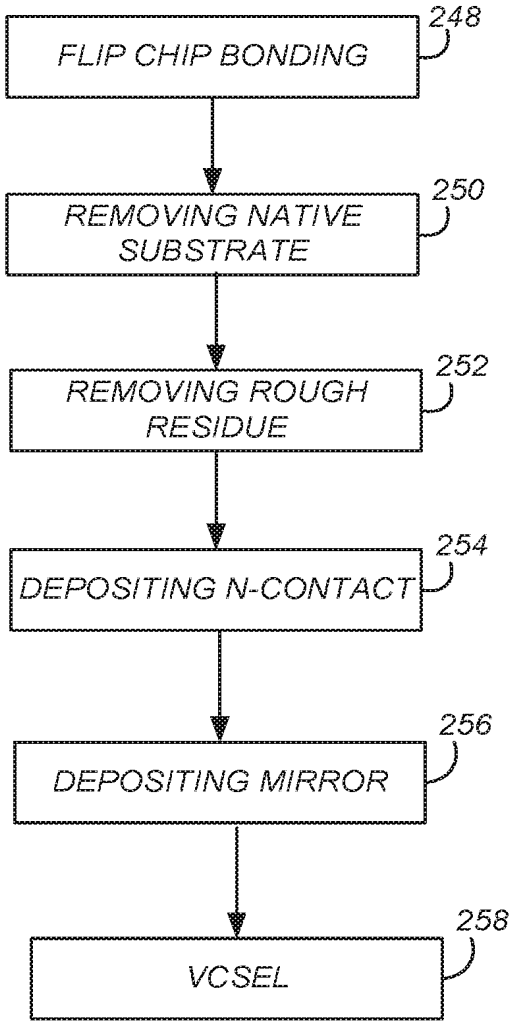
FLIP CHIP BONDING
248
REMOVING NATIVE SUBSTRATE
250
REMOVING ROUGH RESIDUE
252
DEPOSITING N-CONTACT
254
DEPOSITING MIRROR
256
VCSEL
258

FIG. 2 cont'd

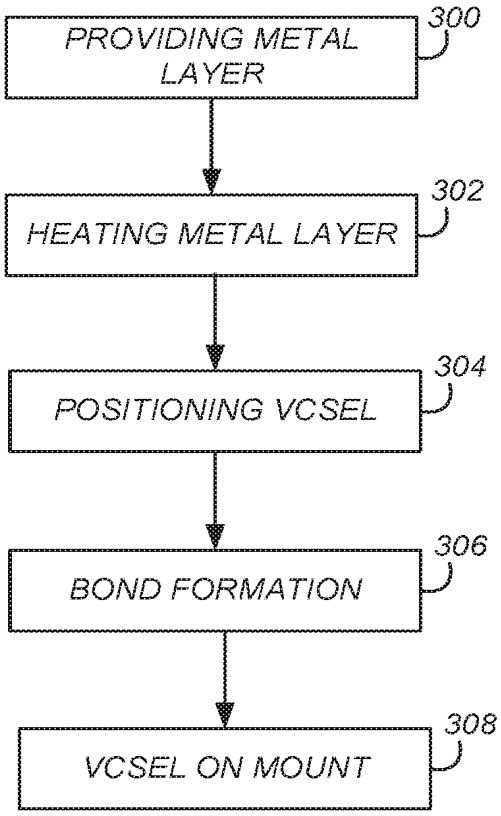
PROVIDING METAL LAYER
300
HEATING METAL LAYER
302
POSITIONING VCSEL
304
BOND FORMATION
306
VCSEL ON MOUNT
308

FIG. 3

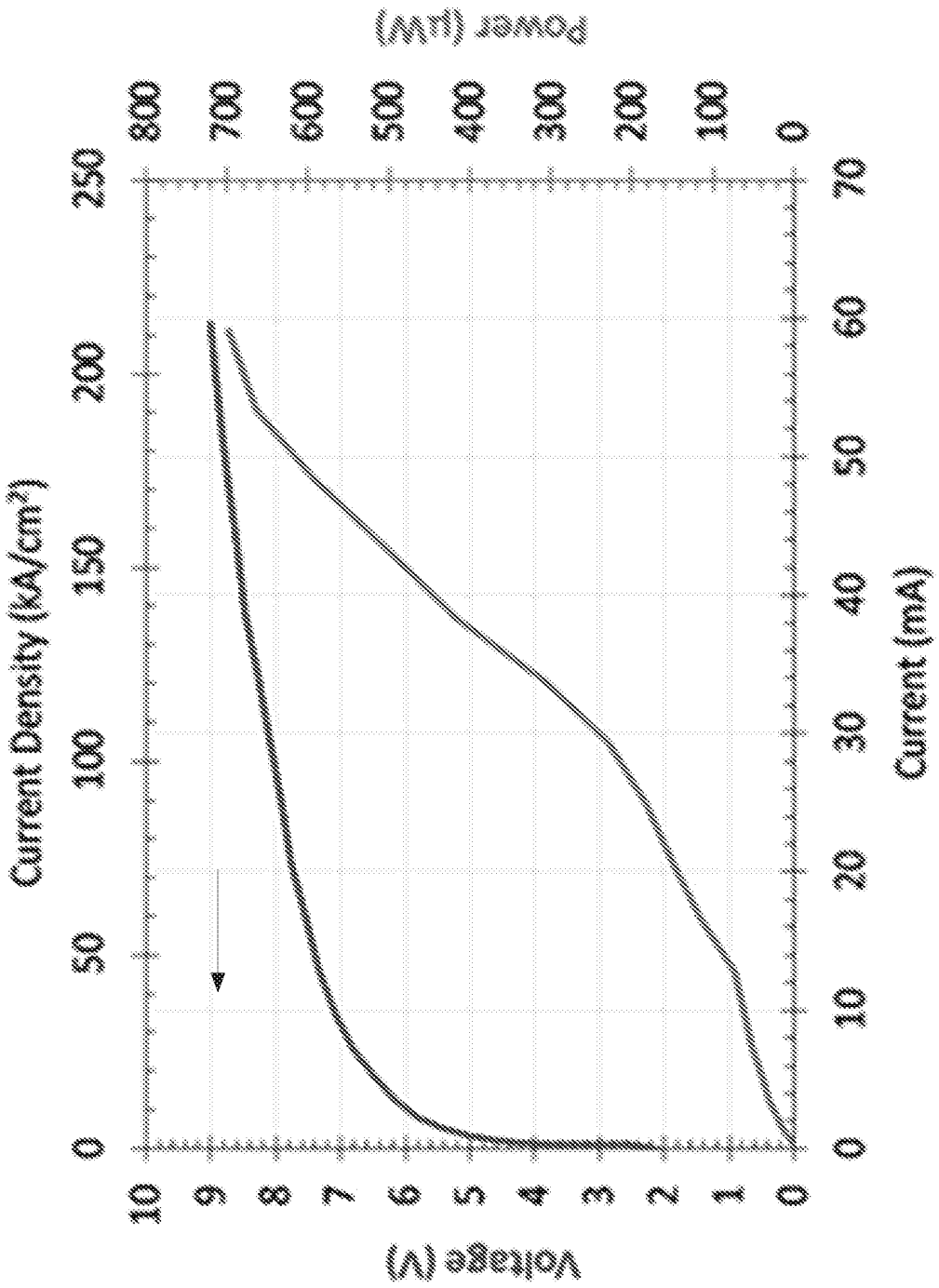
Power (μW)
800
700
600
500
400
300
200
100
0
Current Density (kA/cm²)
250
200
150
100
50
0
Current (mA)
70
60
50
40
30
20
10
0
Voltage (V)
10
9
8
7
6
5
4
3
2
1
0

FIG. 4A

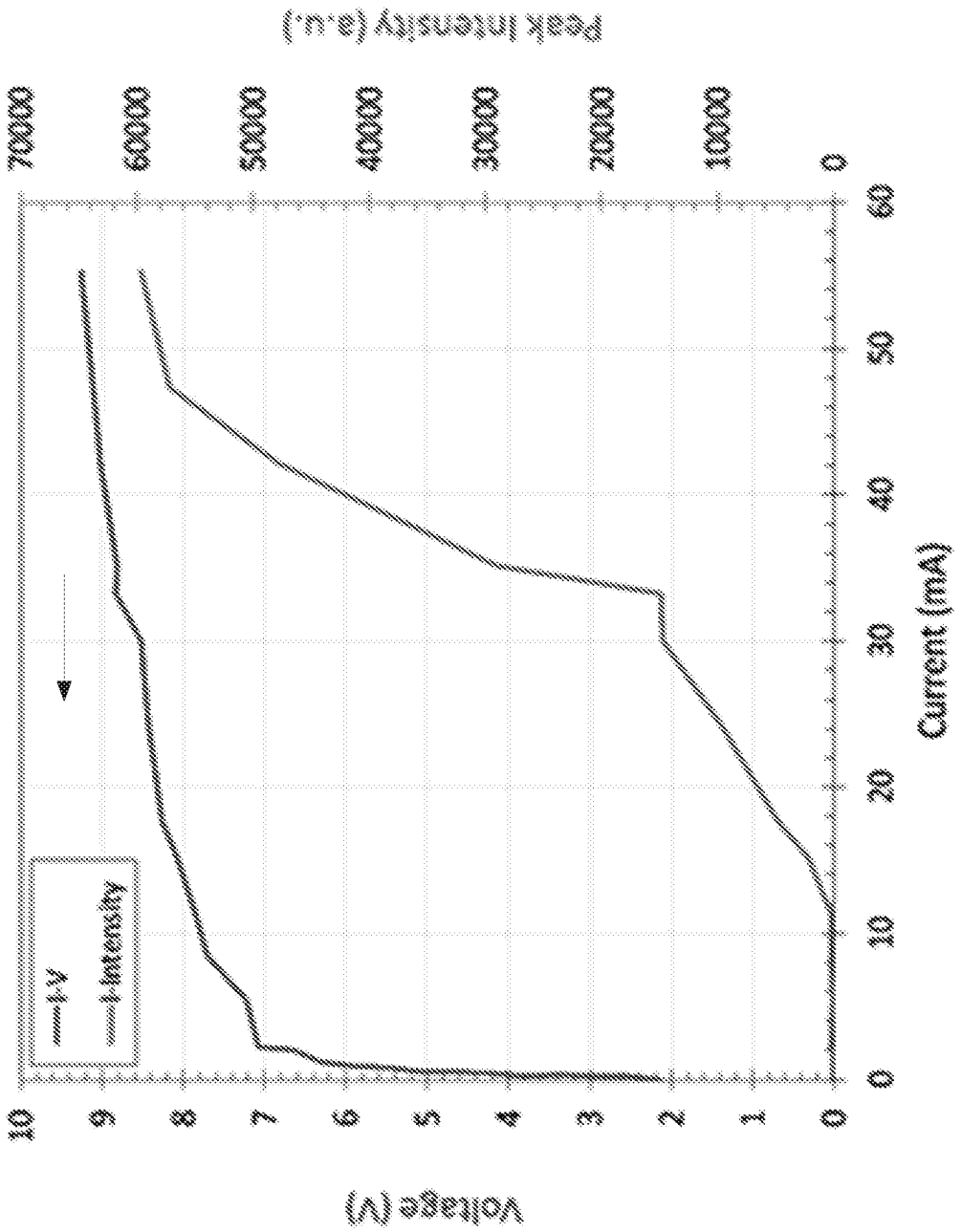
Peak Intensity (a.u.)
70000
60000
50000
40000
30000
20000
10000
0
Voltage (V)
0
1
2
3
4
5
6
7
8
9
10
Current (mA)
0
10
20
30
40
50
60
I-V
I-Intensity

FIG. 4B

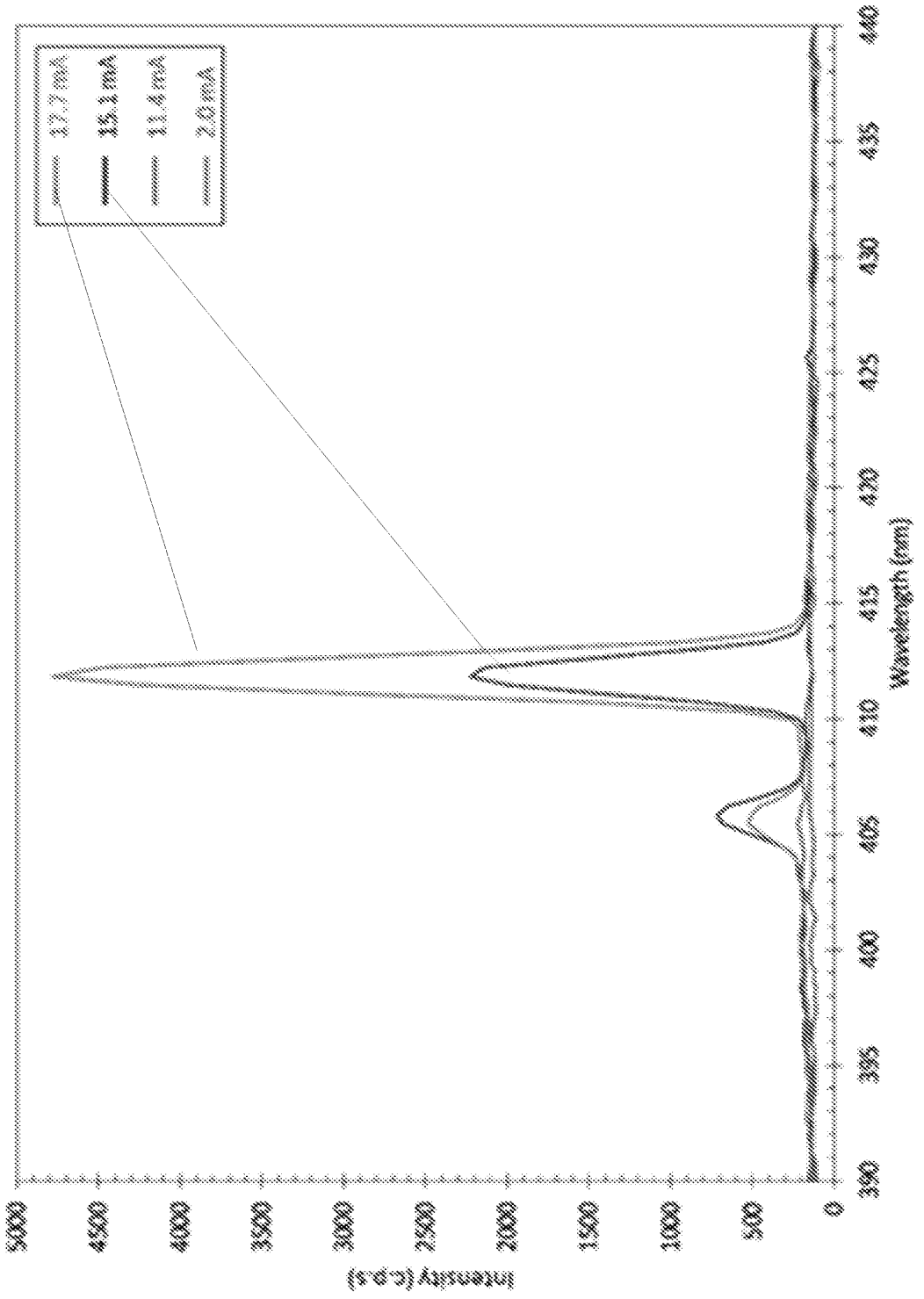
17.7 mA
15.1 mA
11.4 mA
2.0 mA
Intensity (C.p.s)
5000
4500
4000
3500
3000
2500
2000
1500
1000
500
0
390
395
400
405
410
415
420
425
430
435
440
Wavelength (nm)

FIG. 5A

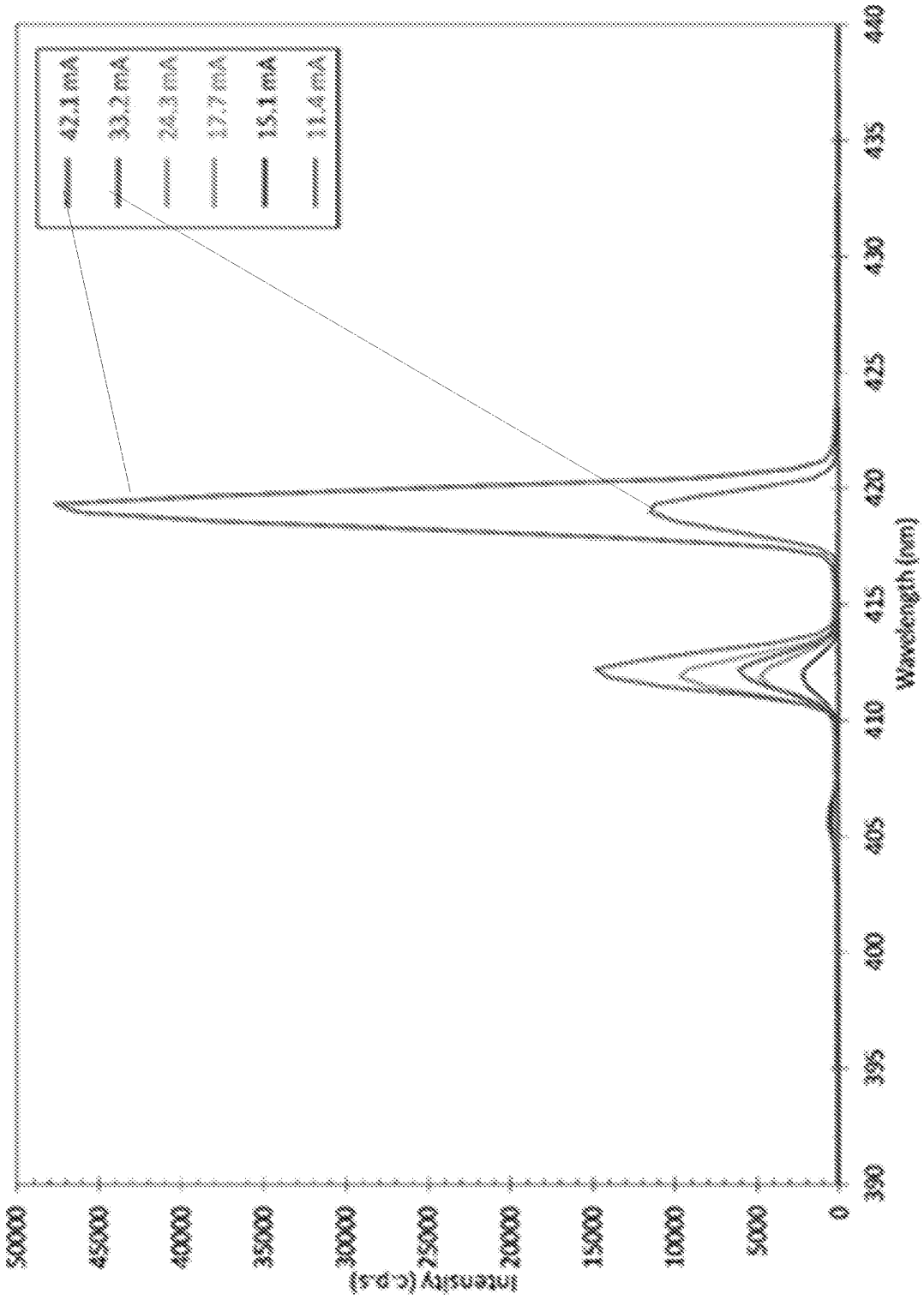
42.1 mA
33.2 mA
24.3 mA
17.7 mA
15.1 mA
11.4 mA
Intensity (c.p.s.)
Wavelength (nm)

FIG. 5B

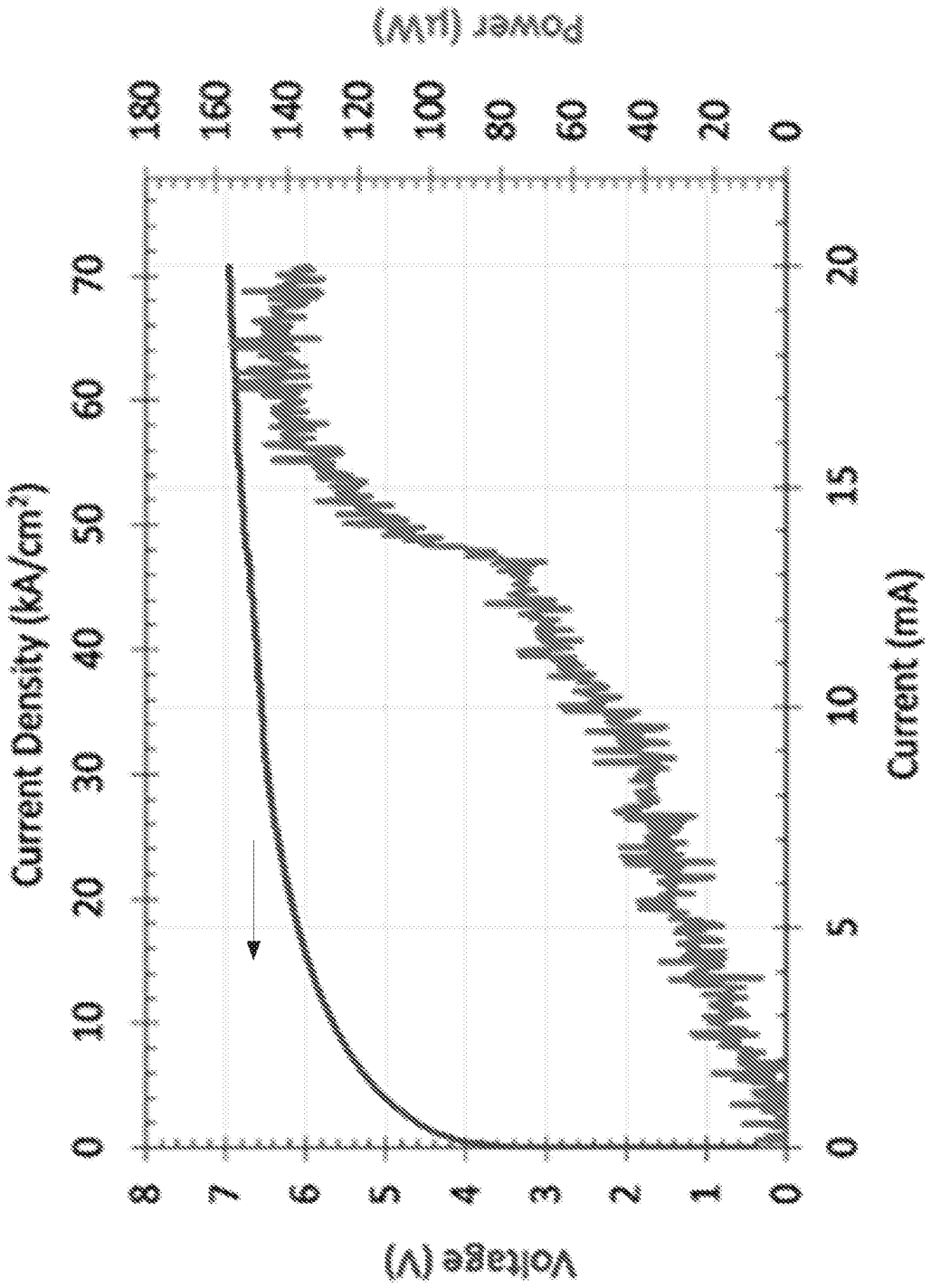
Power (μW)
180
160
140
120
100
80
60
40
20
0
Current Density (kA/cm²)
70
60
50
40
30
20
10
0
Current (mA)
20
15
10
5
0
Voltage (V)
8
7
6
5
4
3
2
1
0

FIG. 6A

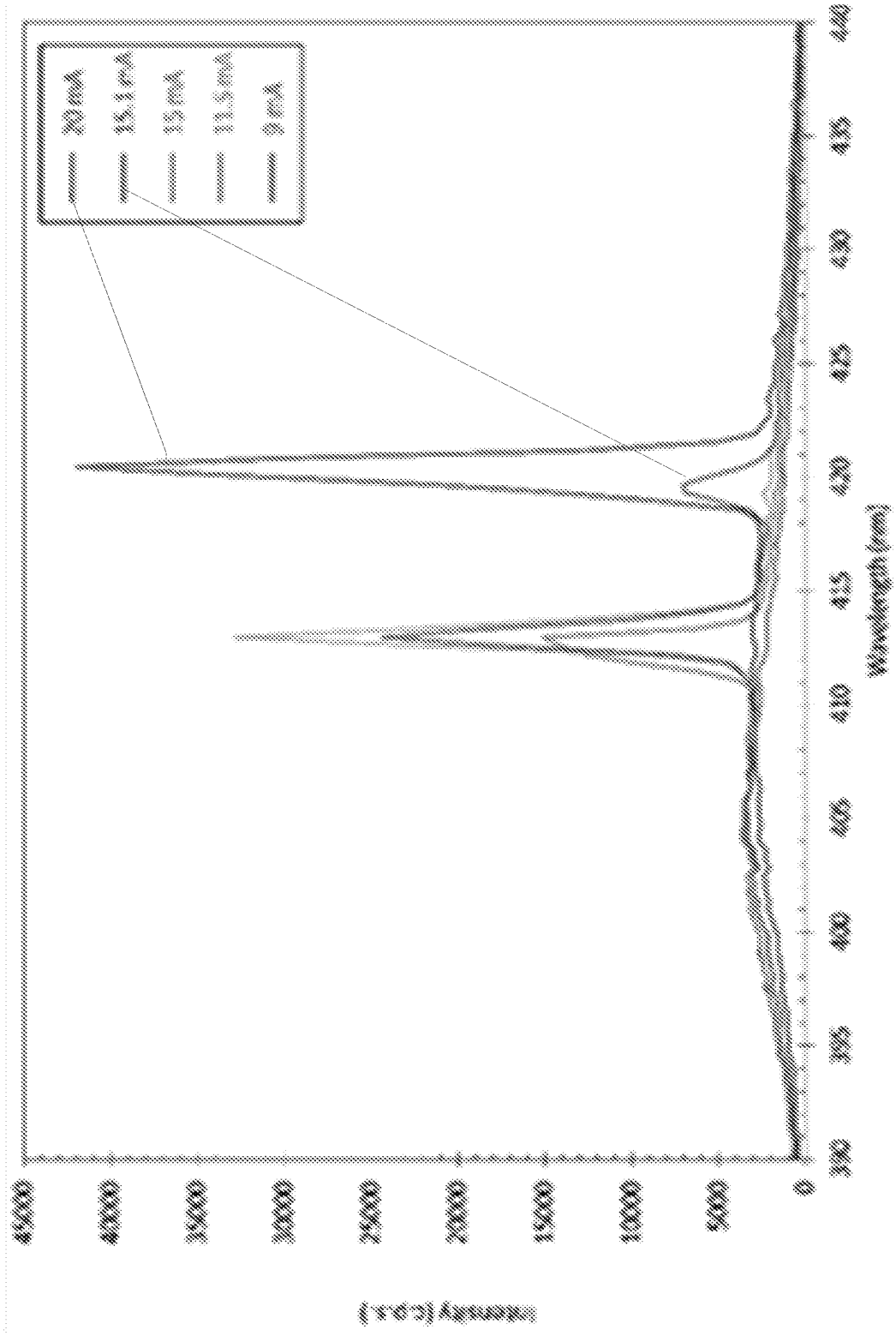

FIG. 6B

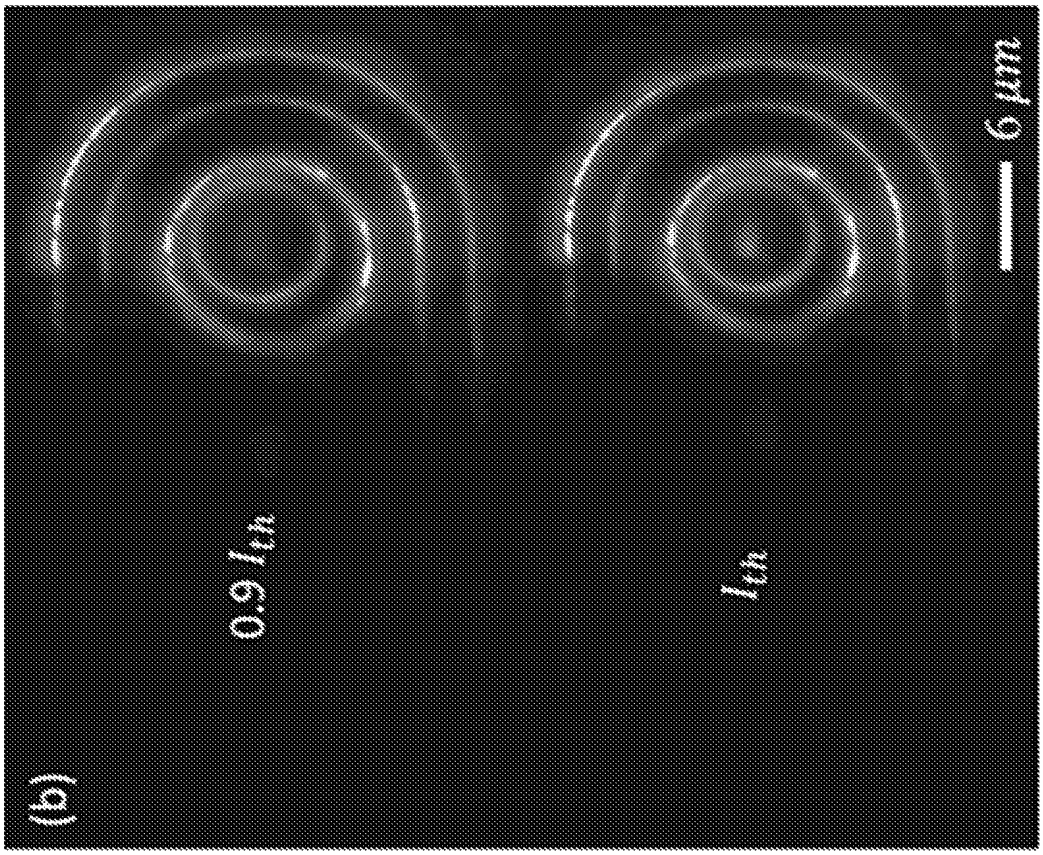

FIG. 7B

FIG. 7A

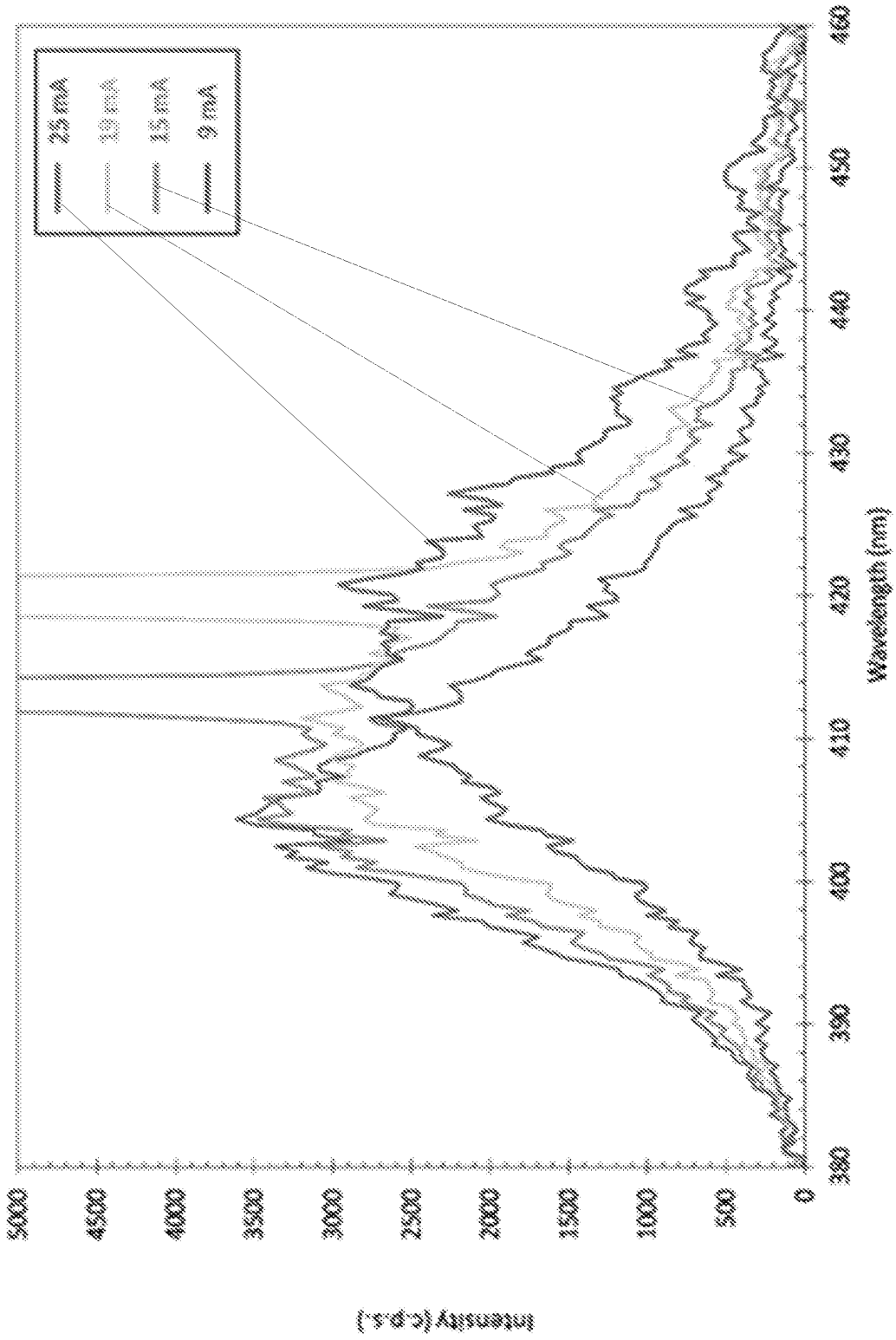
25 mA
19 mA
15 mA
9 mA
Intensity (c.p.s.)
Wavelength (nm)
0
500
1000
1500
2000
2500
3000
3500
4000
4500
5000
380
390
400
410
420
430
440
450
460

FIG. 8

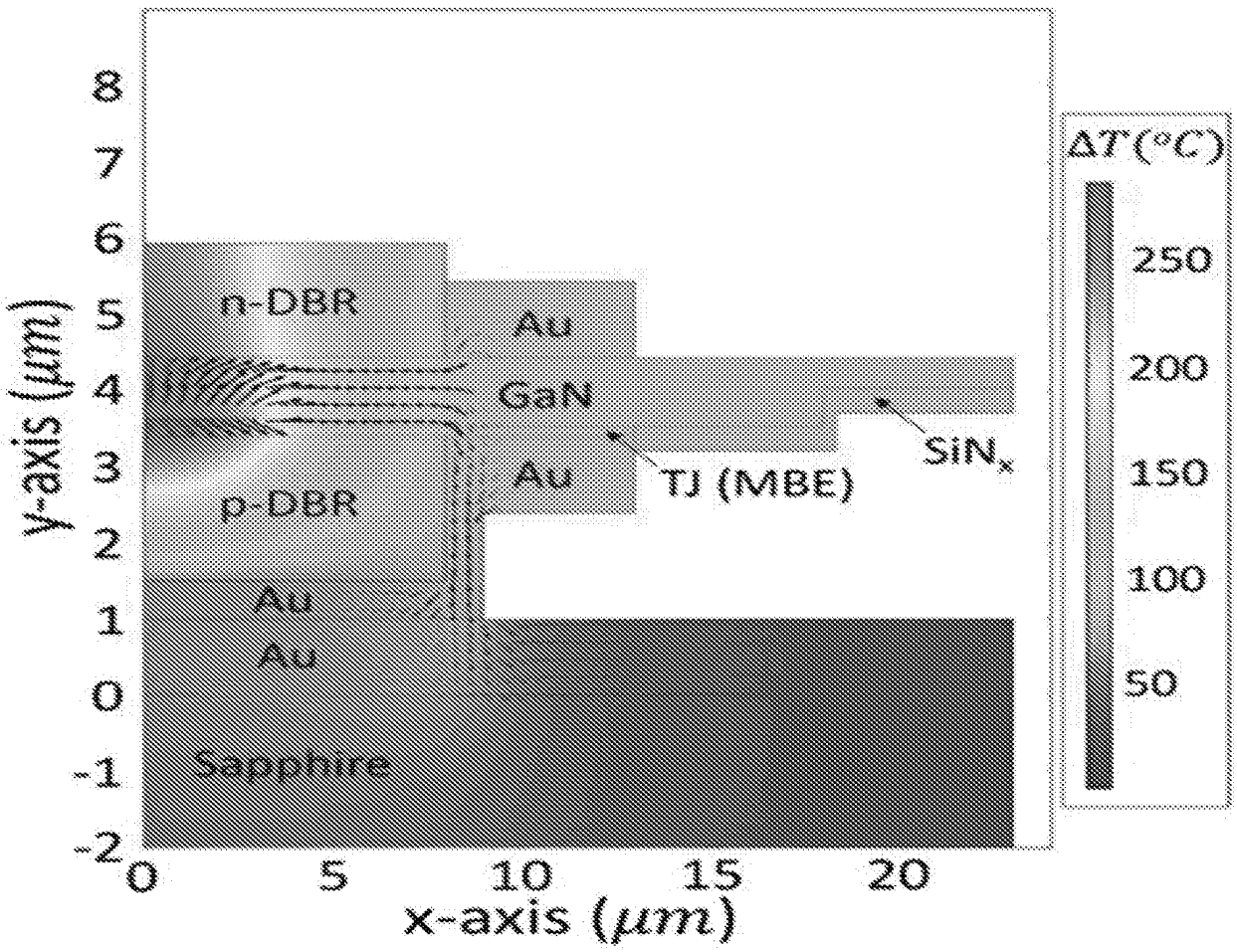
n-DBR
Au
GaN
Au
TJ (MBE)
SiNx
p-DBR
Au
Au
Sapphire
Y-axis (μm)
x-axis (μm)
ΔT (°C)
250
200
150
100
50
8
7
6
5
4
3
2
1
0
-1
-2
0
5
10
15
20

FIG. 9

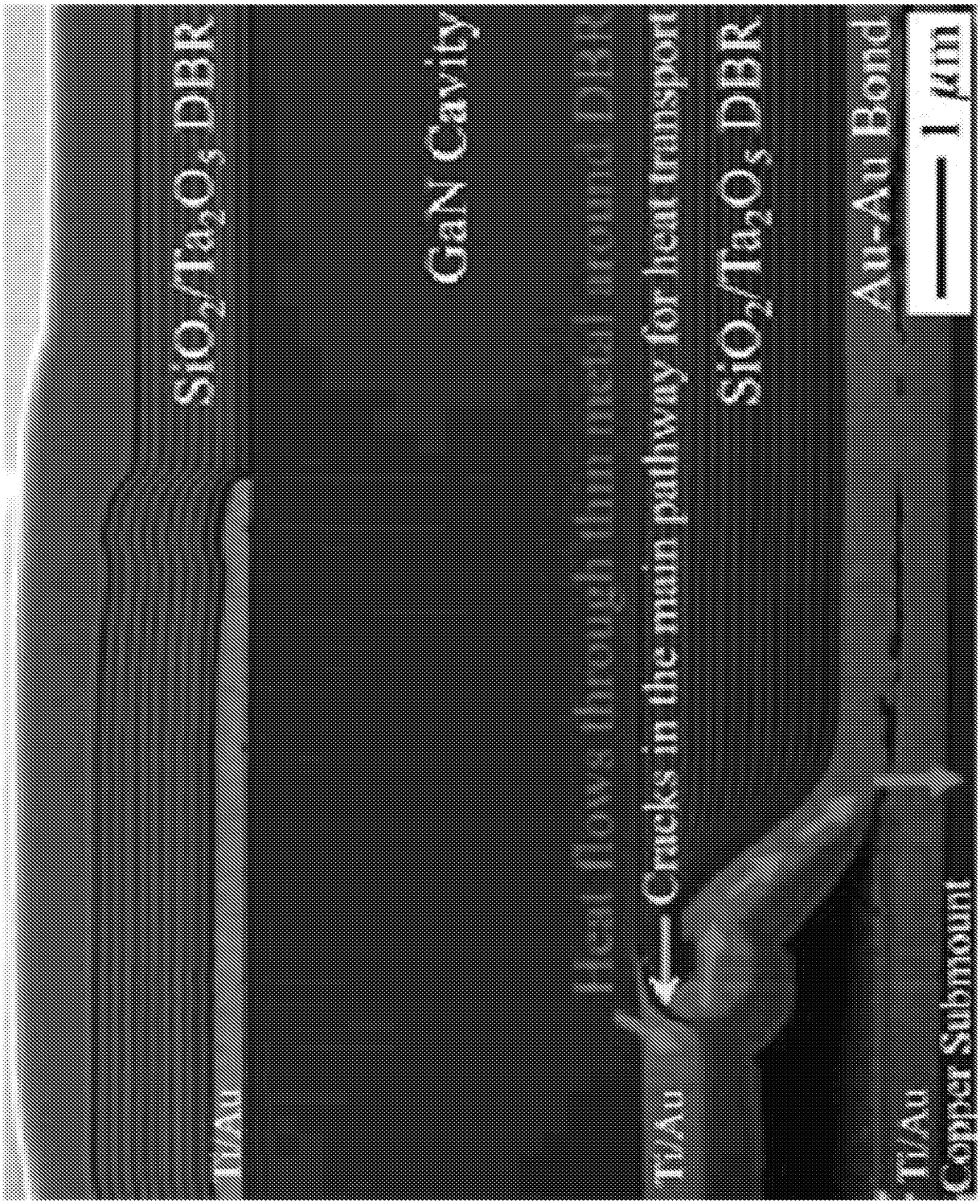
SiO2/Ta2O5 DBR
Ti/Au
GaN Cavity
Cracks in the main pathway for heat transport
SiO2/Ta2O5 DBR
Au-Au Bond
Ti/Au
Copper Submount
1 μm

FIG. 10

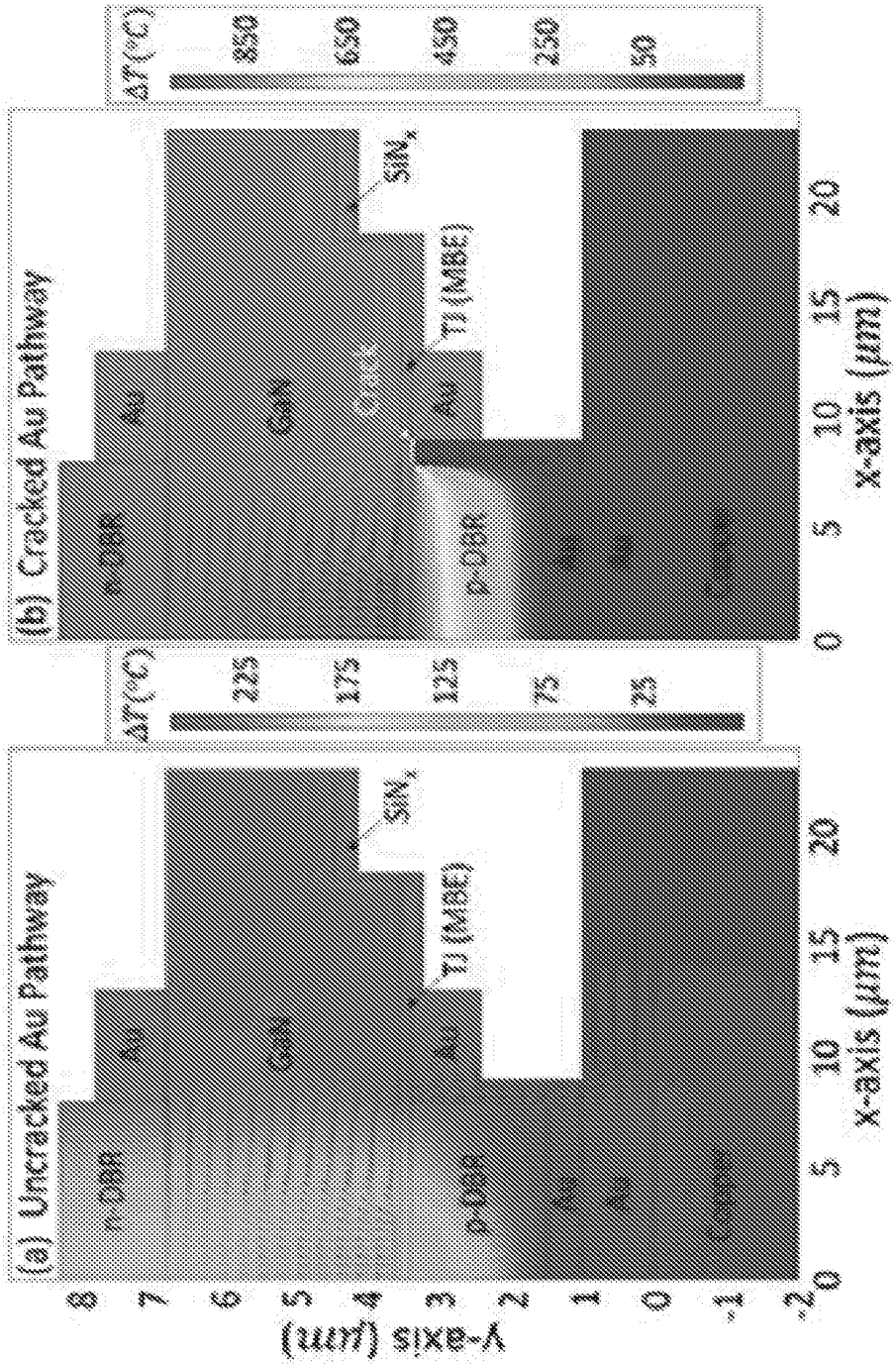

FIG. 11A

FIG. 11B

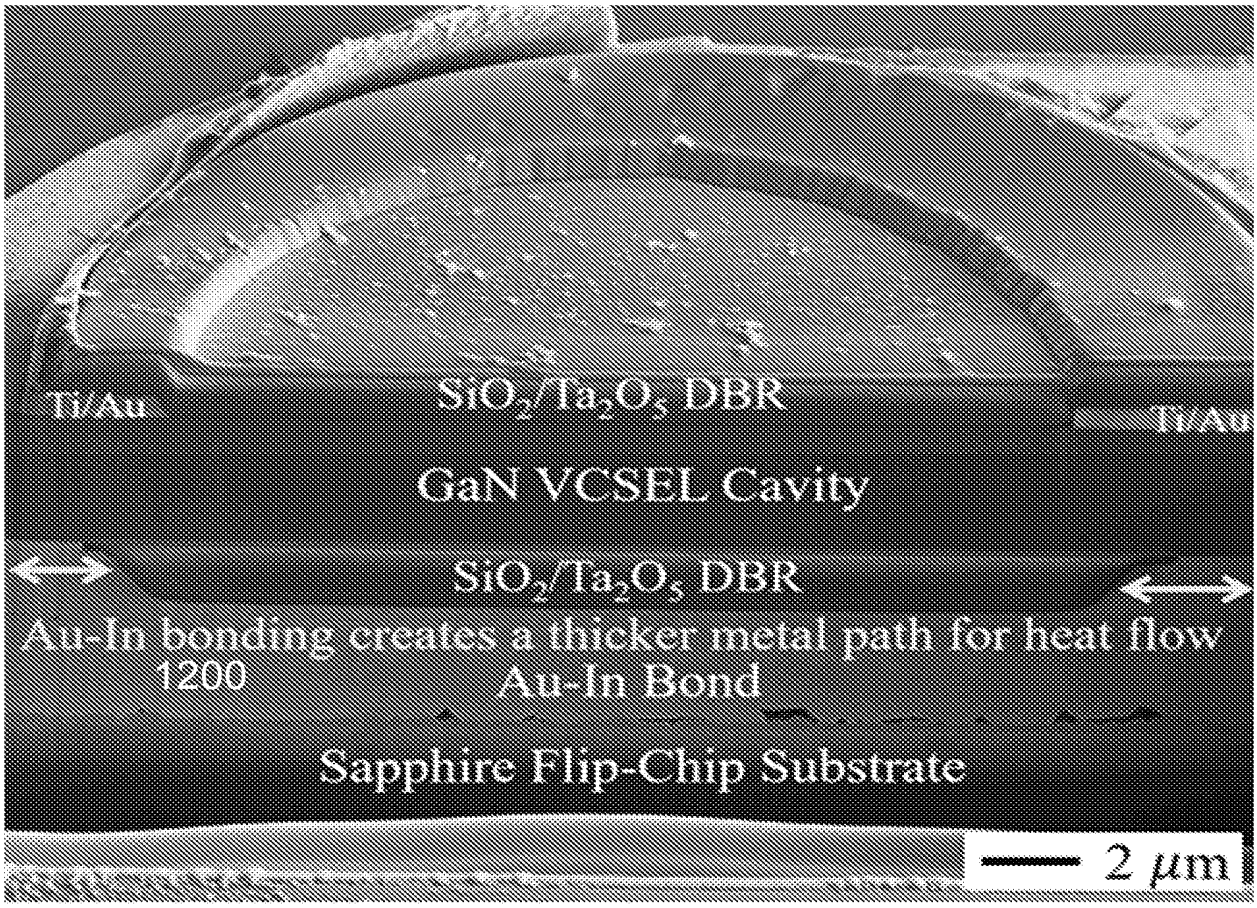
Ti/Au
SiO_2/Ta_2O_5 DBR
Ti/Au
GaN VCSEL Cavity
SiO_2/Ta_2O_5 DBR
Au-In bonding creates a thicker metal path for heat flow
1200
Au-In Bond
Sapphire Flip-Chip Substrate
2 μm

FIG. 12

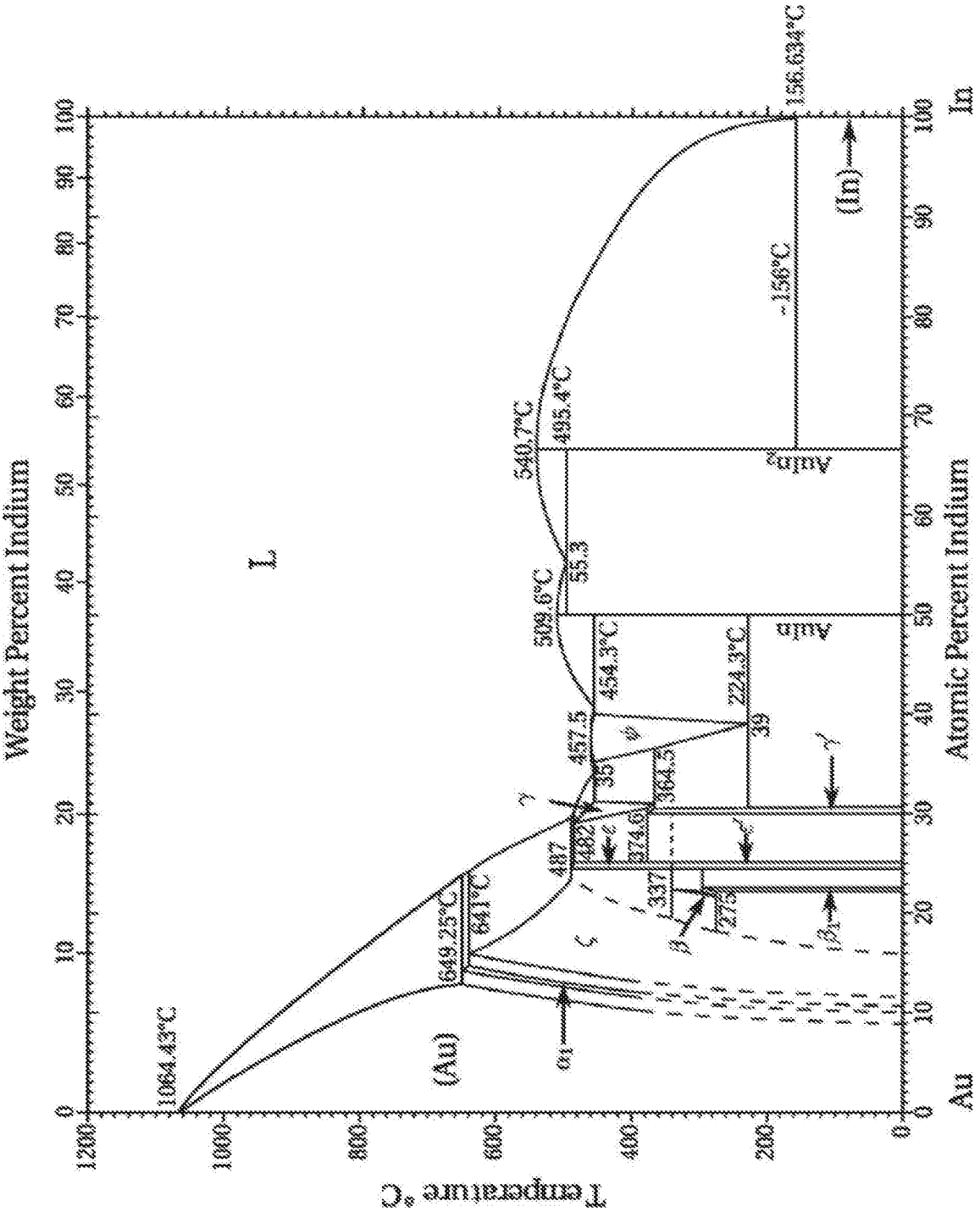
Weight Percent Indium
Atomic Percent Indium
Temperature °C
Au
In
L
(Au)
(In)
1064.43°C
649.25°C
64.1°C
540.7°C
495.4°C
309.6°C
55.3
454.3°C
224.3°C
457.5
39
364.5
487
374.6
337
275
156.634°C
~156°C
AuIn_2
AuIn
α_1
α_2
β
γ
ζ
η
ε

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/053902

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01S 5/183; H01S 5/18 (2019.01)
CPC - H01S 5/1838; H01S 5/183 (2019.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 228/193; 228/195; 372/34; 372/36; 372/38.07; 372/50.124 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/0072009 A1 (WUNDERER et al) 13 March 2014 (13.03.2014) entire document	1, 31, 32
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Y		2-12, 22-24
Y	US 2009/0120997 A1 (OUDAR et al) 14 May 2009 (14.05.2009) entire document	2-10, 22-24
Y	US 2007/0051939 A1 (NAKAHARA et al) 08 March 2007 (08.03.2007) entire document	11, 12
A	US 2012/0163138 A1 (GAGE et al) 28 June 2012 (28.06.2012) entire document	1-12, 22-24, 31, 32
A	US 2002/0105997 A1 (ZHANG) 08 August 2002 (08.08.2002) entire document	1-12, 22-24, 31, 32

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2019	12 FEB 2019
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/053982

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 13-19, 28-30
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See extra sheet(s).

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-12, 22-24, 31, 32

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/053982

Continued from Box No. III Observations where unity of invention is lacking

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1-12, 22-24 and 31-32 are drawn to a device, comprising: a mount; a Vertical Cavity Surface Emitting Laser (VCSEL) on the mount; and a thermally conductive bond between the mount and the VCSEL.

Group II, claims 20-21, 25-27 and 33, are drawn to a VCSEL comprising: a first mirror and a second mirror defining a cavity for electromagnetic radiation emitted from the VCSEL.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: a mount; a Vertical Cavity Surface Emitting Laser (VCSEL) on the mount; and a thermally conductive bond between the mount and the VCSEL, the bond comprising a layer of metal having a thermal conductivity such that heat, generated during operation of the VCSEL, is transferred from the VCSEL to the mount and the VCSEL emits continuous wave electromagnetic radiation as claimed therein is not present in the invention of Group II. The special technical feature of the Group II invention: a first mirror and a second mirror defining a cavity for electromagnetic radiation emitted from the VCSEL; a flip chip substrate: a metal layer between the VCSEL and the flip chip substrate, wherein: the metal layer includes indium and gold, and the first mirror or the second mirror is embedded in the metal layer as claimed therein is not present in the invention of Group I.

Groups I and II lack unity of invention because even though the inventions of these groups require the technical feature of a Vertical Cavity Surface Emitting Laser (VCSEL emitting electromagnetic radiation, this technical feature is not a special technical feature as it does not make a contribution over the prior art.

Specifically, US 2012/0163138 to Gage et al. teaches a Vertical Cavity Surface Emitting Laser (VCSEL emitting electromagnetic radiation (Paras. [0004], [0025]).

Since none of the special technical features of the Group I or II inventions are found in more than one of the inventions, unity of invention is lacking.