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(54) Title: METHOD TO REDUCE PORE DIAMETER USING ATOMIC LAYER DEPOSITION AND ETCHING

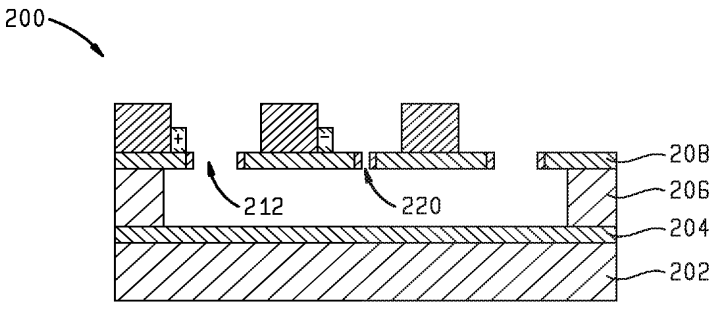

FIG. 2K

(57) Abstract: Methods are provided for manufacturing well-controlled, solid-state nanopores and arrays of well-controlled, solid-state nanopores by a cyclic process including atomic layer deposition (ALD), or chemical vapor deposition (CVD), and etching. One or more features are formed in a thin film deposited on a topside of a substrate. A dielectric material is deposited over the substrate having the one or more features in the thin film. An etching process is then used to etch a portion of the dielectric material deposited over the substrate having the one or more features in the thin film. The dielectric material deposition and etching processes are optionally repeated to reduce the size of the features until a well-controlled nanopore is formed through the thin film on the substrate.

WO 2019/060172 A1

METHOD TO REDUCE PORE DIAMETER USING ATOMIC LAYER DEPOSITION AND ETCHING

BACKGROUND

Field

[0001] Aspects disclosed herein relate to methods of manufacturing well-controlled, solid-state nanopores and arrays of well-controlled, solid-state nanopores by cyclic atomic layer deposition (ALD), or chemical vapor deposition (CVD), and etching.

Description of the Related Art

[0002] Nanopores are widely used for applications such as deoxyribonucleic acid (DNA) and ribonucleic acid (RNA) sequencing. In one example, nanopore sequencing is performed using an electrical detection method, which generally includes transporting an unknown sample through the nanopore, which is immersed in a conducting fluid, and applying electric potential across the nanopore. Electric current resulting from the conduction of ions through the nanopore is measured. The magnitude of the electric current density across a nanopore surface depends on the nanopore dimensions and the composition of the sample, such as DNA or RNA, which is occupying the nanopore at the time. Different nucleotides cause characteristic changes in electric current density across nanopore surfaces. These electric current changes are measured and used to sequence the DNA or RNA sample.

[0003] Various methods have been used for biological sequencing. Sequencing by synthesis, or second generation sequencing, is used to identify which bases have attached to a single strand of DNA. Third generation sequencing, which generally includes threading an entire DNA strand through a single pore, is used to directly read the DNA. Some sequencing methods require the DNA or RNA sample to be cut up and then reassembled. Additionally, some

sequencing methods use biological membranes and biological pores, which have shelf lives and must be kept cold prior to use.

[0004] Solid-state nanopores, which are nanometer-sized pores formed on a free-standing membrane such as silicon nitride or silicon oxide, have recently been used for sequencing. Current solid-state nanopore fabrication methods, such as using a tunneling electron microscope, focused ion beam, or electron beam, however, cannot easily and cheaply achieve the size and position control requirements necessary for manufacturing arrays of nanopores. Additionally, current nanopore fabrication methods are time consuming.

[0005] Therefore, there is a need in the art for improved methods of manufacturing a well-controlled, solid-state nanopore and arrays of well-controlled, solid-state nanopores.

SUMMARY

[0006] Methods are provided for manufacturing well-controlled, solid-state nanopores and arrays of well-controlled, solid-state nanopores by a cyclic process including atomic layer deposition (ALD), or chemical vapor deposition (CVD), and etching. One or more features are formed in a thin film deposited on a topside of a substrate. A dielectric material is deposited over the substrate having the one or more features in the thin film. An etching process is then used to etch a portion of the dielectric material deposited over the substrate having the one or more features in the thin film. The dielectric material deposition and etching processes are optionally repeated to reduce the size of the features until a well-controlled nanopore is formed through the thin film on the substrate.

[0007] In one aspect, a method for forming a nanopore is provided. The method includes providing a substrate having at least one feature formed in a thin film deposited on a topside thereof, the feature having one or more sidewalls and a bottom, depositing a first amount of dielectric material over the substrate

having the at least one feature and etching a first portion of the first amount of dielectric material on the bottom of the at least one feature.

[0008] In another aspect, a method for forming a nanopore is provided. The method includes providing a substrate having at least one feature formed in a thin film deposited on a topside thereof, the feature having one or more sidewalls and a bottom, depositing a first amount of dielectric material over the substrate having the at least one feature, etching a first portion of the first amount of dielectric material on the bottom of the at least one feature, depositing a second amount of dielectric material over the substrate having the at least one feature, and etching a second portion of the second amount of dielectric material on the bottom of the at least one feature to form at least one nanopore.

[0009] In yet another aspect, a substrate is provided. The substrate includes a first silicon layer and a second silicon layer, an dielectric layer disposed between the first silicon layer and the second silicon layer; and a thin film disposed over the second silicon layer. The thin film includes at least one first feature formed therethrough, the at least one first feature having one or more sidewalls and a bottom, a plurality of second features formed therethrough, each of the plurality of second features having one or more sidewalls and a bottom, and a dielectric material disposed on the sidewalls of the at least one first feature and the sidewalls of the plurality of second features such that the at least one first feature has a first diameter and the plurality of second features have a second diameter, the first diameter being less than the second diameter, the first diameter corresponding to a nanopore formed in the thin film.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to aspects, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary aspects and are therefore not to

be considered limiting of its scope, and may admit to other equally effective aspects.

[0011] Figure 1 is a process flow of a method for forming one or more nanopores according to the present disclosure.

[0012] Figures 2A-2K depict cross-sectional views of a substrate on which one or more nanopores are formed at various stages of a process flow disclosed herein.

[0013] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one aspect may be beneficially incorporated in other aspects without further recitation.

DETAILED DESCRIPTION

[0014] Methods are provided for manufacturing well-controlled, solid-state nanopores and arrays of well-controlled, solid-state nanopores by a process including atomic layer deposition (ALD) and etching. One or more features are formed in a thin film deposited on a topside of a substrate. A dielectric material is deposited over the substrate having the one or more features in the thin film using ALD. An etching process is then used to etch a portion of the dielectric material deposited over the substrate having the one or more features in the thin film. The dielectric material ALD and etching processes are repeated to reduce the size of the features until a well-controlled nanopore is formed through the thin film on the substrate.

[0015] Methods described herein refer to formation of nanopores on a semiconductor substrate as an example. It is also contemplated that the described methods are useful to form other pore-like structures on various materials, including solid-state and biological materials. Methods described herein refer to formation of one or more trenches or tubes as examples; however,

other etched features and any combinations thereof are also contemplated. For illustrative purposes a silicon on insulator (SOI) substrate with a silicon oxide layer is described; however, any suitable substrate materials and dielectric materials are also contemplated. Additionally, methods described herein refer to a topside and a backside of the substrate. The topside and backside generally refer to opposite sides of the substrate and do not necessarily refer to an upward or downward orientation.

[0016] Figure 1 is a process flow of a method 100 for forming one or more nanopores according to the present disclosure. Prior to method 100, a substrate is processed. A thin film is deposited over a topside of the substrate and one or more features are patterned in the thin film over the topside of the substrate. At operation 110, the substrate having one or more features patterned in the thin film over the topside of the substrate is provided. At operation 120, a first amount of dielectric material is deposited over the substrate having one or more features in the thin film on the topside thereof. At operation 130, a portion of the deposited dielectric material is etched, such as the portion of deposited dielectric material at the bottom of the one or more features. A portion of the deposited dielectric material, such as the portion of deposited dielectric material on the one or more sidewalls of the one or more features, remains on the substrate. Operation 120 and operation 130 are optionally cyclically repeated until a well-controlled nanopore is formed on the topside of the substrate at operation 140. For example, in one aspect, a second amount of dielectric material is deposited over the substrate having the one or more features patterned in the thin film thereof and then a portion of the second amount of dielectric material is etched from the substrate. In one example, the dielectric material deposition and etching processes are repeated any suitable number of times to form a well-controlled nanopore. In further examples, one full cycle of deposition and etching will be suitable to form a well-controlled nanopore at or near the center of the one or more features

[0017] The substrate is generally any suitable substrate, such as a doped or undoped silicon (Si) substrate. The thin film deposited over the topside of the substrate is generally any suitable thin film. The thin film is generally deposited by any suitable deposition process, including but not limited to, atomic layer deposition or chemical vapor deposition and is of any suitable thickness. Patterning the one or more features in the deposited dielectric thin film is accomplished by any suitable patterning process, including but not limited to, standard photolithography. The one or more features that are patterned are generally any suitable size and shape, such as trenches or tubes. In one aspect, the one or more features are of various width, such as a first width and a second width, or of various diameters, such as a first diameter and a second diameter. Any suitable etching process is generally used to etch the portion of the dielectric materials. Suitable etching processes include, but are not limited to, dry etching processes, for example reactive ion etching (RIE). Operation 120 and operation 130 are optionally repeated any suitable number of times to form a well-controlled nanopore at or near a center of the one or more features. In some aspects, one full cycle of deposition and etching will be suitable to form a nanopore at or near the center of the one or more features; however, in other aspects, multiple repetitions of the cycles will be suitable to form a nanopore at the center of the one or more features, depending on the size of the nanopore to be formed. Further substrate processing may be performed at the conclusion of method 100. For example, a selective etch process may be used to remove a portion of the substrate.

[0018] Figures 2A-2K depict cross-sectional views of a substrate 200 on which one or more nanopores are formed according to a process flow disclosed herein, such as at various stages of the process flow 100.

[0019] As shown in Figure 2A, a dielectric layer 204 is deposited over a first Si layer 202. As shown in Figure 2B, a second Si layer 206 is deposited over the dielectric layer 204 to provide a silicon on insulator (SOI) substrate.

[0020] A thin film 208 is then deposited over the second Si layer 206, as shown in Figure 2C. The thin film 208 is generally deposited by any suitable deposition process, including but not limited to ALD, and generally has a thickness between about 1 nanometer (nm) and about 10 nm, for example between about 2 nm about 6 nm, such as about 5 nm. In the example of Figure 2C, the thin film 208 is a silicon-containing film.

[0021] As shown in Figure 2D, the thin film 208 is patterned with at least one first feature 210 (one is shown) and one or more second features 212 (two are shown). In the example of Figure 2D, the first feature 210 has a first width or diameter and the second features 212 have a second width or diameter. The first feature 210 includes one or more sidewalls 214 and a bottom 216, which corresponds to a first surface of the second Si layer 206, as shown in Figure 2E, which is an enlarged portion of Figure 2D. The first width or diameter is generally between about 10 nanometers (nm) and about 100 nm, for example, between about 20 nm and about 60 nm, such as about 50 nm. The second width or diameter is generally between about 0.5 microns (μm) and about 100 μm, such as about 1 μm.

[0022] A dielectric material 218 is deposited over the substrate 200, as shown in Figure 2F. The dielectric material 218 is generally conformally deposited by ALD or CVD and covers the thin film 208 as well as the exposed portion of the second Si layer 206, or bottom 216 of the one or more first features 210.

[0023] An RIE etching process is then performed to remove a portion of the dielectric material 218, as shown in Figure 2G. The RIE generally removes a portion of the dielectric material 218 on the bottom 216 of the first feature 210, or the first surface of the second Si layer 206 and does not etch the dielectric material 218 deposited on the sidewalls 214.

[0024] The ALD or CVD of dielectric material and subsequent RIE etch are optionally cyclically repeated until a nanopore 220 is formed at or near the center of each of the one or more first features 210, as shown in Figure 2G and Figure

2H. As shown in the example of Figure 2H, the cyclic processes generally form a funnel-shaped gap between the dielectric material 218 deposited on the sidewalls 214. The nanopore 220 is generally formed at the bottom of the funnel-shaped gap at or near the center of the first feature 210.

[0025] By using cyclic ALD and etch processes, the dielectric material 218 is selectively deposited on the sidewalls 214 of the first features 210 formed on the substrate 200. Being able to selectively deposit the dielectric material 218 on the sidewalls 214 provides the ability to shrink the size of the nanopore 220 very controllably. A well-controlled size of the nanopore 220 is generally a diameter or width suitable for sequencing a sample of a certain size. In one aspect, the size of the nanopore 220 is about 100 nm or less, such as 50 nm or less. In one aspect, the size of the nanopore 220 is between about 0.5 nm and about 5 nm, for example between about 1 nm and about 3 nm, such as 2 nm. In another aspect, the size of the nanopore 220 is between about 1.5 nm and about 1.8 nm, such as about 1.6 nm, which is roughly the size of a single strand of DNA. In another aspect, the size of the nanopore 220 is between about 2 nm and about 3 nm, such as about 2.8 nm, which is roughly the size of double-stranded DNA. A well-controlled position of the nanopore 220 is generally any position on the substrate which is suitable for configuration of one or more nanopores. The disclosed deposition and etch processes also allow the length of the nanopore to remain constant, which provides for improved signal-to-noise ratio during processes, such as DNA sequencing. Additionally, methods disclosed herein are generally used to control the position of each of the one or more nanopores 220 such that a nanopore array of desired configuration for sequencing or other processes is formed.

[0026] The substrate 200 may be further processed after the one or more nanopores 220 are formed. For example, a portion of the second Si layer 206 may be selectively etched such that a thin film membrane of thin film 208 have one or more nanopores 220 formed therein remains, as shown in Figure 2J. One or more additional layers may be deposited over at least a portion of the thin film

membrane, for example a silicon nitride (SiN) layer and positive and negative electrodes, for sequencing processes, as shown in Figure 2K. The one or more additional layers may be deposited at any stage of the process flows disclosed herein.

[0027] Benefits of the present disclosure include the ability to quickly form well-controlled nanopores and nanopore arrays, which are generally individually addressable. Disclosed methods generally provide nanopores that are well-controlled in size and in position through a thin membrane. Methods of manufacturing nanopores of well-controlled size provide improved signal-to-noise ratios because the size of the nanopore is similar to the size of the sample, such as a single strand of DNA, being transmitted through the nanopore, which increases the change in electric current passing through the nanopore. Additionally, methods of manufacturing nanopores having well-controlled positions enables a sample, such as DNA, to freely pass through the nanopore. The thinness of the membrane, which is generally between about 1 nm and about 10 nm, for example between about 1 nm and about 5 nm, such as about 1 nm, provides for improved reading of the DNA sequence.

[0028] While the foregoing is directed to aspects of the present disclosure, other and further aspects of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method for forming a nanopore, comprising:

providing a substrate having at least one feature formed in a thin film deposited on a topside thereof, the feature having one or more sidewalls and a bottom;

depositing a first amount of dielectric material over the substrate having the at least one feature; and

etching a first portion of the first amount of dielectric material on the bottom of the at least one feature.

2. The method of claim 1, wherein the method further comprises:

repeating the depositing of the first amount of dielectric material and the etching the first portion of the first amount of dielectric material on the bottom until at least one nanopore is formed between the first amount of dielectric material deposited on the one or more sidewalls at or near a center of at least one feature.

3. The method of claim 1, wherein depositing the first amount of dielectric material is accomplished by atomic layer deposition or chemical vapor deposition.

4. The method of claim 1, wherein etching the first amount of dielectric material is accomplished by dry etching.

5. The method of claim 1, wherein a size of the nanopore is less than about 100 nanometers.

6. The method of claim 1, wherein the method further comprises:

selectively removing a portion of the substrate underneath the nanopore.

7. A method for forming a nanopore, comprising:

providing a substrate having at least one feature formed in a thin film deposited on a topside thereof, the feature having one or more sidewalls and a bottom;

depositing a first amount of dielectric material over the substrate having the at least one feature;

etching a first portion of the first amount of dielectric material on the bottom of the at least one feature;

depositing a second amount of dielectric material over the substrate having the at least one feature; and

etching a second portion of the second amount of dielectric material on the bottom of the at least one feature to form at least one nanopore.

8. The method of claim 7, wherein depositing the first amount of dielectric material and depositing the second amount of dielectric material is accomplished by atomic layer deposition or chemical vapor deposition.

9. The method of claim 7, wherein etching the first portion of the first amount of dielectric material and etching the second portion of the second amount of dielectric material is accomplished by dry etching.

10. The method of claim 7, further comprising:

depositing a third amount of dielectric material over the substrate having the at least one feature; and

etching a third portion of the third amount of dielectric material on the bottom of the at least one feature to form at least one nanopore.

11. The method of claim 7, further comprising:

selectively removing a portion of the substrate underneath the at least one nanopore.

12. The method of claim 7, wherein a size of the nanopore is less than about 50 nanometers.

13. A substrate, comprising:

a first silicon layer and a second silicon layer;

a dielectric layer disposed between the first silicon layer and the second silicon layer; and

a thin film disposed over the second silicon layer, the thin film comprising:

at least one first feature formed therethrough, the at least one first feature having one or more sidewalls and a bottom;

a plurality of second features formed therethrough, each of the plurality of second features having one or more sidewalls and a bottom; and

a dielectric material disposed on the sidewalls of the at least one first feature and the sidewalls of the plurality of second features such that the at least one first feature has a first diameter and the plurality of second features have a second diameter, the first diameter being less than the second diameter, the first diameter corresponding to a nanopore formed in the thin film.

14. The substrate of claim 13, wherein a portion of the second silicon layer below the at least one first feature and the plurality of second features has been selectively removed.

15. The substrate of claim 13, further comprising:

one or more additional layers disposed over at least a portion of the thin film;

at least one positive electrode disposed over the thin film over at least a portion of the thin film; and

at least one negative electrode disposed over at least a portion of the thin film.

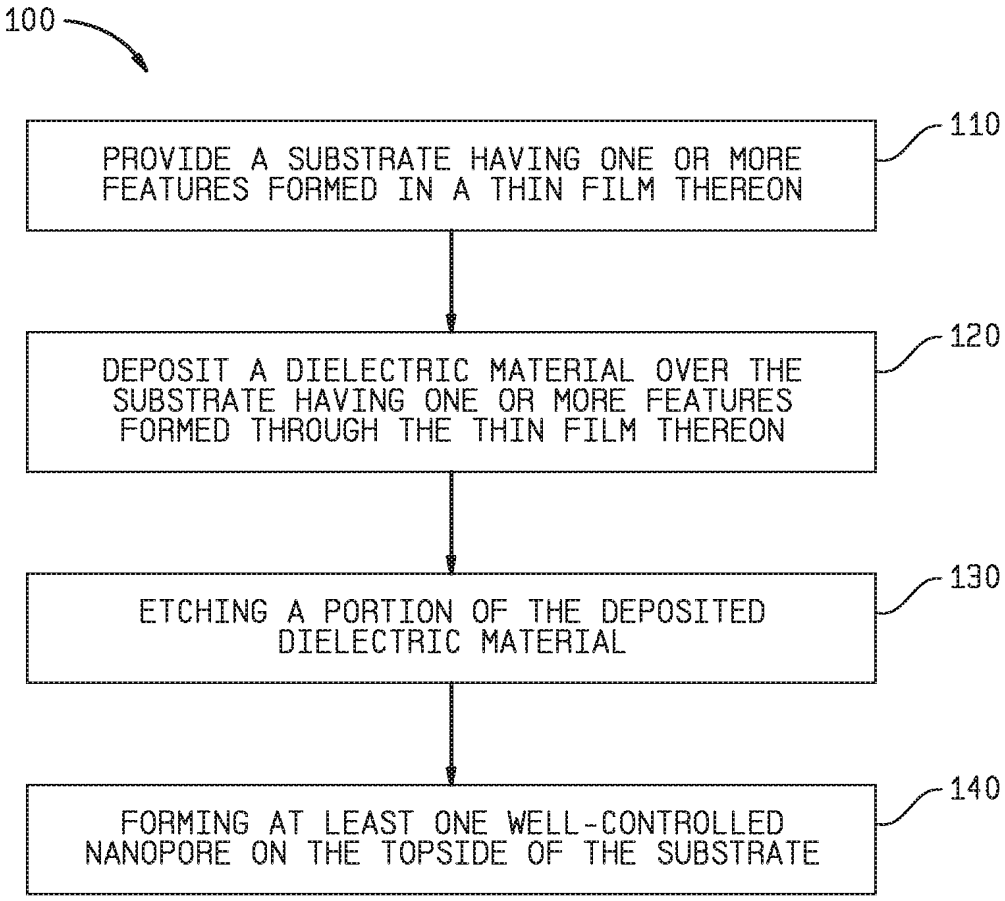
100
PROVIDE A SUBSTRATE HAVING ONE OR MORE FEATURES FORMED IN A THIN FILM THEREON
110
DEPOSIT A DIELECTRIC MATERIAL OVER THE SUBSTRATE HAVING ONE OR MORE FEATURES FORMED THROUGH THE THIN FILM THEREON
120
ETCHING A PORTION OF THE DEPOSITED DIELECTRIC MATERIAL
130
FORMING AT LEAST ONE WELL-CONTROLLED NANOPORE ON THE TOPSIDE OF THE SUBSTRATE
140

FIG. 1

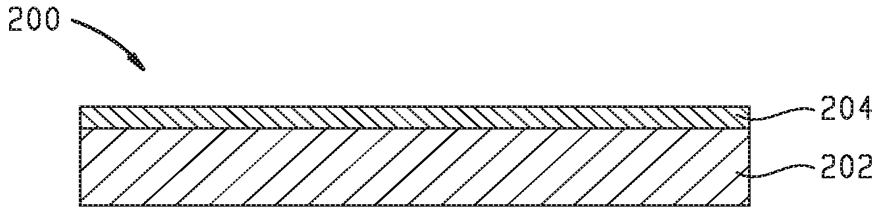

FIG. 2A

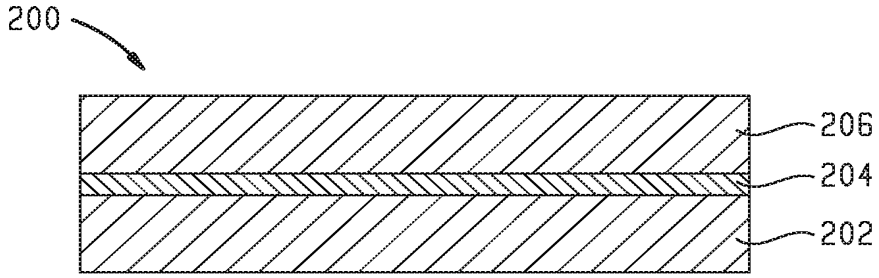

FIG. 2B

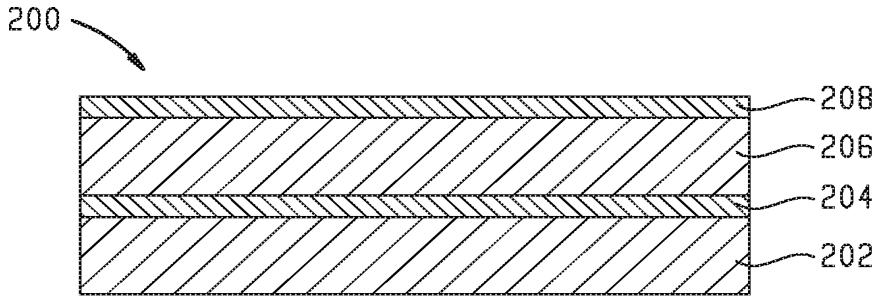

FIG. 2C

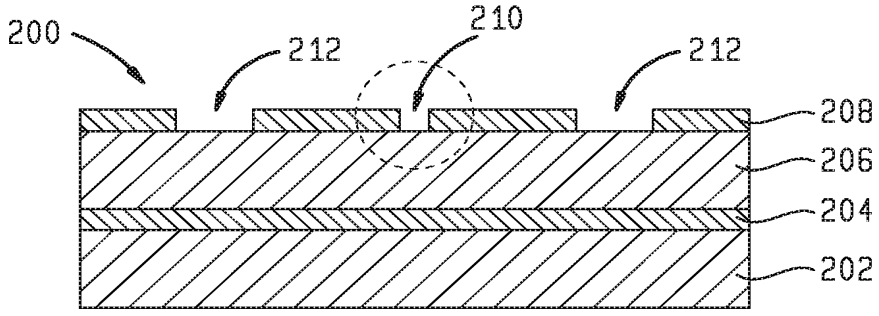

FIG. 2D

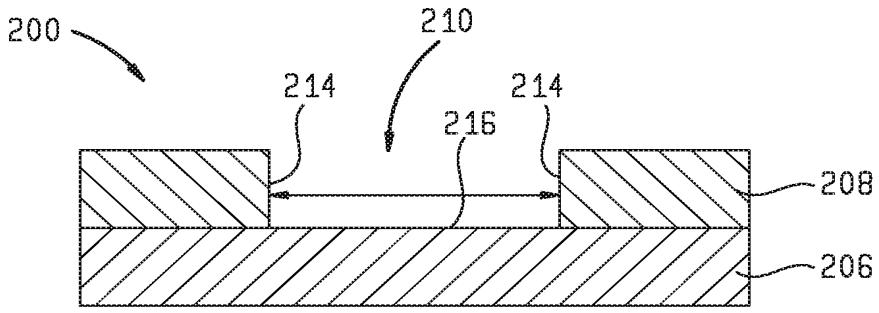

FIG. 2E

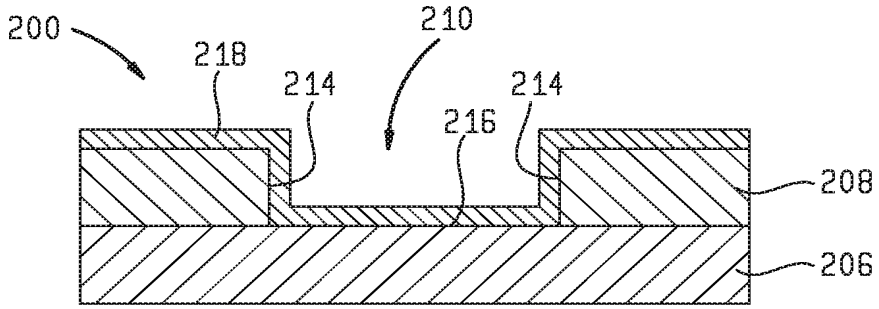

FIG. 2F

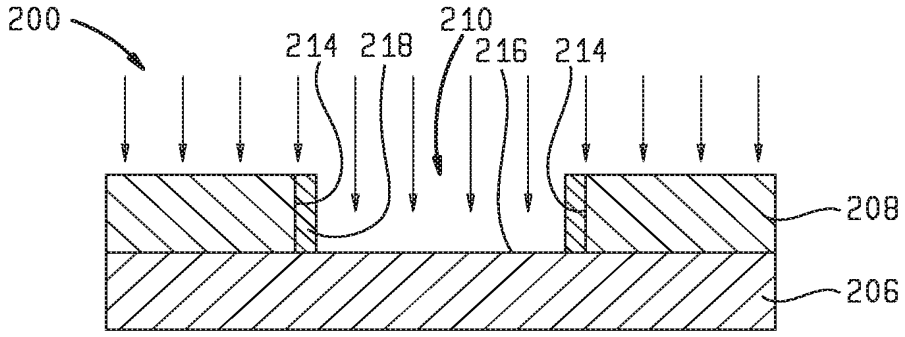

FIG. 2G

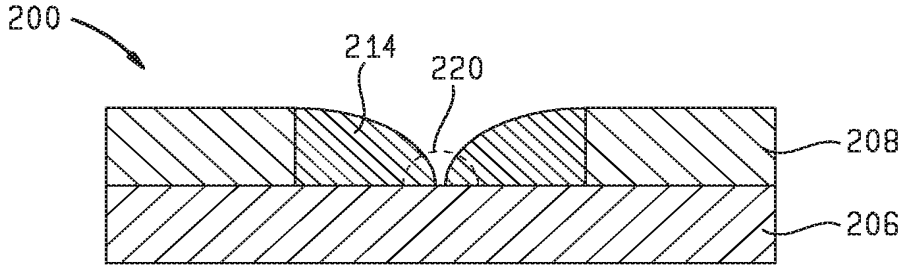

FIG. 2H

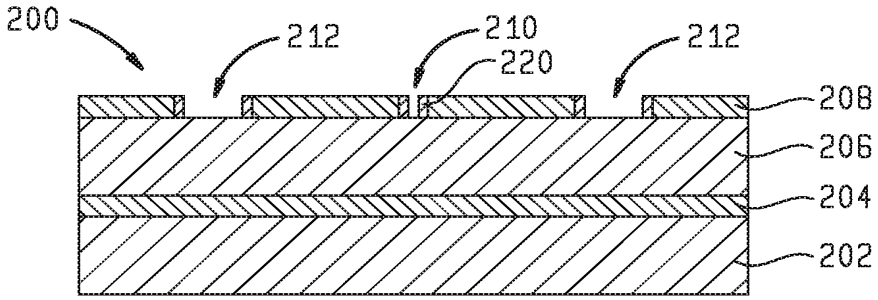

FIG. 2I

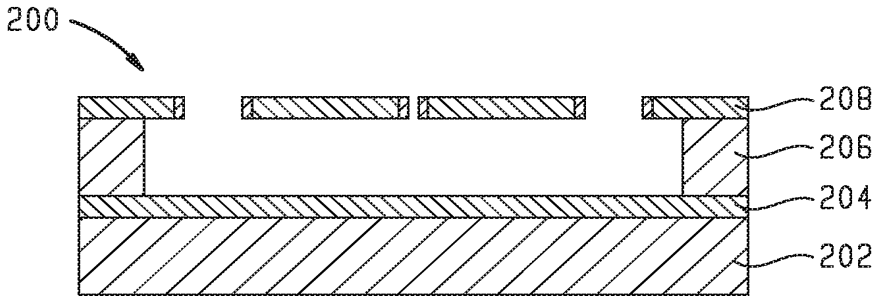

FIG. 2J

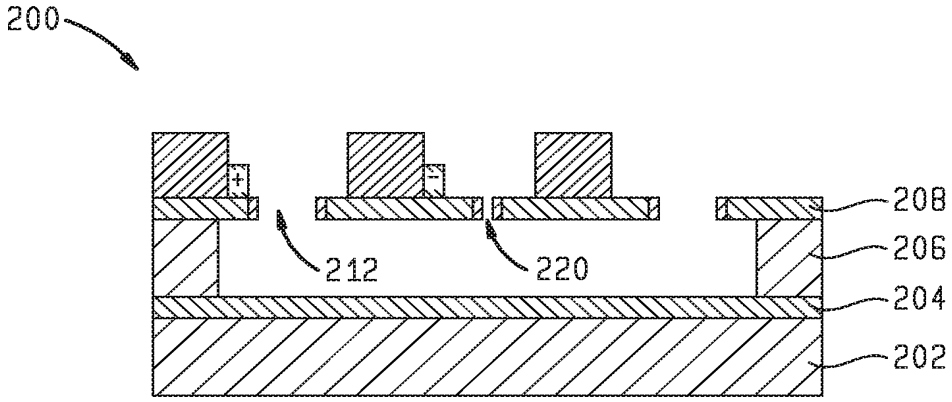

FIG. 2K

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/050405

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/3065(2006.01)i, H01L 21/027(2006.01)i, H01L 21/02(2006.01)i, G03F 7/00(2006.01)i, H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/3065; H01L 21/027; H01L 21/28; H01L 21/311; H01L 21/50; H01L 21/768; G03F 7/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: nanopore, feature, dielectric material, diameter

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0108068 A1 (STEVEN ALAN LYTLE) 03 May 2012 See paragraphs [0020]-[0029], claim 19 and figures 2, 4A-4E.	1,3-6
Y		2,7-15
Y	KR 10-1999-0039740 A (HYUNDAI MICRO ELECTRONICS CO., LTD.) 05 June 1999 See page 2 and figures 2a-2d.	2,7-12
Y	US 2009-0233395 A1 (SUNG-GYU PYO et al.) 17 September 2009 See paragraphs [0063]-[0067] and figures 5-6I.	13-15
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☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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02 January 2019 (02.01.2019)	**02 January 2019 (02.01.2019)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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