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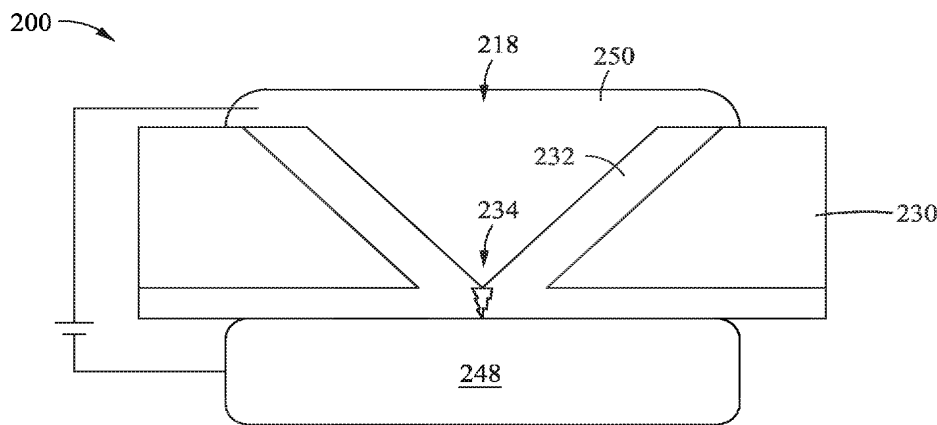


Fig. 2L

(57) Abstract: Methods are provided for manufacturing well-controlled, solid-state nanopores and arrays thereof. In one aspect, methods for manufacturing nanopores and arrays thereof exploit a physical seam. One or more etch pits are formed in a topside of a substrate and one or more trenches, which align with the one or more etch pits, are formed in a backside of the substrate. An opening is formed between the one or more etch pits and the one or more trenches. A dielectric material is then formed over the substrate to fill the opening. Contacts are then disposed on the topside and the backside of the substrate and a voltage is applied from the topside to the backside, or vice versa, through the dielectric material to form a nanopore. In another aspect, the nanopore is formed at or near the center of the opening at a seam, which is formed in the dielectric material.



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PORE FORMATION IN A SUBSTRATE

BACKGROUND

Field

[0001] Aspects disclosed herein relate to methods of manufacturing well-controlled, solid-state nanopores and arrays of well-controlled, solid-state nanopores in a substrate.

Description of the Related Art

[0002] Nanopores are widely used for applications such as deoxyribonucleic acid (DNA) and ribonucleic acid (RNA) sequencing. In one example, nanopore sequencing is performed using an electrical detection method, which generally includes transporting an unknown sample through the nanopore, which is immersed in a conducting fluid, and applying electric potential across the nanopore. Electric current resulting from the conduction of ions through the nanopore is measured. The magnitude of the electric current density across a nanopore surface depends on the nanopore dimensions and the composition of the sample, such as DNA or RNA, which is occupying the nanopore at the time. Different nucleotides cause characteristic changes in electric current density across nanopore surfaces. These electric current changes are measured and used to sequence the DNA or RNA sample.

[0003] Various methods have been used for biological sequencing. Sequencing by synthesis, or second generation sequencing, is used to identify which bases have attached to a single strand of DNA. Third generation sequencing, which generally includes threading an entire DNA strand through a single pore, is used to directly read the DNA. Some sequencing methods require the DNA or RNA sample to be cut up and then reassembled. Additionally, some sequencing methods use biological membranes and biological pores, which have shelf lives and must be kept cold prior to use.

[0004] Solid-state nanopores, which are nanometer-sized pores formed on a free-standing membrane such as silicon nitride or silicon oxide, have recently been used for sequencing. Current solid-state nanopore fabrication methods, such as using a tunneling electron microscope, focused ion beam, or electron beam, however, cannot easily and cheaply achieve the size and position control requirements necessary for manufacturing arrays of nanopores. Additionally, current nanopore fabrication methods are time consuming.

[0005] Therefore, there is a need in the art for improved methods of manufacturing a well-controlled, solid-state nanopore and arrays of well-controlled, solid-state nanopores.

SUMMARY

[0006] Methods are provided for manufacturing well-controlled, solid-state nanopores and arrays of well-controlled, solid-state nanopores. In one aspect, methods for manufacturing nanopores and arrays of nanopores exploit a physical seam. One or more etch pits are formed in a topside of a substrate and one or more trenches, which align with the one or more etch pits, are formed in a backside of the substrate. An opening is formed between the one or more etch pits and the one or more trenches. A dielectric material is then formed over the substrate, for example, by oxidation or atomic layer deposition, to fill the opening. Contacts are then formed or placed on the topside and the backside of the substrate and a voltage is applied from the topside to the backside of the substrate, or vice versa, through the dielectric material to form a nanopore. In another aspect, the nanopore is formed at or near the center of the opening at a seam, which is formed in the dielectric material.

[0007] In one aspect, a method for forming a nanopore is provided. The method generally includes providing a substrate having at least one feature on a topside and at least one feature on a backside aligned with the at least one

feature on the topside and at least one opening between the at least one feature on the topside and the at least one feature on the backside, forming a dielectric material over the substrate to fill the at least one opening, the dielectric material having at least one seam formed therein, and exploiting the at least one seam to form at least one nanopore.

[0008] In another aspect, a method for forming a nanopore is provided. The method generally includes forming an etch pit on a topside of a substrate, forming a trench on a backside of the substrate, the trench being aligned with the etch pit, forming an opening between the etch pit and the trench, the opening connecting the etch pit and the trench, forming a dielectric material over the substrate to fill the opening, the dielectric material having a seam formed therein, and exploiting the seam to form a nanopore.

[0009] In yet another aspect, a substrate is disclosed. The substrate generally includes a plurality of topside features on a topside of the substrate, a plurality of backside features on a backside of the substrate, each of the plurality of features on the topside being aligned to each of the plurality of features on the backside, a plurality of openings connecting each of the plurality of topside features to each of the plurality of backside features, and a dielectric material formed over the substrate, the dielectric material in each of the topside features having a nanopore at or near a center of each of the plurality of openings.

[0010] In yet another aspect, a method for forming a nanopore is provided. The method generally includes forming a trench on a backside of the substrate, forming an etch pit on a topside of the substrate, the etch pit being formed over an etch-stop layer, the etch-stop layer forming a barrier between the trench and the etch pit, forming a dielectric material from the barrier, disposing one or more contacts on the topside and the backside of the substrate, and applying a voltage from the topside contact to the backside contact, or vice versa, through the dielectric material to form a nanopore.

[0011] In yet another aspect, a method for forming a nanopore is provided. The method generally includes providing a substrate having at least one feature on a topside and at least one feature on a backside aligned with the at least one feature on the topside and at least one opening between the at least one feature on the topside and the at least one feature on the backside, forming a dielectric material over the substrate to fill the at least one opening, and applying a voltage from the topside to the backside through the dielectric material to form at least one nanopore.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to aspects, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary aspects and are therefore not to be considered limiting of its scope, and may admit to other equally effective aspects.

[0013] Figure 1 is a process flow of a method for forming one or more nanopores according to the present disclosure.

[0014] Figures 2A-2O depict cross-sectional views of a substrate in which one or more nanopores are formed at various stages of a process flow disclosed herein.

[0015] Figures 3A-3C depict cross-sectional views of a substrate in which one or more nanopores are formed at various stages of another process flow disclosed herein.

[0016] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the

figures. It is contemplated that elements and features of one aspect may be beneficially incorporated in other aspects without further recitation.

DETAILED DESCRIPTION

[0017] Methods are provided for manufacturing well-controlled, solid-state nanopores and arrays of well-controlled, solid-state nanopores. In one aspect, methods for manufacturing nanopores and arrays of nanopores exploit a physical seam. One or more etch pits are formed in a topside of a substrate and one or more trenches, which align with the one or more etch pits, are formed in a backside of the substrate. An opening is formed between the one or more etch pits and the one or more trenches. A dielectric material is then formed over the substrate, for example, by oxidation or atomic layer deposition, to fill the opening. Contacts are then formed or placed on the topside and the backside of the substrate and a voltage is applied from the topside to the backside of the substrate, or vice versa, through the dielectric material to form a nanopore. In another aspect, the nanopore is formed at or near the center of the opening at a seam, which is formed in the dielectric material.

[0018] Methods disclosed herein refer to formation of solid-state nanopores on a semiconductor substrate as an example. It is also contemplated that the disclosed methods are useful to form other pore-like structures on various materials, including solid-state and biological materials. Methods disclosed herein also refer to formation of frustum-shaped etch pits and trenches as an example; however, other etched features and any combinations thereof are also contemplated. For illustrative purposes, a silicon on insulator (SOI) substrate with a silicon oxide dielectric layer is described; however, any suitable substrate materials and dielectric materials are also contemplated. Additionally, methods disclosed herein refer to a topside and a backside of the substrate. The topside and backside generally refer to opposite sides of the substrate and do not necessarily require an upward or downward orientation. As such, it is

contemplated that methods described herein are also useful for forming a nanopore through a vertical membrane by exploiting a seam thereon. Additionally, while the methods disclosed herein generally refer to exploiting a seam, it is also contemplated that the disclosed methods are useful for exploiting a gap to form a nanopore.

[0019] Figure 1 is a process flow of a method 100 for forming one or more nanopores according to the present disclosure.

[0020] Prior to method 100, a substrate is provided. The substrate is generally any suitable semiconductor substrate, such as a doped or undoped silicon (Si) substrate. The method 100 begins at operation 110 by forming one or more etch pits in a topside of a substrate. At operation 120, one or more trenches are formed in a backside of the substrate, which align with the one or more etch pits in the topside of the substrate. At operation 130, an opening is formed between each of the one or more etch pits and the one or more trenches. At operation 140, a dielectric material is formed over the substrate to fill the opening and form a seam at or near the center of the opening. The seam is generally formed at the intersection of the dielectric material formed on each of the sidewalls. At operation 150, the seam is exploited to form a nanopore by applying a voltage from the topside to the backside of the substrate, or vice versa, to open the seam and form the well-controlled nanopore.

[0021] In one aspect, operation 140 and operation 150 are part of stand-alone processes that are performed on an already-processed substrate having an opening therein.

[0022] Operation 120, operation 130, and operation 140 are generally performed in any suitable order. In one aspect, forming one or more trenches in the backside of the substrate at operation 120 occurs prior to forming one or more etch pits in the topside of the substrate at operation 110, and depositing the

dielectric material at operation 140 is generally performed at any suitable stage of the method 100.

[0023] In one aspect, the substrate is oxidized to fill the opening and a seam is formed at or near the center of the opening in each of the one or more etch pits. In another aspect, a dielectric material is deposited over the substrate and a seam is formed at or near the center of the opening in each of the one or more etch pits. The dielectric material is generally deposited by any suitable deposition methods, including but not limited to, atomic layer deposition (ALD), physical vapor deposition (PVD), or chemical vapor deposition (CVD). Additionally, while some examples include formation of a seam in the deposited dielectric material, it is also contemplated that the dielectric material does not have a seam and that applying a voltage across the dielectric material at voltage sufficient to cause dielectric breakdown will form a nanopore within the dielectric material.

[0024] In another aspect, the method 100 further includes forming an etch stop layer at the bottom of the one or more etch pits in the topside of the substrate, for example, before oxidizing the substrate or depositing the dielectric material.

[0025] Figures 2A-2O depict cross-sectional views of a substrate 200 in which one or more nanopores are formed according to a method disclosed herein, such as at various stages of the method 100. While Figures 2A-2O are shown in a particular sequence, it is also contemplated that the various stages of method 100 depicted in Figures 2A-2O are performed in any suitable order.

[0026] As shown in Figure 2A, a topside hard mask 210 is disposed over a topside of the substrate 200, a topside bottom anti-reflective coating (BARC) layer 212 is disposed over the topside hard mask 210, and a topside photoresist 214 is disposed over the topside BARC layer 212. A topside patterning process

is then performed to form one or more trenches 216 in the topside hard mask 210 and the topside BARC layer 212. Generally, the topside patterning process includes patterning the topside photoresist 214, as shown in Figure 2B, and then etching, for example by reactive ion etching (RIE), the unmasked topside hard mask 210 and topside BARC layer 212, as shown in Figure 2C. The topside photoresist 214 is optionally removed. A topside etch process, such as a KOH etch or other suitable etch process, is then performed to form one or more frustum-shaped etch pits 218 in the substrate 200, as shown in Figure 2D. Other suitable etch processes include, but are not limited to, anisotropic etch processes.

[0027] The substrate 200 is then flipped for backside processing. As shown in Figure 2E, a backside hard mask 220 is deposited over a backside of the substrate 200, a backside BARC layer 222 is deposited over the backside hard mask 220, and a backside photoresist 224 is deposited over the backside BARC layer 222. A backside patterning process is then performed to form one or more backside trenches 226 in the backside hard mask 220 and the backside BARC layer 222. Generally, the backside patterning process includes patterning the backside photoresist 224, as shown in Figure 2F, and then etching the unmasked backside hard mask 220, backside BARC layer 222, and a portion of the substrate 200 to form the one or backside trenches 226, as shown in Figure 2G. The spin coated backside photoresist 224 is optionally removed.

[0028] In the aspect of Figures 2A-2O, the substrate 200 is an SOI substrate having a buried oxide layer 202 therein with a 150 nanometer (nm) Si device layer 230 on the topside thereof as an example; however, any suitable substrate or SOI substrate is also contemplated. The topside hard mask 210 is a low-pressure chemical vapor deposition (LPCVD) nitride, and the topside photoresist 214 is a spin coated photoresist. The one or more frustum-shaped etch pits 218 are generally any suitable size based on the size of the substrate. For example,

in an aspect in which an SOI substrate having 150 nm Si device layer on a topside thereof is used, the one or more frustum-shaped etch pits 218 are 212 nanometer (nm) by 212 nm square openings spaced at 5 millimeter (mm) pitch. A KOH etch generally etches Si at an angle of about 54.7 degrees. Accordingly, when the topside KOH etch is performed on the SOI substrate 200 for a predetermined period of time, the one or more frustum-shaped etch pits 218 generally terminate with a tip of the frustum-shaped etch pit 218 on and in contact with the buried oxide layer 202. The predetermined period of time is generally determined to reduce or eliminate lateral etch relative to the mask opening. In general, the <100> plane 229 of the Si, shown in Figure 2I, will etch at a rate that corresponds to the temperature of the solution and the concentration of KOH in H₂O. For most scenarios, KOH will etch the <100> plane of Si at a rate of between about 0.4nm/s and about 20nm/s. The rate can be accelerated or retarded by cooling or heating the solution.

[0029] Patterning the backside photoresist 224 includes forming a pattern of openings of any suitable size and shape, which are aligned with the one or more frustum-shaped etch pits 218. For example, in an aspect in which an SOI substrate having 150 nm Si device layer on a topside thereof is used, as discussed above, the backside photoresist 224 is patterned with 100 micrometer (μm) by 100 μm square openings at 5 mm pitch, which are aligned with the one or more frustum-shaped etch pits 218 on the topside of the substrate 200. In one aspect, a deep reactive ion etch (DRIE) is then used to form the one or more backside trenches 226. The one or more backside trenches 226 are etched down to the backside surface of the buried oxide layer 202 such that the bottom of each of the one or more backside trenches 226 corresponds to the top of the buried oxide layer 202, as shown in Figure 2G. A local removal process, such as a hydrofluoric acid (HF) dip, is then used to remove the buried oxide layer 202 in the one or more backside trenches 226 such that a bottom of each of the one or more backside trenches 226 is on and in contact with the device layer 230 and

an opening 228 is formed at the tip of the one or more frustum-shaped etch pits 218, as shown in Figure 2I, which is an enlarged and inverted portion of Figure 2H. In further aspects, wet etch processes are used to form the one or more backside trenches 226.

[0030] Generally, the size of the opening 228 is controlled by controlling the chemistry, temperature, concentration gradients, and byproduct removal gradients during the etch processes. In one aspect, the opening is between about 5 nm by 5 nm and about 10 nm by 10 nm. The size of the opening is generally measured using a scanning electron microscope (SEM) or a transmission electron microscope (TEM).

[0031] A dielectric material 232 is then formed over the substrate 200 to fill the opening 228, as shown in Figure 2J. The thickness of the dielectric material 232 is generally between about 0.5 nm to about 10 nm, for example between about 1 nm and about 5 nm, such as about 1 nm. In one aspect, the silicon device layer of the SOI substrate 200 is oxidized, for example by exposing the substrate to oxygen or water (H₂O) to form the dielectric material 232. In another aspect, the dielectric material 232 is deposited by ALD. In another aspect, the dielectric material 232 is formed by depositing a metal or semiconductor layer, for example, by ALD, CVD, or PVD, and then oxidizing the metal or semiconductor layer to form a dielectric material. As shown in Figure 2K, which is an enlarged portion of Figure 2J, a seam 234 is formed in the dielectric material 232 at or near the center of the opening 228, where the dielectric material 232 formed on the sidewalls 236a, 236b of the frustum-shaped etch pits 218 comes together. When oxidation of the silicon device layer is used, for example, the opening 228 is closed by the volume expansion when the silicon (Si) is converted to silicon dioxide (SiO₂). The seam 234 is a weak point in the dielectric material 232.

[0032] The seam 234 is then exploited to form a well-controlled nanopore 236. Generally, exploiting the seam 234 includes applying a voltage from a top

contact over the dielectric material 232 on a topside of the substrate 200 to a bottom contact over the dielectric material 232 on the backside of the substrate 200, or vice versa, through the seam 234. The applied voltage induces dielectric breakdown of the oxide at the seam 234, forming a well-controlled, localized and robust nanopore at the location of the seam 234, which is generally at or near the center of the opening 228. The applied voltage generally removes at least a portion of the dielectric material 232 to form the nanopore, for example, by degrading a portion of the dielectric material 232. The applied voltage generally includes typical voltages above the breakdown voltage of the dielectric material. For example, the breakdown voltage of SiO_2 is generally between about 2 megavolts (MV)/cm and about 6 MV/cm, or between about 200-600 millivolts (mV)/nm of material. In one aspect, the applied voltage is slightly below the breakdown voltage of the dielectric material and the current is applied for longer to slowly break down the membrane. In another aspect, the applied voltage is above the breakdown voltage of the dielectric material such that a nanopore is blasted therethrough.

[0033] In one aspect, the top contact 248 is disposed in a first electrolyte on the topside of the substrate 200 and the bottom contact 250 is disposed in a second electrolyte on the backside of the substrate 200, as shown in Figure 2L. In one example, the top contact 252 and/or the bottom contact 254 is a conductive tungsten (W) layer, as shown in Figure 2M. In further aspects, the top and bottom contacts are any suitable conductive material, such one or more metals or combinations thereof.

[0034] Once the voltage has been conducted through the seam 234, a nanopore 240 is formed at or near the center of the opening 228, as shown in Figure 2N. Because the nanopore 240 has been formed according to methods disclosed herein, the size and position of the nanopore 240 are well controlled. A well-controlled size of the nanopore 240 is generally a diameter suitable for

sequencing a sample of a certain size. In one aspect, the size of the nanopore 240 is about 100 nm or less. In one aspect, the size of the nanopore 240 is between about 0.5 nm and about 5 nm, for example between about 1 nm and about 3 nm, such as 2 nm. In another aspect, the size of the nanopore 240 is between about 1.5 nm and about 1.8 nm, such as about 1.6 nm, which is roughly the size of a single strand of DNA. In another aspect, the size of the nanopore 240 is between about 2 nm and about 3 nm, such as about 2.8 nm, which is roughly the size of double-stranded DNA. A well-controlled position of the nanopore 240 is generally any position on the substrate which is suitable for configuration of one or more nanopores. In one aspect, the substrate 200 includes an array of nanopores 240, as shown in Figure 2O. Methods disclosed herein are generally used to control the position of each of the one or more nanopores 240 such that a nanopore array of desired configuration for sequencing or other processes is formed.

[0035] In one aspect using a tungsten layer, the tungsten is generally patterned to be addressable to each nanopore such that an array of nanopores for sequencing is formed. In another aspect, the voltage is applied sequentially to each feature to form an array of nanopores for sequencing.

[0036] As disclosed above, the stages depicted in Figures 2A-2O are generally performed in any suitable order. In one aspect, the one or more etch pits 218 are formed and then a thin layer of dielectric material 232 is conformally deposited over the one or more etch pits 218. Then, the one or more backside trenches 226 are formed and the buried oxide layer 202 is preferentially removed such that a free-standing dielectric layer remains. A voltage is then applied across the dielectric material 232 to form one or more nanopores 240, as disclosed above.

[0037] In this aspect, a thickness of the conformal dielectric material 232 is between about 0.5 nm and about 10 nm, for example between about 0.5 nm and

about 5 nm, for example between about 1 nm and about 2 nm, such as about 1 nm. The dielectric material 232 is generally any suitable dielectric material with an etch rate that is low relative to SiO₂. Examples of suitable dielectric materials include, but are not limited to, Al₂O₃, Y₂O₃, TiO₂, and SiN. The etch rate of the dielectric material 232 compared to the etch rate of SiO₂ is generally greater than about 10:1, for example about 100:1, for example about 1,000:1, for example about 10,000:1. A seam may or may not be formed at the center of the opening 228 at the bottom of the etch pit 218. However, voltage may still be applied across the dielectric material 232 such that a nanopore 240 is formed at a weak point in the dielectric material 232.

[0038] Figures 3A-3C depict cross-sectional views of a substrate 300 in which one or more nanopores are formed according to a process flow disclosed herein, such as at various stages of the method 100. The stages depicted in Figures 3A-3B are alternative stages of nanopore formation in the substrate, which may be substituted into the various stages depicted in Figures 2A-2O and disclosed above.

[0039] In the aspect depicted in Figures 3A-3C, an etch-stop layer 350 is disposed at the bottom of the one or more etch pits 218, as shown in Figure 3A. The etch-stop layer 350 causes the KOH etch to stop at the bottom of the etch pit 218 at a well-controlled thickness. An opening 228 still exists at the bottom of the etch pit 218 at the thin, exposed etch-stop layer 350. The substrate 300 is then oxidized to form a well-controlled oxide layer, such as a layer of dielectric material 232, for example by rapid thermal processing (RTP) oxidation, to close the opening 228, as shown in Figure 3B. A voltage is then applied across the dielectric material 232, causing dielectric breakdown within the area of the opening 228 at the base of the etch pit 218 such that a nanopore 240 is formed within the opening 228, as shown in Figure 3C. According to this aspect, a seam may or may not be formed in the dielectric material 232; however, dielectric

breakdown at a weak point in the dielectric material 232 at the base of the etch pit 218 will still form the nanopore 240.

[0040] The etch-stop layer 350 is deposited by any suitable method at any suitable stage of the process flows disclosed herein. In one aspect, the etch-stop layer 350 is formed by implanting or diffusing dopants into the silicon device layer and in contact with the buried oxide layer 202 of the SOI substrate during SOI substrate manufacturing. In another aspect, the etch-stop layer 350 is formed after the one or more backside trenches 226 are formed in the backside of the substrate 300 and prior to the formation of the one or more etch pits 218 in the substrate 300. The thickness of the etch-stop layer is any suitable thickness, such as, less than or equal to 10 nm, for example less than or equal to 2 nm, for example less than or equal to 1 nm. The etch-stop layer 350 generally includes any suitable dopant, including but not limited to, boron (B).

[0041] The thickness of the oxidation is any suitable thickness, such as between about 0.5 nm and about 10 nm, for example between about 1 nm and about 5 nm, for example about 1 nm.

[0042] Benefits of the present disclosure include the ability to quickly form well-controlled nanopores and nanopore arrays, which are generally individually addressable. Disclosed methods generally provide nanopores that are well-controlled in size and in position through a thin film membrane. Methods of manufacturing nanopores of well-controlled size provide improved signal-to-noise ratios because the size of the nanopore is similar to the size of the sample, such as a single strand of DNA, being transmitted through the nanopore, which increases the change in electric current passing through the nanopore. Additionally, methods of manufacturing nanopores having well-controlled positions enables a sample, such as DNA, to freely pass through the nanopore. Additionally, the thinness of the membrane, for example, about 1 nm, provides for improved reading of the DNA sequence.

[0043] While the foregoing is directed to aspects of the present disclosure, other and further aspects of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method for forming a nanopore comprising:
 - providing a substrate having at least one feature on a topside and at least one feature on a backside aligned with the at least one feature on the topside, and at least one opening between the at least one feature on the topside and the at least one feature on the backside;
 - forming a dielectric material over the substrate to fill the at least one opening, the dielectric material having at least one seam or gap formed therein; and
 - exploiting the at least one seam or gap to form at least one nanopore.
2. The method of claim 1, wherein forming the dielectric material over the substrate to fill the at least one opening comprises:
 - oxidizing the substrate.
3. The method of claim 1, wherein forming the dielectric material over the substrate to fill the at least one opening comprises:
 - depositing the dielectric material over the substrate by atomic layer deposition, physical vapor deposition, or chemical vapor deposition.
4. The method of claim 1, wherein exploiting the at least one seam or gap to form at least one nanopore comprises:
 - disposing a top contact over the topside of the substrate;
 - disposing a bottom contact over the backside of the substrate; and
 - applying a voltage from the top contact to the bottom contact across the at least one seam or gap.
5. The method of claim 4, wherein a first electrolyte is disposed over the topside of the substrate and a second electrolyte is disposed over the backside of the substrate, and wherein the top contact is disposed in the first electrolyte and the bottom contact is disposed in the second electrolyte.

6. The method of claim 1, wherein the nanopore is formed at or near a center of the at least one opening.
7. A method for forming a nanopore comprising:
 - forming an etch pit on a topside of a substrate;
 - forming a trench on a backside of the substrate, the trench being aligned with the etch pit;
 - forming an opening between the etch pit and the trench, the opening connecting the etch pit and the trench;
 - forming a dielectric material over the substrate to fill the opening, the dielectric material having a seam or gap formed therein; and
 - exploiting the seam or gap to form a nanopore.
8. The method of claim 7, wherein forming a dielectric material over the substrate to fill the opening comprises:
 - oxidizing the substrate.
9. The method of claim 7, wherein forming the dielectric material over the substrate to fill the opening comprises:
 - depositing the dielectric material over the substrate by atomic layer deposition, physical vapor deposition, or chemical vapor deposition.
10. The method of claim 7, wherein exploiting the seam or gap to form the nanopore comprises:
 - disposing a top contact over the topside of the substrate;
 - disposing a bottom contact over the backside of the substrate; and
 - applying a voltage from the top contact to the bottom contact across the seam or gap.
11. The method of claim 10, wherein a first electrolyte is disposed over the topside of the substrate and a second electrolyte is disposed over the backside of the substrate, and wherein the top contact is disposed in the first electrolyte and the bottom contact is disposed in the second electrolyte.

12. The method of claim 7, wherein the seam or gap is formed between a first portion of the formed dielectric material and a second portion of the formed dielectric material.

13. A substrate comprising:
a plurality of topside features on a topside of the substrate;
a plurality of backside features on a backside of the substrate, each of the plurality of topside features being aligned to each of the plurality of backside features;
a plurality of openings connecting each of the plurality of topside features to each of the plurality of backside features; and
a dielectric material formed over the substrate, the dielectric material in each of the topside features having a nanopore at or near a center of each of the plurality of openings.

14. The substrate of claim 13, wherein a diameter of the nanopore is less than or equal to 100 nanometers.

15. The substrate of claim 13, wherein the plurality of topside features are frustum-shaped etch pits, and wherein the plurality of backside features are trenches or frustum-shaped etch pits.

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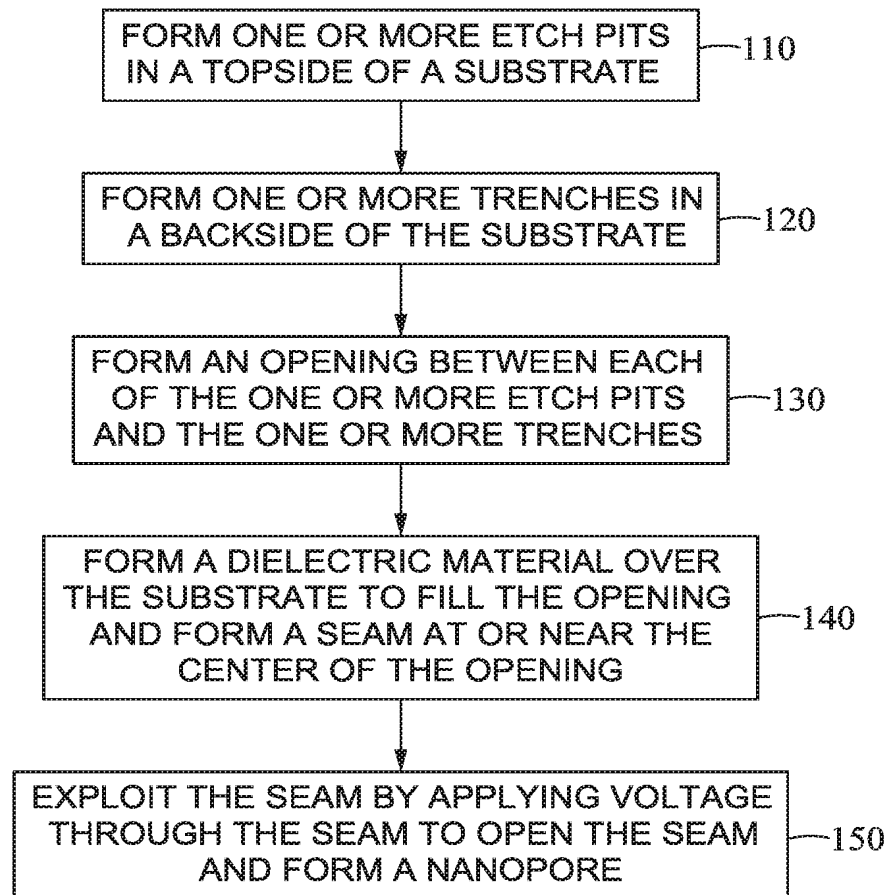


Fig. 1

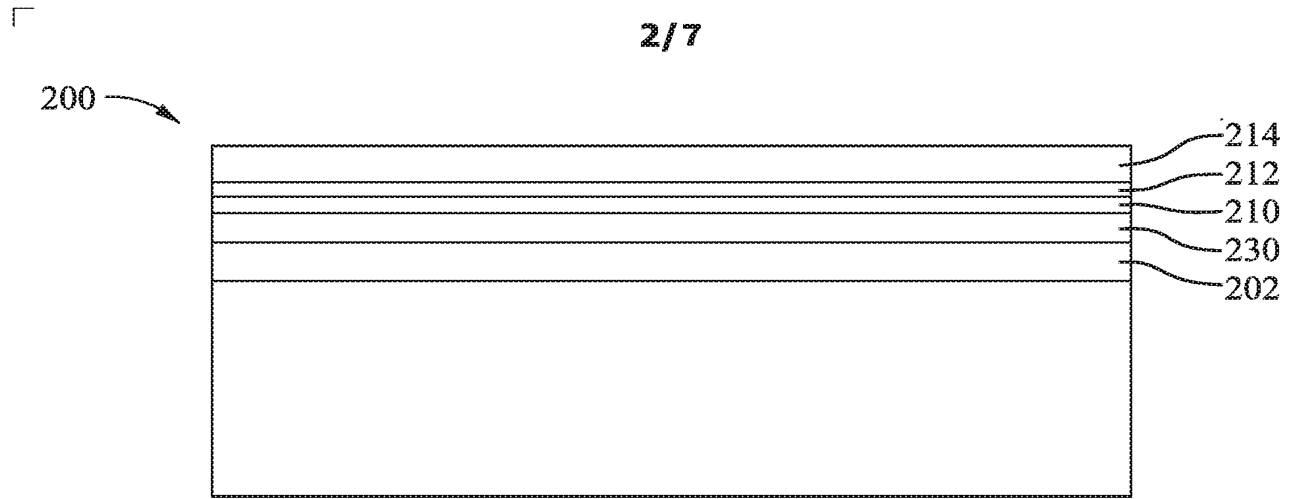


Fig. 2A

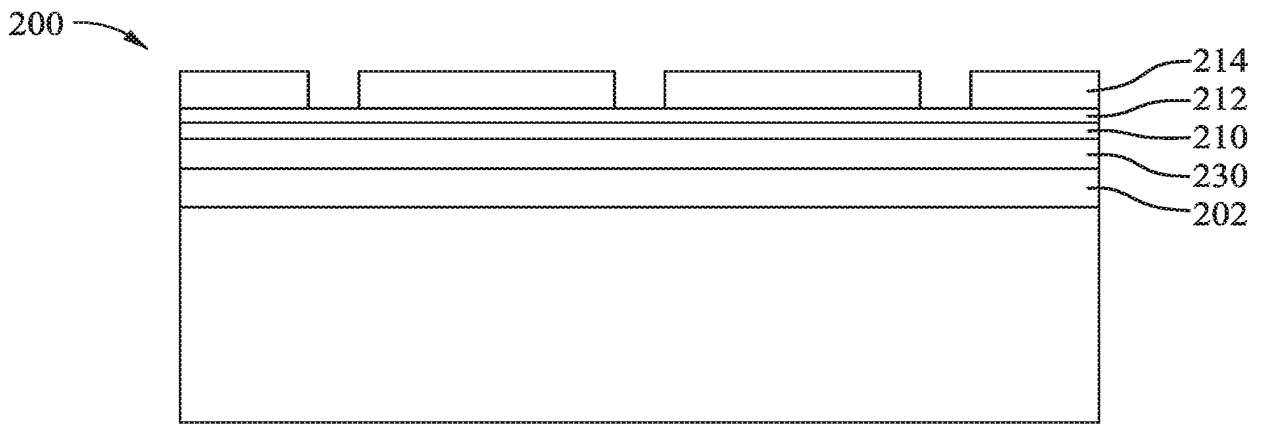


Fig. 2B

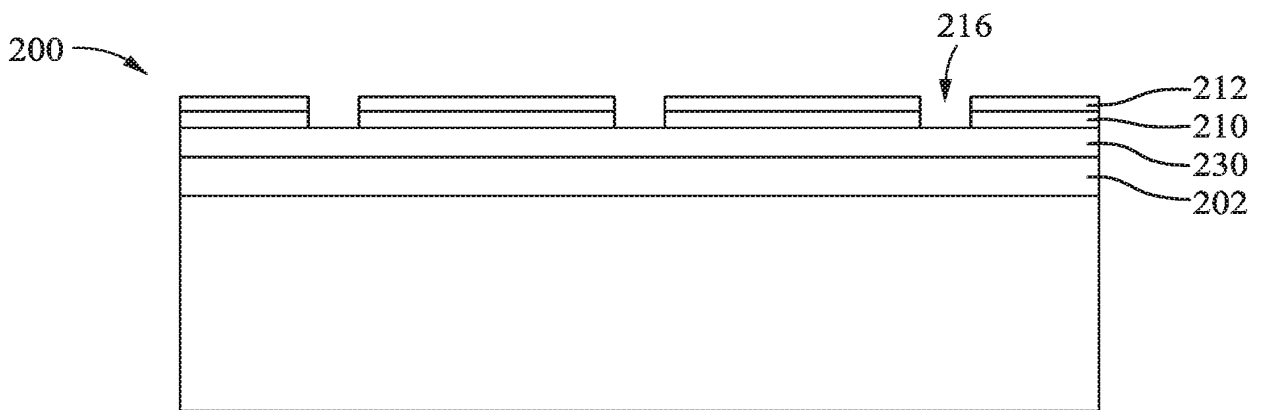


Fig. 2C

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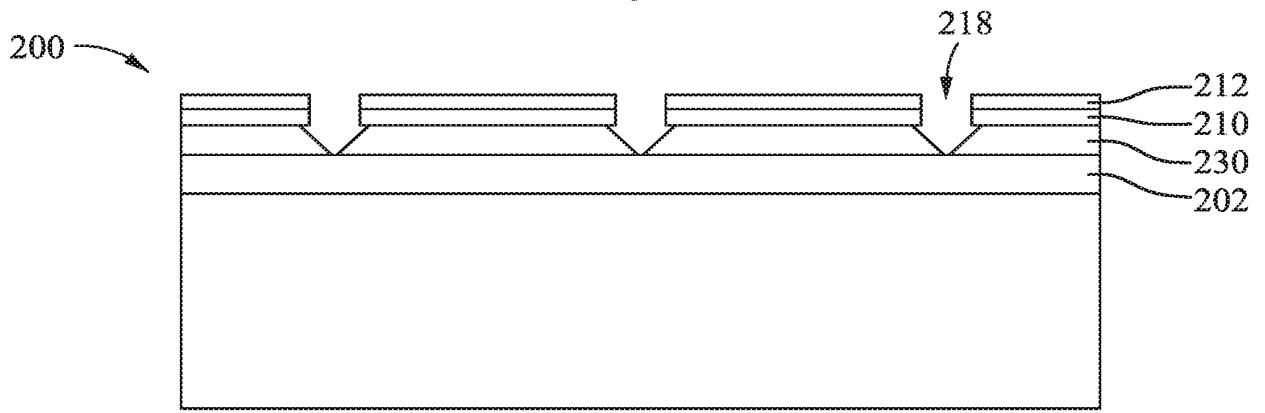


Fig. 2D

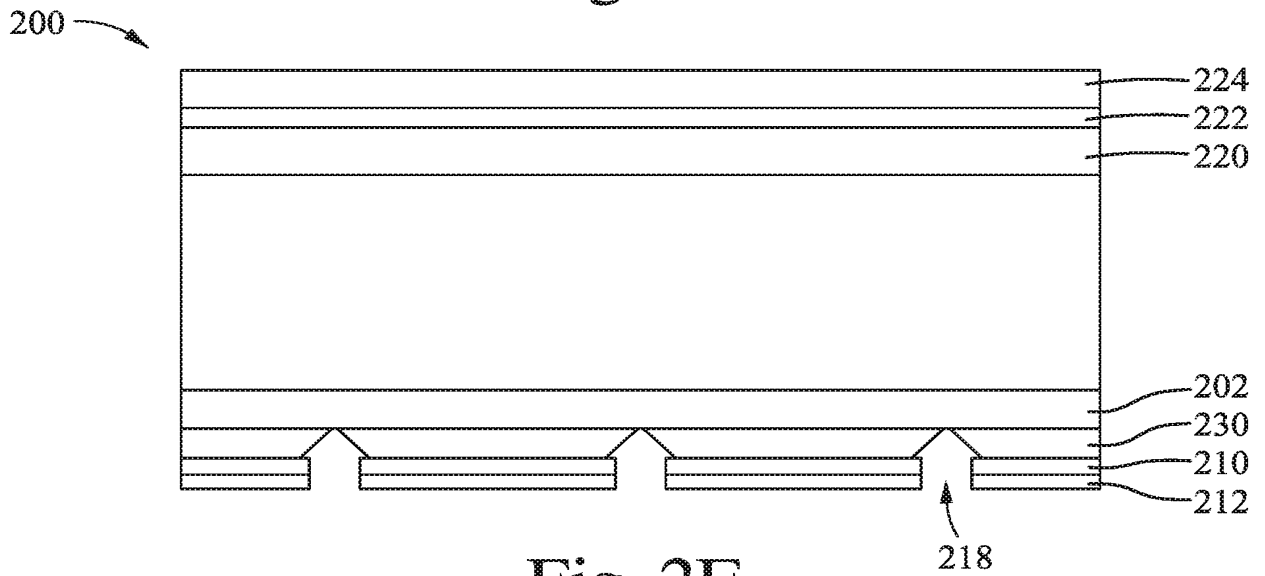


Fig. 2E

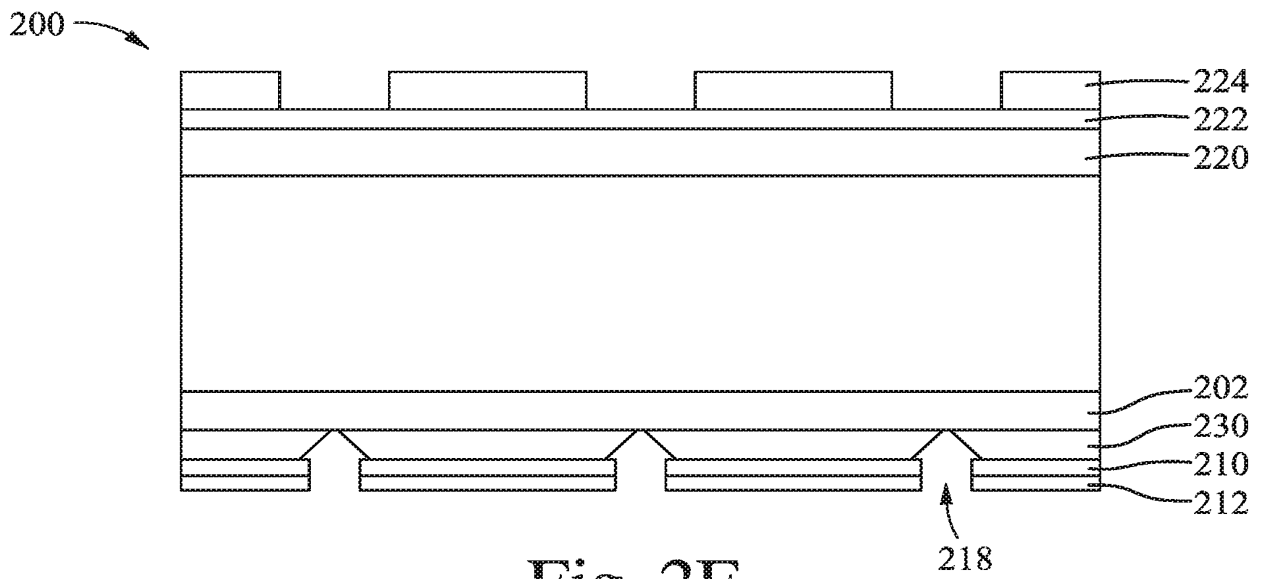


Fig. 2F

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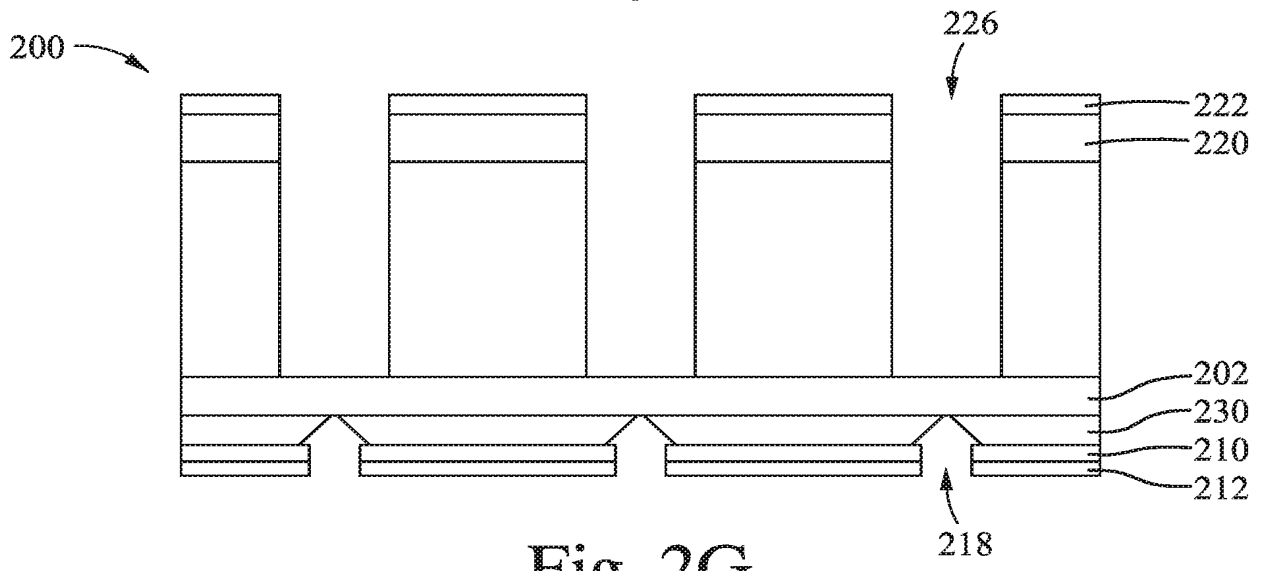


Fig. 2G

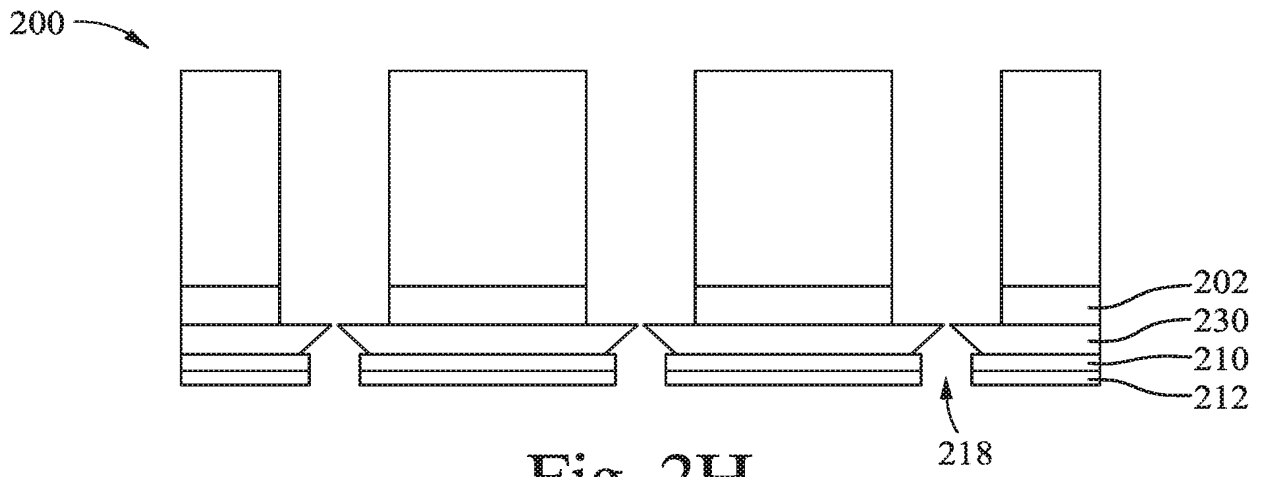


Fig. 2H

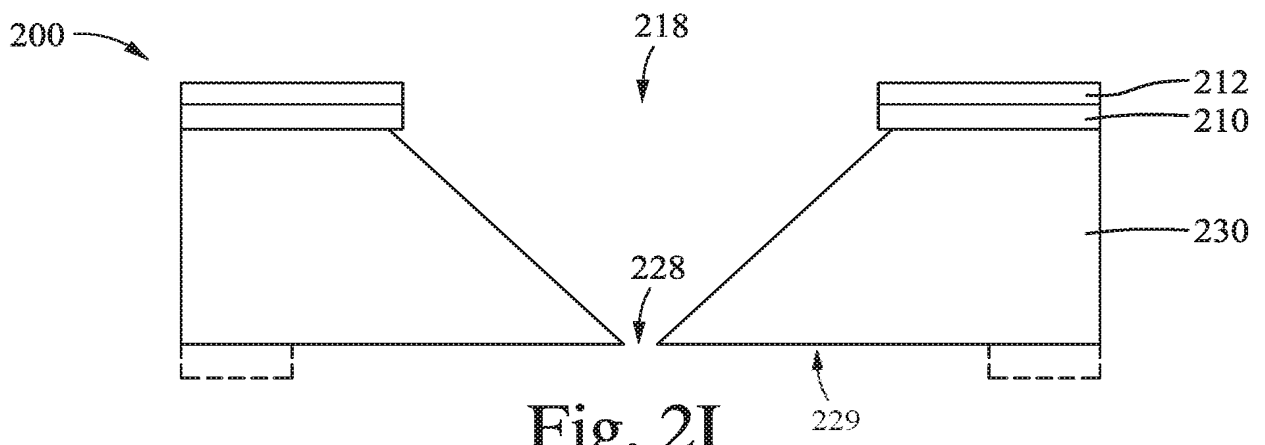


Fig. 2I

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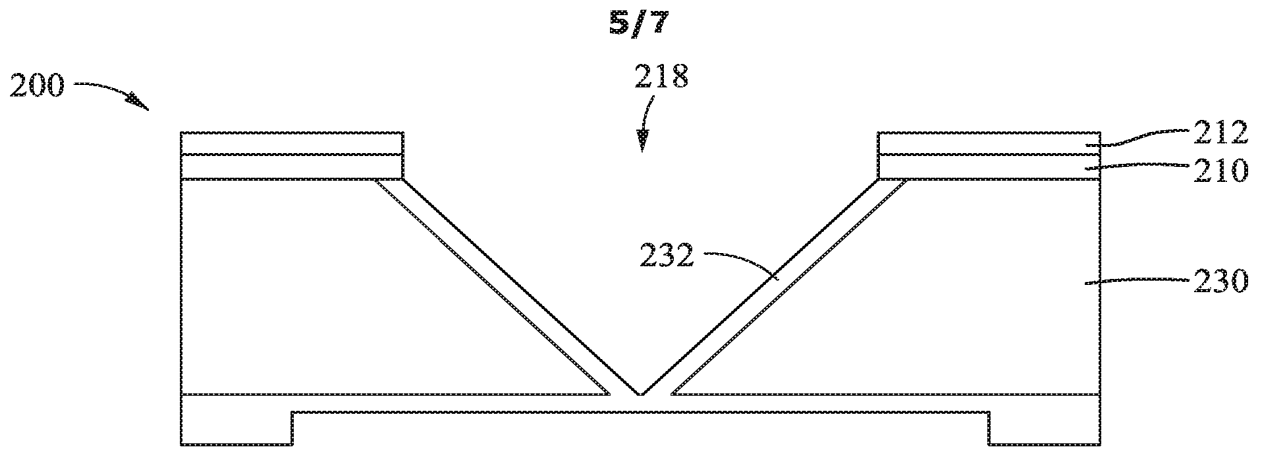


Fig. 2J

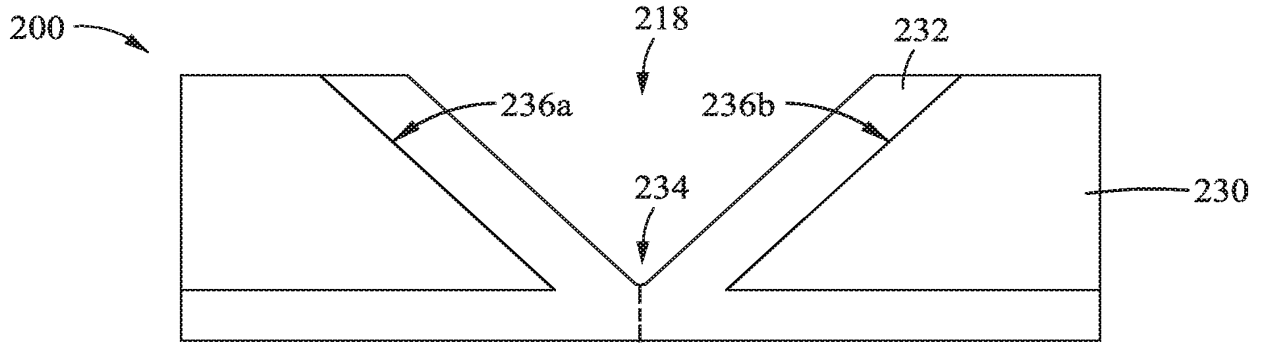


Fig. 2K

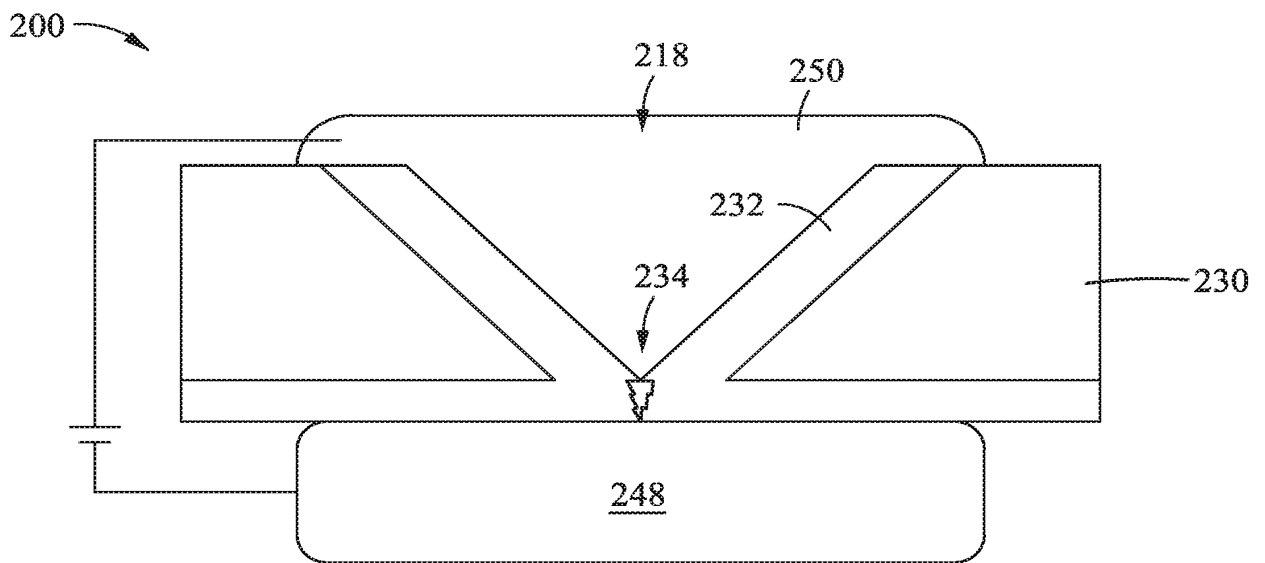


Fig. 2L

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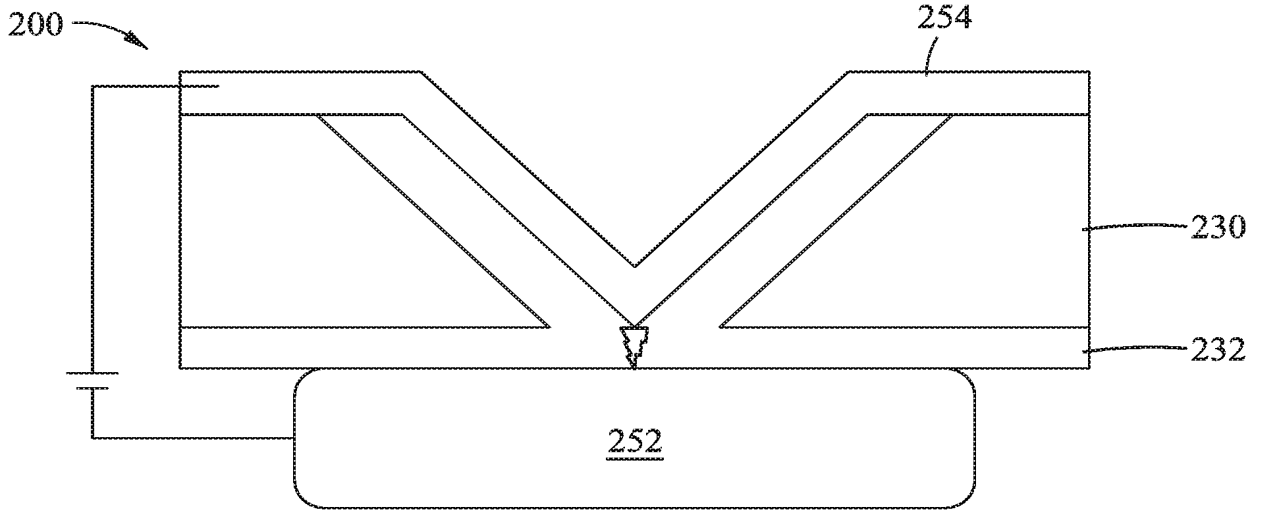


Fig. 2M

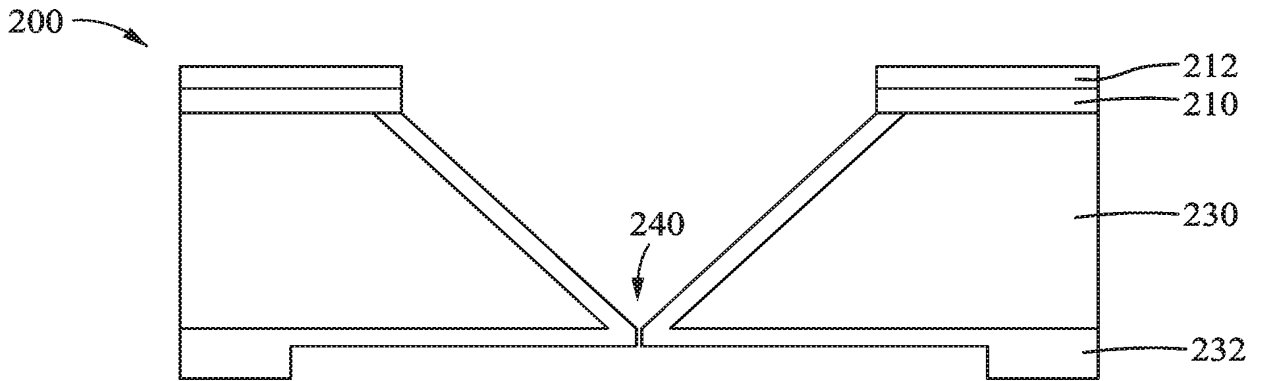


Fig. 2N

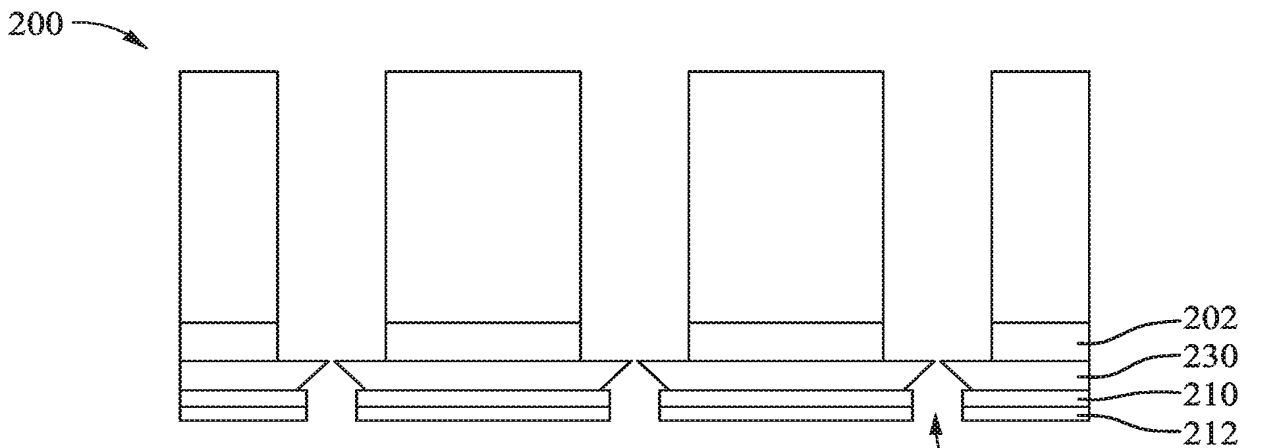


Fig. 2O

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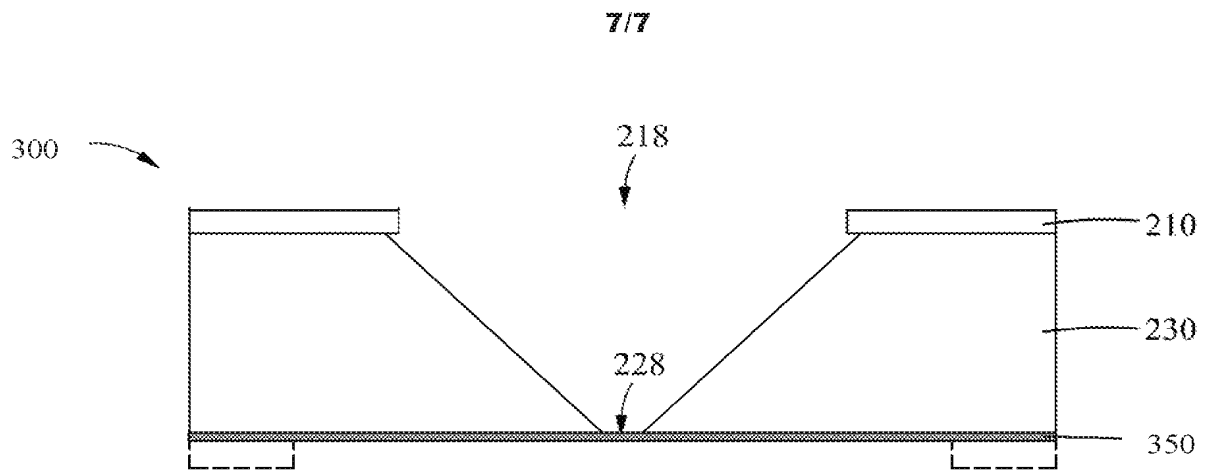


Fig. 3A

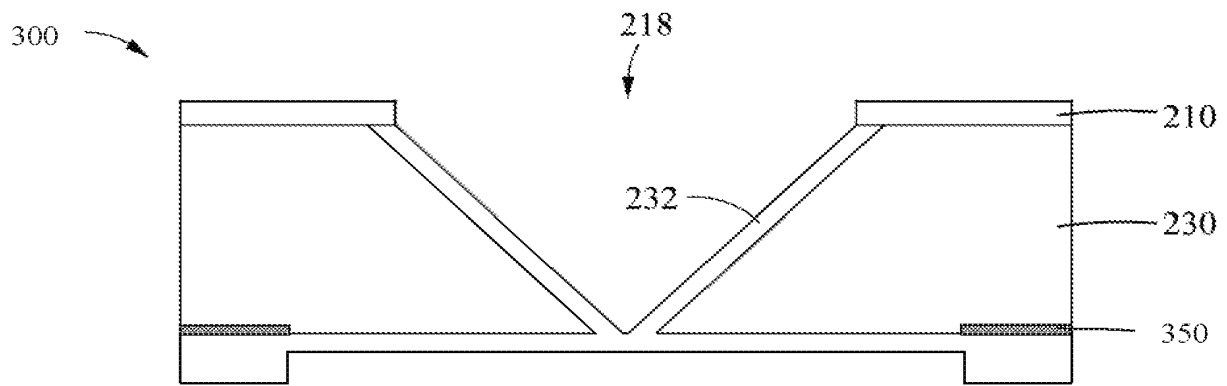


Fig. 3B

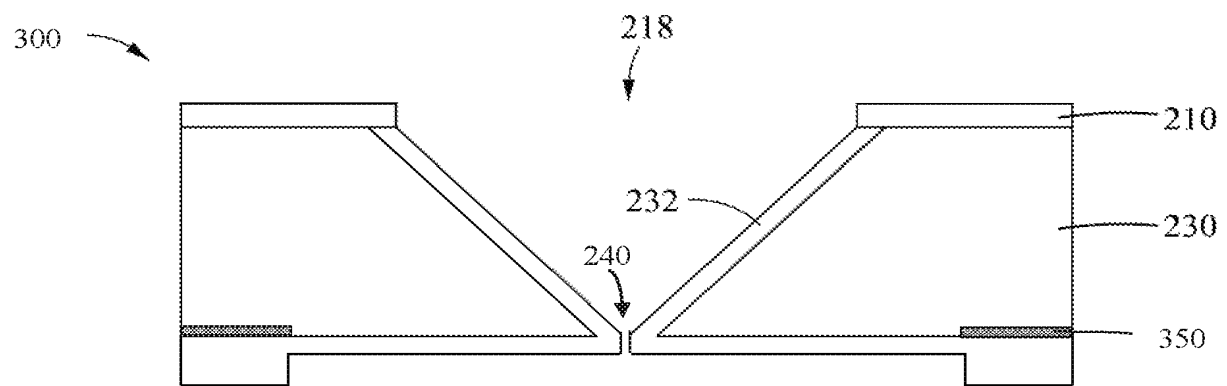


Fig. 3C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/045758**A. CLASSIFICATION OF SUBJECT MATTER**
B81B 1/00(2006.01)i, B81C 1/00(2006.01)i, B82Y 5/00(2011.01)n

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

B81B 1/00; B81C 1/00; G01N 27/407; G01N 27/414; G01N 33/487; G01N 33/50; H01L 29/66; H01M 8/1039; B82Y 5/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: nanopore, substrate, topside, backside, aligned, opening, dielectric material, seam, gap

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 1526109 A2 (AGILENT TECHNOLOGIES INC.) 27 April 2005 See paragraphs [0003]-[0051]; claims 1, 27; and figures 1, 3, 4G.	1-15
Y	US 2017-0263966 A1 (THE UNIVERSITY OF MANCHESTER) 14 September 2017 See paragraphs [0041], [0127]; and figure 4.	1-15
Y	US 2016-0313278 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 27 October 2016 See paragraphs [0033]-[0058]; and figures 4C, 4L.	7-12
A	US 2014-0045270 A1 (SAMSUNG ELECTRONICS CO., LTD.) 13 February 2014 See paragraph [0070]; and figure 1.	1-15
A	US 2015-0069329 A1 (SAMSUNG ELECTRONICS CO., LTD.) 12 March 2015 See paragraph [0056]; and figure 4L.	1-15

 Further documents are listed in the continuation of Box C. See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

04 December 2018 (04.12.2018)

Date of mailing of the international search report

04 December 2018 (04.12.2018)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/045758

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