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(54) **Title**: FLEXIBLE ARRAYS OF MICRO LIGHT EMITTING DIODES USING A PHOTOELECTROCHEMICAL (PEC) LIFTOFF TECHNIQUE

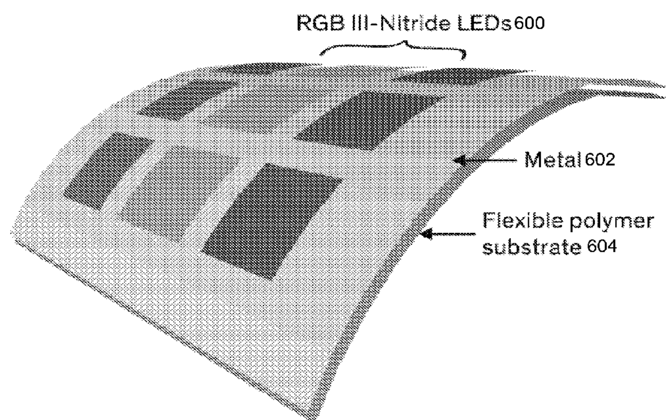

FIG. 6

(57) **Abstract**: Flexible arrays of III-nitride micro light-emitting diodes (LEDs) are fabricated using a photoelectrochemical (PEC) etch as a liftoff technique. A sacrificial layer is grown on a host substrate, wherein the sacrificial layer comprises a III-nitride layer and the host substrate comprises a bulk gallium nitride (GaN) substrate. A III-nitride device structure is then grown on or above the sacrificial layer. A submount is prepared with a polymer film deposited thereon, and the device structure is flip-chip bonded onto the polymer film of the submount. The sacrificial layer is removed using the PEC etch to separate the host substrate from the device structure bonded to the polymer film of the submount. Finally, the polymer film with the device structure is de-laminated from the submount.

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FLEXIBLE ARRAYS OF MICRO LIGHT EMITTING DIODES USING A PHOTOELECTROCHEMICAL (PEC) LIFTOFF TECHNIQUE

CROSS REFERENCE TO RELATED APPLICATIONS

5 This application claims the benefit under 35 U.S.C. Section 119(e) of co-pending and commonly-assigned U.S. Provisional Application Serial No. 62/069,644, filed on October 28, 2014, by David Hwang, Nathan G. Young, Ben Yonkee, Burhan K. Saifaddin, Steven P. DenBaars, James S. Speck, and Shuji Nakamura, entitled "FLEXIBLE ARRAYS OF MICRO-LEDS USING A PHOTOELECTROCHEMICAL 10 (PEC) LIFTOFF TECHNIQUE," attorney's docket number 30794.576-US-P1 (2015-205-1);

which application is incorporated by reference herein.

BACKGROUND OF THE INVENTION

15 1. Field of the Invention.

This invention is related to the fabrication of flexible arrays of III-nitride micro Light Emitting Diodes (LEDs) using a photoelectrochemical (PEC) liftoff technique.

2. Description of the Related Art.

20 (Note: This application references a number of different publications and patents as indicated throughout the specification by one or more reference numbers in brackets, e.g., [x]. A list of these different publications and patents ordered according to these reference numbers can be found below in the section entitled "References." Each of these publications and patents is incorporated by reference herein.)

25 Commercially available III-nitride light-emitting diodes (LEDs) typically have thin films that are epitaxially grown in the c-direction [0001] on sapphire substrates. However, III-nitride thin films grown on sapphire have high threading dislocation (TD)

densities on the order of 10^9 - 10^{10} cm^{-2} [1] (where cm is centimeters), which degrade material quality and inhibit optical performance.

To overcome these problems, efforts have therefore been made to grow on bulk GaN substrates. These bulk substrates include numerous orientations, including the basal c-plane {0001}; nonpolar a-plane {1 1 -2 0} and m-plane {1 0 -1 0} families; and semipolar plane families such as the {1 0 -1 1} and {2 0 -2 1} planes, to name a few. However, such substrates are rigid substrates, which result in rigid devices, and there is an increasing demand for flexible electronic devices.

Thus, there is a need for improved methods of fabricating III-nitride LEDs. The present invention satisfies this need.

SUMMARY OF THE INVENTION

To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a method of fabricating an electronic or optoelectronic device (e.g., flexible arrays of micro-LEDs) using a PEC liftoff technique, by: (a) growing a sacrificial layer on a host substrate (e.g., a bulk GaN substrate), wherein the sacrificial layer comprises a III-nitride layer; (b) growing a III-nitride device structure (e.g., by metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE)) on or above the sacrificial layer; (c) preparing a submount with a polymer film deposited thereon; (d) flip-chip bonding the device structure onto the polymer film of the submount; (e) removing the sacrificial layer to separate the host substrate from the device structure, wherein the sacrificial layer is removed using a photoelectrochemical (PEC) etch technique; and (f) de-laminating the polymer film (with the device structure) from the submount.

The device structure can include an n-type layer-intrinsic layer-n-type layer (n-i-n) structure.

The submount can be silicon, silicon carbide, or sapphire, and the polymer film may be polyimide or polyethylene terephthalate, for example.

The method can comprise patterning the III-nitride device structure into micro devices prior to the flip chip bonding, e.g., such that the devices have a surface area less than 0.1 μm^2. The device structure can have a thickness of 3 micrometers or less.

The submount can be prepared using a process comprising placing the polymer film onto the submount comprising a wafer; curing the polymer film; and depositing metal onto the polymer film, wherein the metal promotes bonding to a p-contact of the device structure.

The bulk GaN substrate can have a polar plane orientation, nonpolar plane orientation, or a semipolar plane orientation, for example. The host substrate can have a threading dislocation (TD) density of less than 10^9 cm^{-2}.

The method can comprise encapsulating the devices to protect the devices.

The PEC etch technique can expose the sacrificial layer to a solution and apply light from a light source causing the sacrificial layer to etch in the solution. The solution can comprise potassium hydroxide (KOH) and water, and the light source can emit light having an approximate wavelength of 400 nanometers.

The sacrificial layer can be comprised of an InGaN/GaN multi quantum well (MQW), and the InGaN composition can be tuned such that its bandgap is smaller than a photon energy of the light.

The polymer film can be de-laminated from the submount using a blade. The delaminating can comprise delaminating the polymer film from the submount comprising a wafer.

One or more embodiments of the present invention further disclose an optoelectronic or electronic device, comprising a flexible polymer substrate; a III-nitride device structure on the flexible polymer substrate, the III-nitride device including an active layer between an n-type layer and a p-type layer, the optoelectronic or electronic

device fabricated using a process comprising: (a) growing a sacrificial layer on a host substrate, wherein the sacrificial layer comprises a III-nitride layer; (b) growing the III-nitride device structure on or above the sacrificial layer, wherein the III-nitride device structure comprises a top surface and a bottom surface, the bottom surface interfacing the
5 sacrificial layer and opposite the top surface; (c) preparing a submount with a polymer film deposited thereon; (d) flip-chip bonding the top surface of the III-nitride device structure onto the polymer film of the submount; (e) removing the sacrificial layer to separate the host substrate from the device structure, wherein the sacrificial layer is removed using a photoelectrochemical (PEC) etch technique; and (f) de-laminating the
10 polymer film from the submount.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

15 FIG. 1 is a flowchart illustrating a method of fabricating a device according to one or more embodiments of the invention.

FIG. 2 is a schematic of an example device structure, according to one or more embodiments of the invention, comprising a c-plane GaN substrate with 3 μm of n-GaN, an InGaN/GaN sacrificial layer absorbing electromagnetic radiation having a wavelength
20 of 415 nanometers (nm), 2.2 micrometers (μm) of n-GaN, an active region including an InGaN/GaN multi-quantum well absorbing electromagnetic radiation having a wavelength of 450 nm, and 150 nm of p-GaN.

FIG. 3 is a schematic of an example of a processed device structure, according to one or more embodiments of the invention, comprising the layers in FIG. 2 and further
25 including a p-type contact (p-contact), a dielectric, and a PEC contact.

FIG. 4 is a schematic illustrating an apparatus for PEC etching the device structure of FIG. 3 attached to a flexible polymer substrate on a submount, according to one or more embodiments of the invention.

FIG. 5 is a schematic of an example of a processed device structure that has been flip-chip bonded to a flexible polymer substrate on a submount, wherein the host substrate has been removed, according to one or more embodiments of the invention.

FIG. 6 is a schematic of a flexible array of micro-LEDs, including the example processed device structure of FIG. 5 comprising a plurality of red-green-blue (RGB) light-emitting III-nitride (or other) LEDs on top of a thin layer of metal on top of the flexible polymer substrate, according to one or more embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the preferred embodiment, reference is made to a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Technical Description

One or more embodiments of the present invention describe a method to fabricate a flexible, bendable and/or stretchable array of III-nitride micro devices, including but not limited to, light-emitting devices (e.g. VCSELs) and detectors, etc., by PEC liftoff.

The method combines the epitaxy of III-nitride thin films for a device structure on a rigid host substrate, the flip-chip bonding of the device structure to a flexible film substrate deposited on a submount, and the use of a photoelectrochemical (PEC) etch technique to lift off the device structure and remove the rigid host substrate. The PEC etch technique is sensitive to dislocations and does not completely etch materials with TD densities greater than 10^9 cm^{-2}. The term “flip-chip bonding” refers to wafer bonding

the device structure and host substrate to a submount, so that the device structure is positioned between the submount and the host substrate.

FIG. 1 illustrates a method involving the growth of III-nitride films on bulk polar, nonpolar, or semipolar GaN substrates (Block 100), patterning the films into micro devices (Block 102), preparing or obtaining a submount with a suitable flexible substrate (Block 104), flip-chip bonding the micro devices to the suitable flexible substrate on the submount (Block 106), PEC etching a sacrificial layer to remove the micro devices from the rigid host substrate (Block 108), encapsulating the devices with a thin transparent film (Block 110), and delaminating the polymer film from the submount, as illustrated in Block 112, resulting in a flexible array of III-nitride devices (e.g., micro-LEDs). Previous attempts have been made to fabricate flexible GaN LEDs, but these attempts did not use a PEC etch technique to remove the substrate and did not use bulk GaN substrates [2-5].

PEC etching of III-nitrides on various substrates, such as silicon carbide [6,18], sapphire [7-12], and silicon [5], has been previously explored. PEC etching is a dopant-selective, bandgap-selective, and defect-selective etch method that can be used to perform top-down etching or undercut etching.

The PEC etch technique requires emission of light comprising photons having an energy that is larger than the bandgap of the material to be etched. The light generates charge carriers (electrons and holes), which are then separated by electric fields within the material.

The PEC etch technique described in one or more embodiments of the invention makes use of an n-i-n structure. Because of the ways the bands bend in the equilibrium diagram, holes are confined to the intrinsic layer. In the GaN material system, holes react with GaN in an oxidizing electrolyte solution, such as potassium hydroxide (KOH), to create gallium oxide (Ga_2O_3). This oxide can then be dissolved in KOH, wherein the dissociation of the oxide achieves the actual etching of GaN.

The technique is dopant-selective because it can etch n-type III-nitride semiconductor materials selectively over p-type [13]. The technique is bandgap-selective because it requires the light emitted from the light source to comprise photons having an energy larger than the bandgap of the material to be etched [14]. The technique is
5 defect-selective because defects act as traps for the holes, which slows or prevents the etching of the material [8,15]. Therefore, this PEC etch technique will only work on materials that are not highly defective; highly defective in this case refers to TD densities of greater than 10^9 cm^{-2}.

An example process flow using the method illustrated in FIG. 1 is further
10 described below.

Growth of sacrificial layer and device structure (e.g., Block 100)

Block 100 represents growing a sacrificial layer on a host substrate (e.g. bulk GaN), wherein the sacrificial layer comprises a III-nitride layer; and growing a III-nitride
15 device structure on or above the sacrificial layer, wherein the III-nitride device structure comprises a top surface and a bottom surface, the bottom surface interfacing the sacrificial layer and opposite the top surface. The host substrate can have a threading dislocation density less than 10^9 cm^{-2}. The III-nitride device structure can include an n-type layer/intrinsic layer/n-type layer (n-i-n) structure (i.e., intrinsic layer between n-type
20 layers).

First, a thick layer of n-type GaN (n-GaN) is grown (1-4 μm thick) on the host substrate. The sacrificial layer is then grown and can be comprised of (e.g., a six-period) InGaN/GaN multi quantum well (MQW), wherein the InGaN composition of the InGaN layer in the sacrificial layer is tuned such that the bandgap of the InGaN layer is smaller
25 than the photon energy of the light emitted from the light source used for the PEC liftoff.

The layers above the sacrificial layer can comprise a micro-LED device structure. On or above the sacrificial layer is another thick layer of n-GaN that completes the n-i-n

structure needed for the PEC etch, although any material with a wider bandgap (e.g. AlGaN) could be used.

After the n-GaN growth, the active region is grown, which can be another 6-period InGaN/GaN MQW that determines the color of light emission. Depending on the desired emission wavelength, the active region can be made of any III-nitride composition.

Finally, a thin layer of p-type III-nitride is grown. The III-nitride device structure including a p-type layer, n-type layer, and active region between the n-type layer and the p-type layer can have a thickness of 3 micrometers or less, for example.

FIG. 2 is a schematic of an example device structure that can be grown, comprising a c-plane GaN substrate 200 (as the host substrate) with a 3 μm thick n-type GaN (n-GaN) layer 202 deposited thereon, a sacrificial layer comprising an InGaN/GaN sacrificial layer (6 period MQW) 204 absorbing violet electromagnetic radiation (e.g., having a wavelength $\lambda = 415$ nm), a 2.2 μm thick n-GaN layer 206, an active region 208 comprised of (e.g., a 6 period) InGaN/GaN multi-quantum well (MQW) absorbing blue electromagnetic radiation at a wavelength $\lambda = 450$ nm, and a 150 nm thick p-type GaN (p-GaN) layer 210. The device structure may be grown by metal organic chemical vapor deposition (MOCVD) or Molecular Beam Epitaxy (MBE), for example.

The choice of host substrate 200 on which to grow is crucial to the PEC etch. Many commercially available III-nitride LEDs use thin films that are grown on sapphire substrates. However, III-nitride thin films grown on sapphire have high TD densities on the order of 10^9 cm^{-2} [1], which degrade the material quality and could inhibit optical performance.

Efforts have therefore been made to grow on bulk GaN substrates, resulting in no mismatch. These bulk substrates include numerous orientations, including the basal c-plane {0001}; nonpolar a- {1 1 -2 0} and m-plane {1 0 -1 0} families; and semipolar

plane families such as {1 0 -1 1} and {2 0 -2 1}, among others. The method described herein applies to all of these orientations.

Patterning of devices (e.g., Block 102)

5 The thin films can then be patterned (e.g., into micro-LED devices), as represented in Block 102 of FIG. 1), and other materials (e.g., metals) are deposited to serve as or form n-type contacts (n-contacts) and p-type contacts (p-contacts). An example of the result of this processing is shown in FIG. 3, which is a schematic of an example processed device structure comprising the layers in FIG. 2 and further including 10 a p-contact 300, a dielectric 302, and a PEC contact 304, a first mesa 306, and a second mesa 308 formed by the patterning.

The p-contact 300 is deposited onto the p-type III-nitride 210, the mesa 306 is formed so that the dielectric 302 (e.g. silicon nitride) protects the active region 208, the second mesa 308 is formed to expose the sacrificial layer 204, and the PEC contact 304 is 15 deposited to serve as the contact to the oxidizing electrolyte. Protection of the active region 208 during the PEC etch is provided by the dielectric layer 302.

After patterning, the devices can have a surface area less than 0.1 μm^2 and/or the device structure has a thickness of 3 micrometers or less.

20 Preparing a submount with polymer film deposited thereon (e.g., Block 104)

A flexible substrate can then attached to the (e.g., micro-LEDs) via the p-contact 300 in a flip-chip bonding process. First, the submount must be prepared [16,17]. A thin film (e.g., ~24 μm thick) of polyimide, or other suitable polymer, such as polyethylene terephthalate, is placed (spin-coated, rolled, etc.) onto a submount comprising a silicon 25 wafer (although other wafers such as SiC or sapphire may be used), and the film is subsequently cured.

Then, a layer (50 nm – 3 μm thick) of material similar to the p-contact (e.g., metal such as gold, copper, etc.) is deposited onto the polymer film, in order to promote bonding to the p-contact 300 of the device structure. The material may be patterned to provide subsequent individual addressability to the bonded devices. The deposition of the polymer and the material similar to the p-contact may also be repeated in order to provide a more adequate network of contacts to the attached devices.

Flip-chip bonding the top surface of the III-nitride device structure onto the polymer film of the submount (e.g., Block 106)

The resulting submount is then flip-chip bonded to the p-contact of the device structure at a temperature between 200°C and 400°C for between 1 - 3 hours. After this step, the sacrificial layer (e.g., 204) is positioned in between the host substrate (e.g., 200) and submount, and is subsequently exposed.

Removing the sacrificial layer to separate the host substrate from the device structure, wherein the sacrificial layer is removed using a photoelectrochemical (PEC) etch technique (e.g., Block 108)

The removal of the host substrate is done via a PEC etch. The PEC etch setup is comprised of a light/electromagnetic radiation source 400 and an electrochemical cell (comprising voltage source 402, cathode 304, and electrode 404) with an oxidizing electrolyte, such as KOH, as illustrated in FIG. 4. Specifically, the sample 406 (comprising the structure of FIG. 3 attached to a submount 408 and polymer film 410) is immersed in a solution of KOH that has a molarity between 0.001 and 1 (wherein the solution is in a container 412). The cathode 304 is a metal deposited on the semiconductor, which is labeled as the PEC contact 304 n FIG. 3, and the anode is the semiconductor surface 414. The solution may be constantly stirred by a magnetic stirrer.

The sacrificial layer 204 is an intrinsic region as described above, so holes are confined to the sacrificial layer 204 and will etch the sacrificial layer 204. The light source 400 emitting light/electromagnetic radiation 416 with an approximate wavelength of 400 nm, corresponding to a photon energy which is larger than the bandgap of the
5 sacrificial layer 204, shines onto the sample 406 until the sacrificial layer 204 is completely etched. Specifically, the PEC etch technique exposes the sacrificial layer to the solution (e.g., comprising KOH and water) and applies light from a light source causing the sacrificial layer to etch in the solution. This undercut etch completes the removal of the host substrate 200.

10 To complete the fabrication of the micro-LED devices, the sample is patterned for n-contact deposition and an n-type contact (n-contact 500) is deposited on the device structure, as illustrated in FIG. 5. FIG. 5 is a schematic of an example processed device structure that has been flip-chip bonded to the submount 408, illustrating the n-contact 500, and wherein the host substrate 200 has been removed.

15 Finally, a flexible and transparent thin film is blanket deposited to encapsulate and protect the device structure (Block 110).

De-laminating the polymer film from the submount (e.g., Block 112)

Finally, the polymer film 410 is de-laminated from the submount/wafer 408 (e.g.,
20 silicon wafer, e.g. using a razor blade or other means to cut the polymer film 410 around the devices), as represented by Block 110 of FIG. 1. The polymer film can be delaminated from the submount/wafer using a blade.

In one or more embodiments, the resulting product is a flexible array of III-nitride micro-LEDs (e.g., red, green, blue RGB LEDs) on the polymer film, as shown in FIG. 6,
25 which is a schematic of a flexible array of III-nitride micro-LEDs 600 having the LED structure of FIG. 5 on top of a thin layer of metal 602 on top of the flexible polymer substrate 604 (the encapsulating layer is not shown). The RGB LEDs can comprise at

least one LED emitting at a peak wavelength corresponding to red (R) light, at least one LED emitting at a peak wavelength corresponding to green (G) light, and at least one LED emitting at a peak wavelength corresponding to blue (B) light.

However, other devices can also be fabricated. One or more embodiments of the invention describe a method of fabricating a flexible array of III-nitride (e.g., micro devices), including but not limited to light-emitting devices (e.g., vertical-cavity surface-emitting lasers (VCSELs)) and detectors. For example, the device can comprise a transistor, a light emitting diode, a laser diode, a solar cell, or an array of devices such as an array of micro-LEDs, lasers, solar cells, or transistors, grown from a III-nitride (e.g., GaN) substrate and formed on a flexible substrate.

Thus, FIGs. 1-6 illustrate an optoelectronic or electronic device (e.g., a transistor, a light emitting diode, a laser, or a solar cell), comprising a flexible polymer substrate; a III-nitride device structure on the flexible polymer substrate, the III-nitride device including an active layer between an n-type layer and a p-type layer, the optoelectronic or electronic device fabricated using a process comprising (a) growing a sacrificial layer on a host substrate, wherein the sacrificial layer comprises a III-nitride layer; (b) growing the III-nitride device structure on or above the sacrificial layer, wherein the III-nitride device structure comprises a top surface and a bottom surface, the bottom surface interfacing the sacrificial layer and opposite the top surface; (c) preparing a submount with a polymer film deposited thereon; (d) flip-chip bonding the top surface of the III-nitride device structure onto the polymer film of the submount; (e) removing the sacrificial layer to separate the host substrate from the device structure, wherein the sacrificial layer is removed using a photoelectrochemical (PEC) etch technique; and (f) de-laminating the polymer film from the submount. The device can comprise an array of micro-LEDs grown from a GaN substrate and formed on a flexible substrate, for example.

Possible Modifications and Variations

One or more embodiments of the invention describe how III-nitride micro devices grown on bulk GaN substrates can be flip-chip bonded to a flexible substrate on a submount and then lifted off from the rigid host substrate by a PEC etch. By choosing an appropriate flexible substrate, and by properly handling of the submount, a method according to one or more embodiments of the present invention can be used to fabricate a flexible array of III-nitride micro devices. One difficulty is that flip-chip wafer bonding to a flexible substrate is nearly impossible since there is no rigidity. By preparing a flexible film on a rigid substrate and then removing that flexible film, the difficulty in bonding can be overcome.

In this context, "micro devices" refers to devices with areas that may be less than 0.1 μm^2 and that may have side lengths of approximately 300 μm or less. However, the invention described herein may be applied to devices with larger areas and side lengths. The geometries of the devices may include rectangular, circular, or triangular shapes, although other device geometries not described here may also be used.

The method described herein applies to any of the orientations used with III-nitride devices. Specifically, the method of the present invention can be used with III-nitride thin films that are epitaxially grown in the c-direction [0001] on sapphire substrates or on various orientations used with bulk GaN substrates, such as the basal c-plane {0001}; nonpolar a-plane {1 1 -2 0} and m-plane {1 0 -1 0} families; and semipolar plane families such as {1 0 -1 1} and {2 0 -2 1}. However, other device materials compatible with PEC etching could also be used.

Advantages and Improvements

One or more embodiments of the present invention are commercially advantageous because they allow for the development of flexible arrays of III-nitride micro devices. Specifically, a flexible array of III-nitride (inorganic) LEDs can be

created. The flexible LED area is one that has been previously dominated by organic light-emitting diodes (OLEDs). Thus, one or more embodiments of the invention have many applications that include, but are not limited to, flexible displays for mobile phones and wearable electronics with curved surfaces and displays.

5 The use of the PEC liftoff technique will also allow for substrate recycling. Bulk GaN substrates are expensive, so the ability to reuse a bulk GaN substrate will be economical.

Nomenclature

10 GaN and its ternary and quaternary compounds incorporating aluminum and indium (AlGaN, InGaN, AlInGaN) are commonly referred to using the terms (Al,Ga,In)N, III-nitride, III-N, Group III-nitride, nitride, $Al_{(1-x-y)}In_yGa_xN$ where $0 < x < 1$ and $0 < y < 1$, any alloy composition of the (Ga,Al,In,B)N semiconductors having the formula $Ga_wAl_xIn_yB_zN$ where $0 \leq w \leq 1$, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$, and $w + x + y + z$
15 $= 1$, or AlInGaN, as used herein. All these terms are intended to be equivalent and broadly construed to include respective nitrides of the single species, Al, Ga, B, and In, as well as binary, ternary and quaternary compositions of such Group III metal species. Accordingly, these terms comprehend the compounds AlN, GaN, and InN, as well as the ternary compounds AlGaN, GaInN, and AlInN, and the quaternary compound AlGaInN,
20 as species included in such nomenclature. When two or more of the (Ga, Al, In) component species are present, all possible compositions, including stoichiometric proportions as well as "off-stoichiometric" proportions (with respect to the relative mole fractions present of each of the (Ga, Al, In) component species that are present in the composition), can be employed within the broad scope of the invention. Accordingly, it
25 will be appreciated that the discussion of the invention hereinafter in primary reference to GaN materials is applicable to the formation of various other (Al, Ga, In)N material species. Further, (Al,Ga,In)N materials within the scope of the invention may further

include minor quantities of dopants and/or other impurity or inclusional materials. Boron (B) may also be included.

One approach to eliminating the spontaneous and piezoelectric polarization effects in GaN or III-nitride based optoelectronic devices is to grow the III-nitride devices on nonpolar planes of the crystal. Such planes contain equal numbers of Ga (or group III atoms) and N atoms and are charge-neutral. Furthermore, subsequent nonpolar layers are equivalent to one another so the bulk crystal will not be polarized along the growth direction. Two such families of symmetry-equivalent nonpolar planes in GaN are the {11-20} family, known collectively as a-planes, and the {1-100} family, known collectively as m-planes. Thus, nonpolar III-nitride is grown along a direction perpendicular to the (0001) c-axis of the III-nitride crystal.

Another approach to reducing polarization effects in (Ga,Al,In,B)N devices is to grow the devices on semi-polar planes of the crystal. The term “semi-polar plane” (also referred to as “semipolar plane”) can be used to refer to any plane that cannot be classified as c-plane, a-plane, or m-plane. In crystallographic terms, a semi-polar plane may include any plane that has at least two nonzero h, i, or k Miller indices and a nonzero l Miller index.

Some commonly observed examples of semi-polar planes include the (11-22), (10-11), and (10-13) planes. Other examples of semi-polar planes in the wurtzite crystal structure include, but are not limited to, (10-12), (20-21), and (10-14). The nitride crystal’s polarization vector lies neither within such planes or normal to such planes, but rather lies at some angle inclined relative to the plane’s surface normal. For example, the (10-11) and (10-13) planes are at 62.98° and 32.06° to the c-plane, respectively.

Polar c-plane devices can also be fabricated. The Gallium or Ga face of GaN is the c^+ or (0001) plane, and the Nitrogen or N-face of GaN or a III-nitride layer is the c^- or (000-1) plane.

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The following publications, referenced above and incorporated by reference herein, are relevant to this disclosure:

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10

Conclusion

This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be
15 exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A method for fabricating an optoelectronic or electronic device, comprising:

5 (a) growing a sacrificial layer on a host substrate, wherein the sacrificial layer comprises a III-nitride layer;

(b) growing a III-nitride device structure on or above the sacrificial layer, wherein the III-nitride device structure comprises a top surface and a bottom surface, the bottom surface interfacing the sacrificial layer and opposite the top surface;

10 (c) preparing a submount with a polymer film deposited thereon;

(d) flip-chip bonding the top surface of the III-nitride device structure onto the polymer film of the submount;

(e) removing the sacrificial layer to separate the host substrate from the device structure, wherein the sacrificial layer is removed using a photoelectrochemical (PEC) 15 etch technique; and

(f) de-laminating the polymer film and the device strucure from the submount.

2. The method of claim 1, wherein the III-nitride device structure is grown by metalorganic chemical vapor deposition or molecular beam epitaxy.

20

3. The method of claim 1, wherein the III-nitride device structure includes an n-i-n structure.

4. The method of claim 1, wherein the host substrate is a bulk gallium nitride 25 (GaN) substrate.

5. The substrate of claim 4, wherein the bulk GaN substrate has a polar plane orientation.

6. The substrate of claim 4, wherein the bulk GaN substrate has a nonpolar
5 plane orientation.

7. The substrate of claim 4, wherein the bulk GaN substrate has a semipolar plane orientation.

10 8. The substrate of claim 1, wherein the host substrate has a threading dislocation (TD) density of less than 10^9 cm^{-2}.

9. The method of claim 1, wherein the submount is silicon.

15 10. The method of claim 1, wherein the submount is silicon carbide.

11. The method of claim 1, wherein the submount is sapphire.

12. The method of claim 1, wherein the polymer film is polyimide.

20

13. The method of claim 1, wherein the polymer film is polyethylene terephthalate.

14. The method of claim 1, wherein the PEC etch technique exposes the
25 sacrificial layer to a solution and applies light from a light source causing the sacrificial layer to etch in the solution.

15. The method of claim 14, wherein the solution comprises potassium hydroxide (KOH) and water, and the light has an approximate wavelength of 400 nanometers.

5 16. The method of claim 14, wherein:

the sacrificial layer is comprised of an InGaN/GaN multi quantum well (MQW), and

the InGaN composition of the InGaN layer in the sacrificial layer is tuned such that the InGaN layer's bandgap is smaller than a photon energy of the light.

10

17. The method of claim 1, wherein the polymer film is de-laminated from the submount using a blade.

18. The method of claim 1, wherein the preparing further comprises:

15 placing the polymer film onto the submount comprising a wafer;

curing the polymer film; and

depositing metal onto the polymer film, wherein the metal promotes bonding to a p-contact of the device structure.

20 19. The method of claim 18, wherein the delaminating further comprises delaminating the polymer film from the wafer.

20. The method of claim 1, further comprising patterning the III-nitride device structure into micro devices prior to the flip chip bonding.

25

21. The method of claim 20 wherein the devices have a surface area less than 0.1 μm^2 and the device structure has a thickness of 3 micrometers or less.

22. The method of claim 20, further comprising encapsulating the devices to protect the devices.

5 23. The method of claim 1, wherein the device comprises a transistor, a light emitting diode, a laser, or a solar cell.

24. An array of micro-optoelectronic or micro-electronic devices grown from a GaN substrate and formed on a flexible substrate.

10

25. An optoelectronic or electronic device, comprising:

a flexible polymer substrate;

a III-nitride device structure on the flexible polymer substrate, the III-nitride device including an active layer between an n-type layer and a p-type layer, the
15 optoelectronic or electronic device fabricated using a process comprising:

(a) growing a sacrificial layer on a host substrate, wherein the sacrificial layer comprises a III-nitride layer;

(b) growing the III-nitride device structure on or above the sacrificial layer, wherein the III-nitride device structure comprises a top surface and a bottom surface, the
20 bottom surface interfacing the sacrificial layer and opposite the top surface;

(c) preparing a submount with a polymer film deposited thereon;

(d) flip-chip bonding the top surface of the III-nitride device structure onto the polymer film of the submount;

(e) removing the sacrificial layer to separate the host substrate from the device
25 structure, wherein the sacrificial layer is removed using a photoelectrochemical (PEC) etch technique; and

(f) de-laminating the polymer film from the submount.

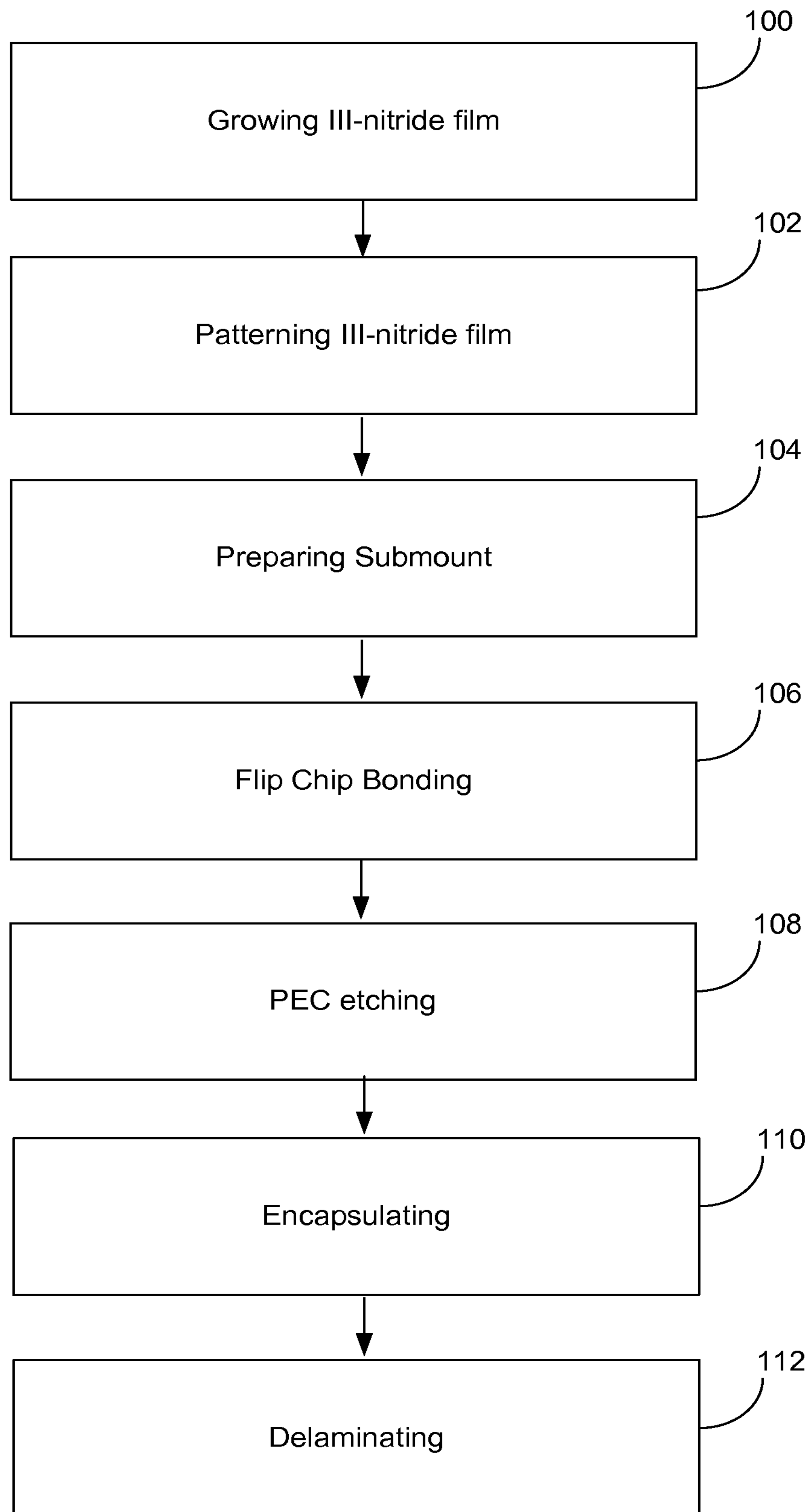

FIG. 1

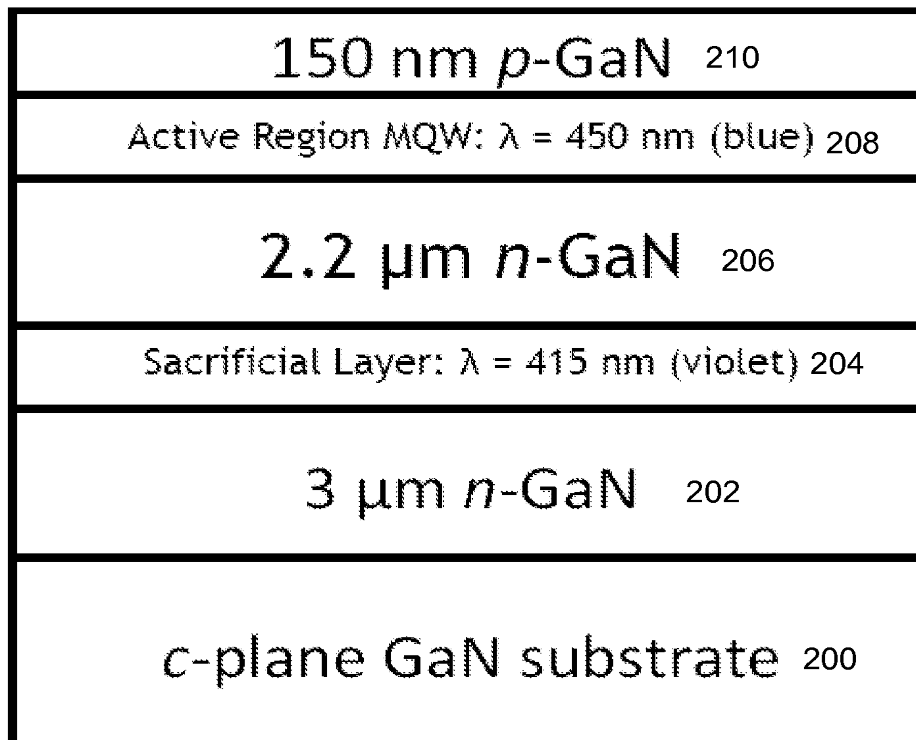

FIG. 2

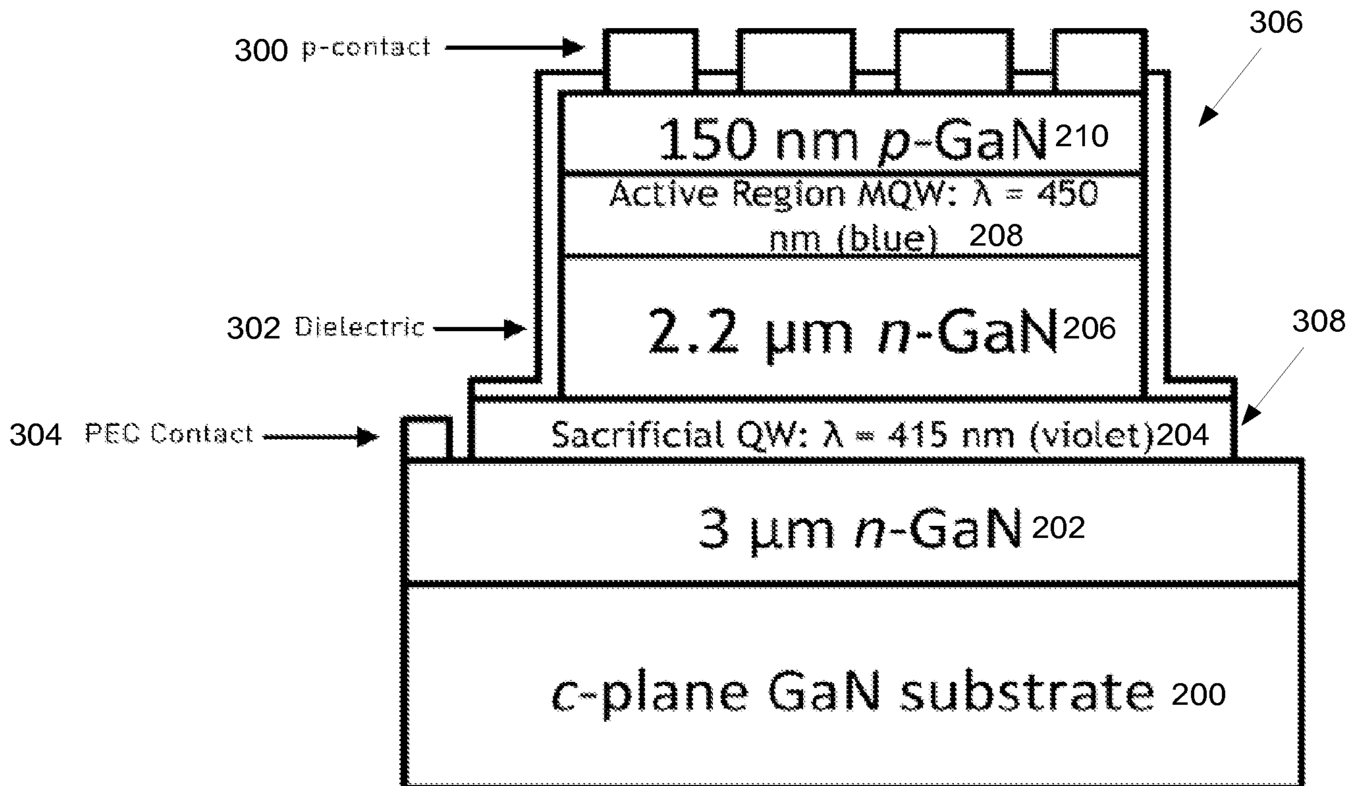

FIG. 3

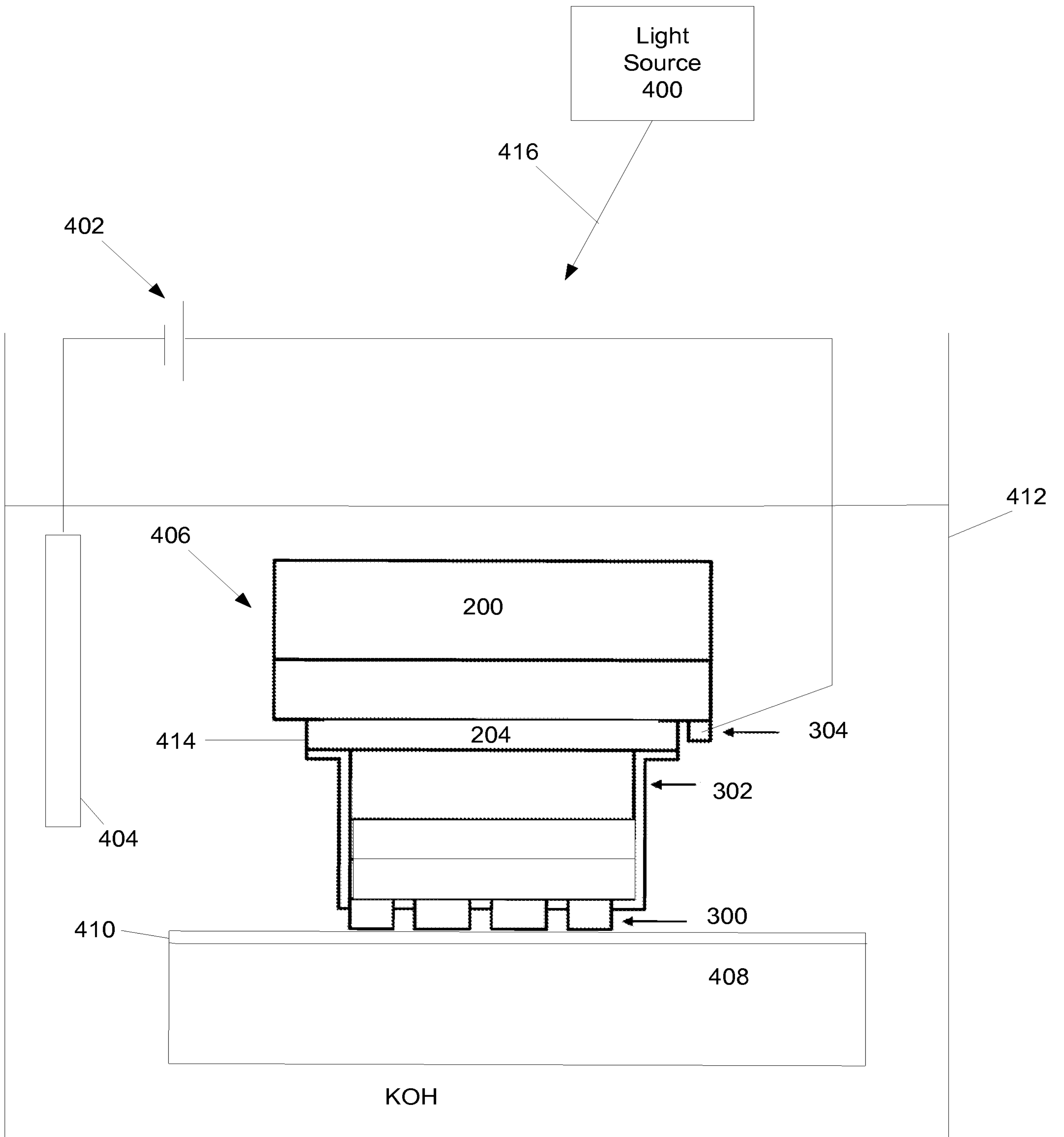

FIG. 4

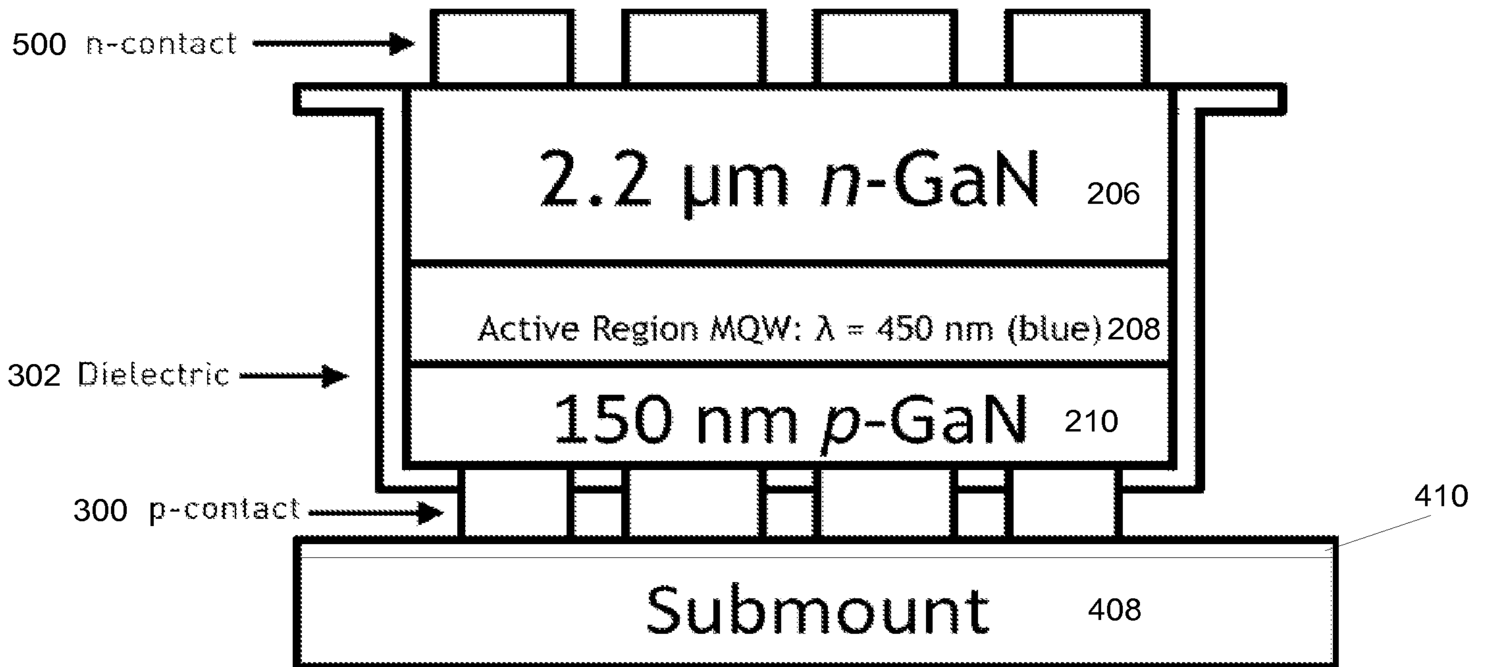

FIG. 5

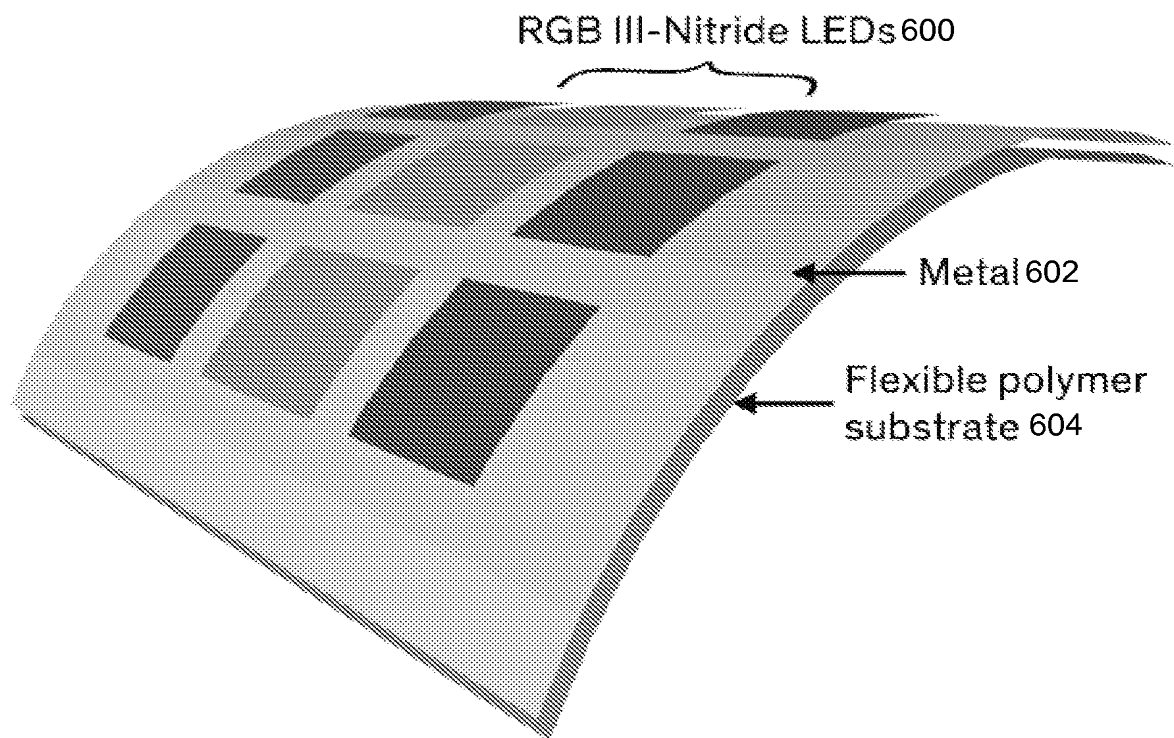

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/057850

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/02 (2015.01)
CPC - H01L 21/02 (2015.10)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/02, 21/04, 21/67, 21/673, 21/683, 21/761 (2015.01)
CPC - H01L 21/02, 21/02002, 21/02104, 21/022, 21/67, 21/673, 21/683, 21/76251 (2015.10)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 257/46, 100; 438/455, 458, 459 (Keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Orbit, Google Patents, Google Scholar
Search terms used: micro, array, flexible, GaN, gallium nitride, grow, submount, flip-chip, PEC, nin, bulk, PEM, de-laminate blade, KOH, water, tunable, bandgap

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,420,242 B1 (CHEUNG et al) 16 July 2002 (16.07.2002) entire document	24
Y	US 2010/0109030 A1 (KRAMES et al) 06 May 2010 (06.05.2010) entire document	1-23, 25
Y	US 2011/0023672 A1 (BLANCHARD et al) 03 February 2011 (03.02.2011) entire document	1-23, 25
Y	US 4,804,638 A (HOKE et al) 14 February 1989 (14.02.1989) entire document	2
Y	US 2006/0267007 A1 (SALZMAN et al) 30 November 2006 (30.11.2006) entire document	3
Y	US 2012/0097919 A1 (SPECK et al) 26 April 2012 (26.04.2012) entire document	4-8
Y	US 2008/0096365 A1 (CHITNIS) 24 April 2008 (24.04.2008) entire document	10, 11
Y	US 2005/0161689 A1 (NARAYAN et al) 28 July 2005 (28.07.2005) entire document	16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2015	21 JAN 2016

Name and mailing address of the ISA/	Authorized officer
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774