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(54) APPARATUS AND CIRCUITS WITH DUAL THRESHOLD VOLTAGE TRANSISTORS AND METHODS OF FABRICATING THE SAME

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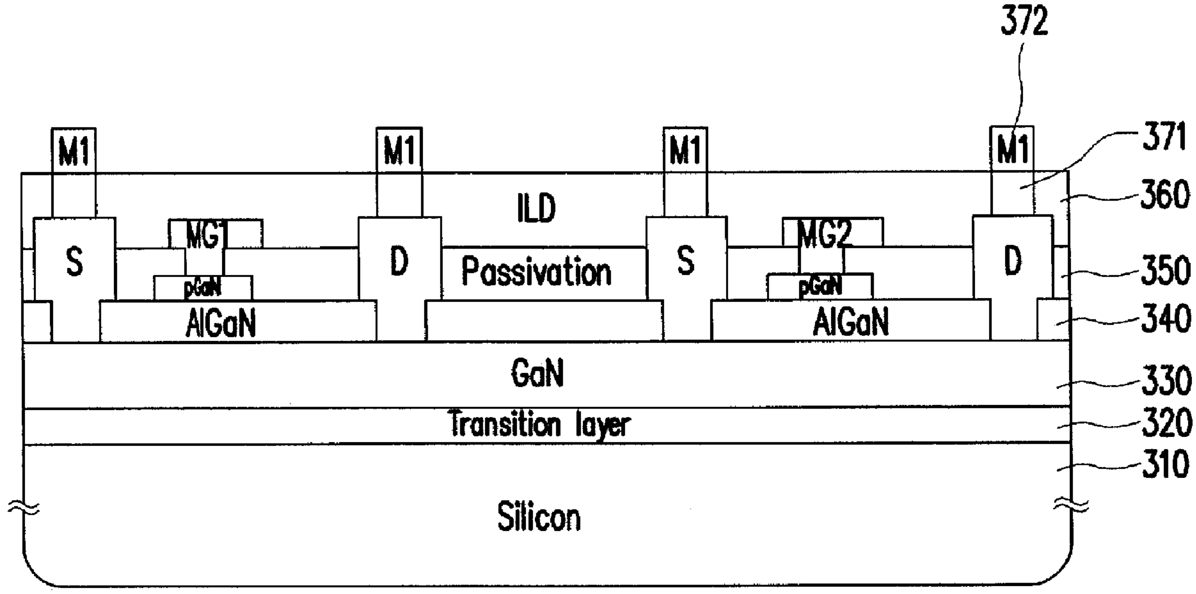
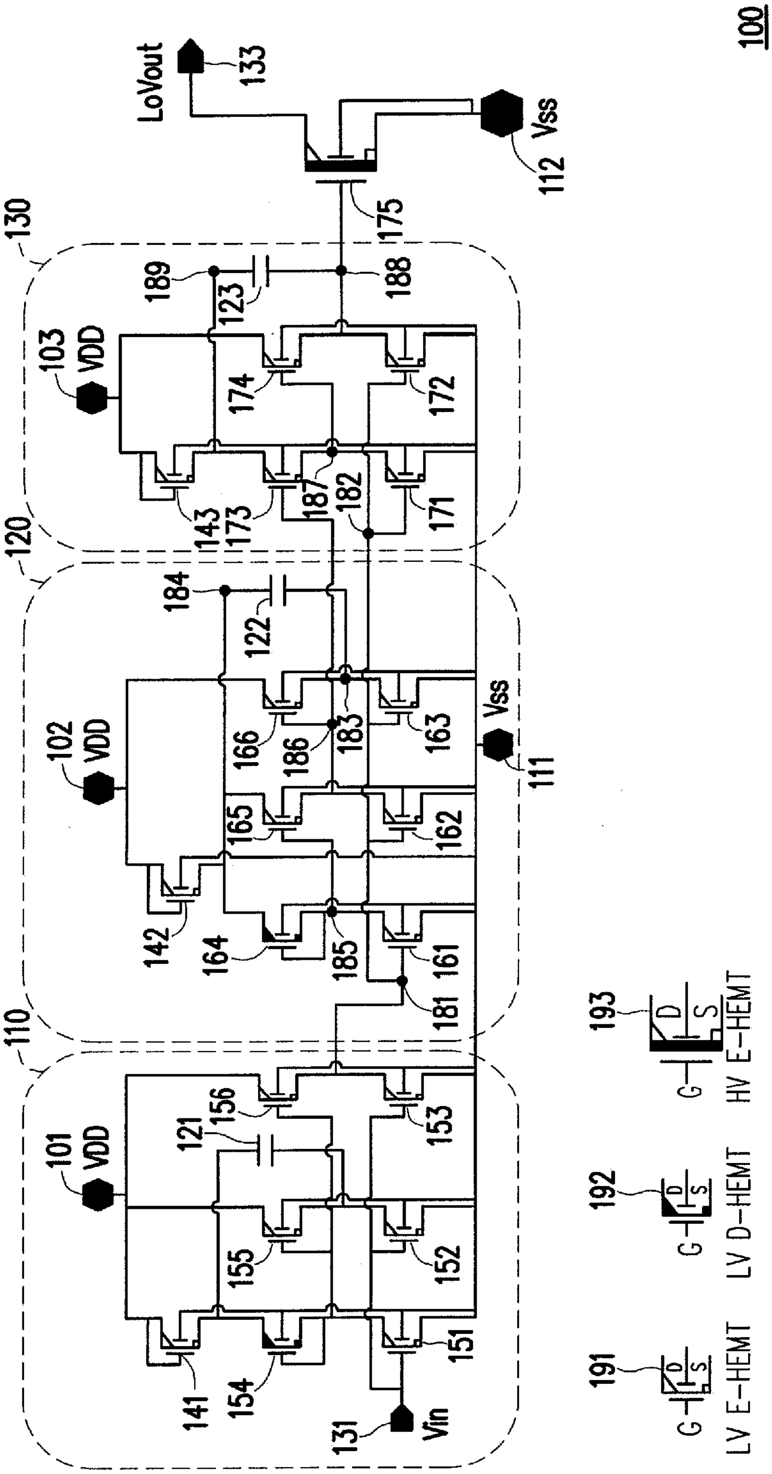
(57) ABSTRACT

Apparatus and circuits with dual threshold voltage transistors and methods of fabricating the same are disclosed. In one example, a semiconductor structure is disclosed. The semiconductor structure includes: a substrate; a first layer comprising a first III-V semiconductor material formed over the substrate; a first transistor formed over the first layer, and a second transistor formed over the first layer. The first transistor comprises a first gate structure comprising a first material, a first source region and a first drain region. The second transistor comprises a second gate structure comprising a second material, a second source region and a second drain region. The first material is different from the second material.

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LoVout
133
Vss
112
175
130
189
123
188
103
VDD
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172
143
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187
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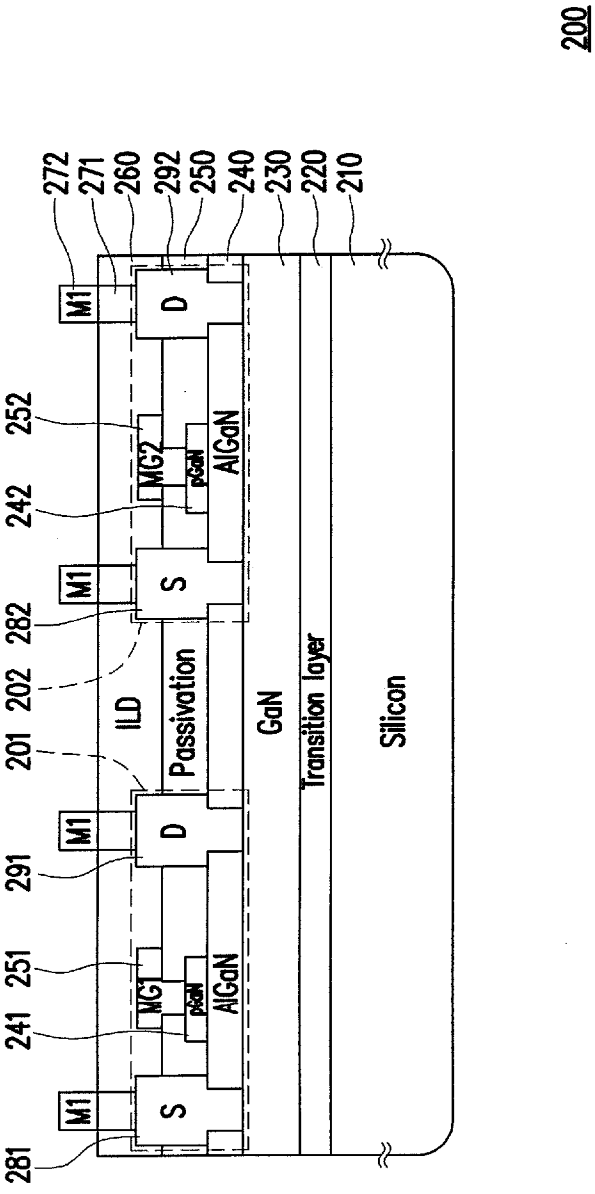
171
120
184
122
102
VDD
166
186
183
163
165
162
Vss
111
142
164
185
161
181
110
101
VDD
121
156
153
155
152
141
154
151
131
Vin
191
G
D
S
LV E-HEMT
192
G
D
S
LV D-HEMT
193
G
D
S
HV E-HEMT

FIG. 1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272
271
260
292
250
240
230
220
210
M1
D
MG2
pGaN
AlGaN
252
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M1
S
282
202
ILD
Passivation
GaN
Transition layer
Silicon
201
M1
D
291
251
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MG1
pGaN
AlGaN
M1
S
281

FIG. 2

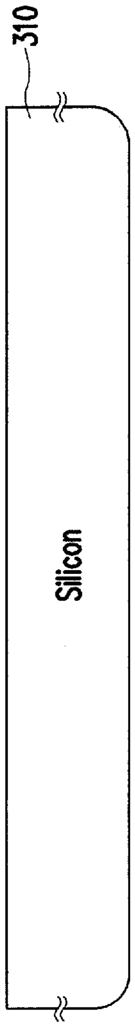


FIG. 3A

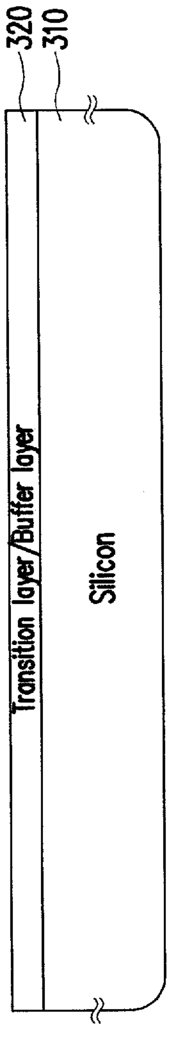


FIG. 3B

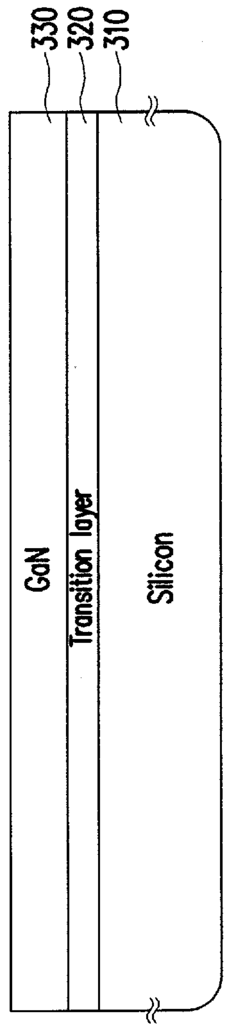


FIG. 3C

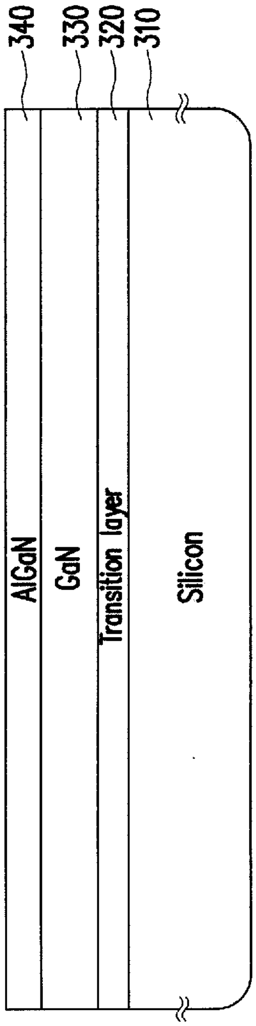
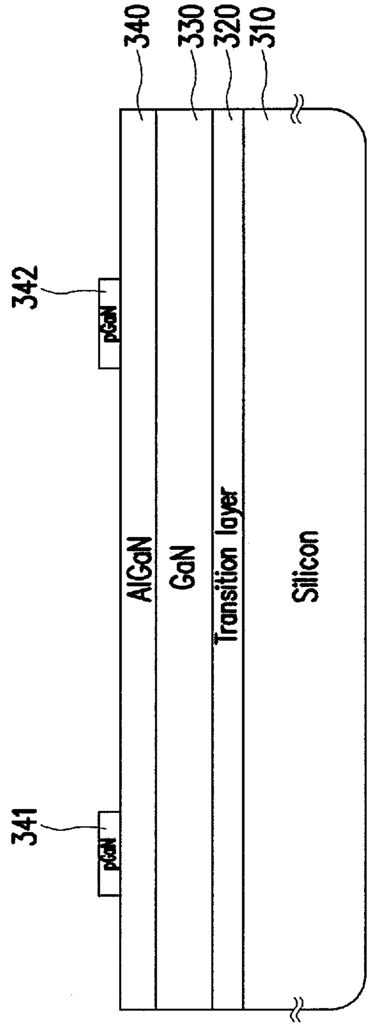


FIG. 3D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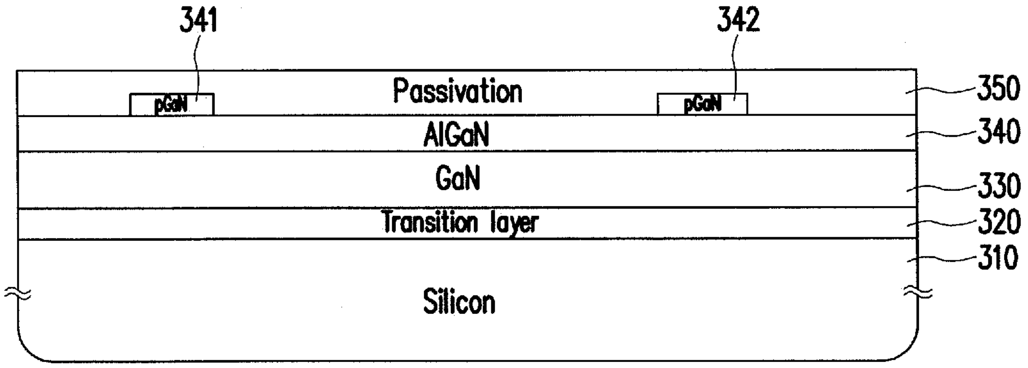
330
320
310
342
pGaN
AlGaN
GaN
Transition layer
Silicon
341
pGaN

FIG. 3E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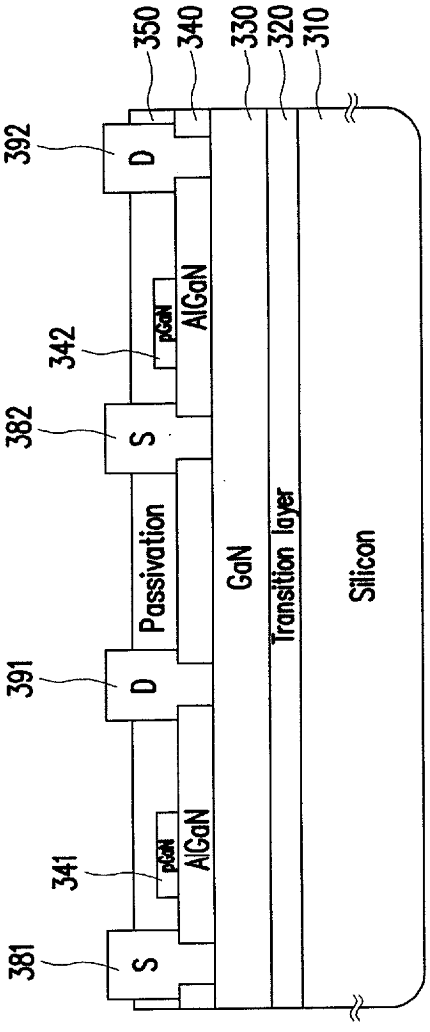
AlGaN
GaN
Transition layer
Silicon
350
340
330
320
310

FIG. 3F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320
310
392
D
342
pGaN
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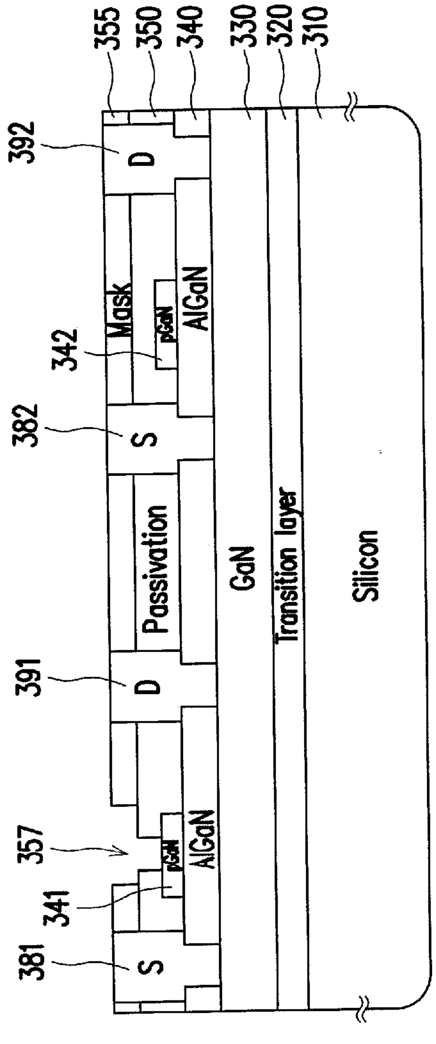
S
Passivation
GaN
Transition layer
Silicon
391
D
341
pGaN
AlGaN
381
S

FIG. 3G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330
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310
392
D
Mask
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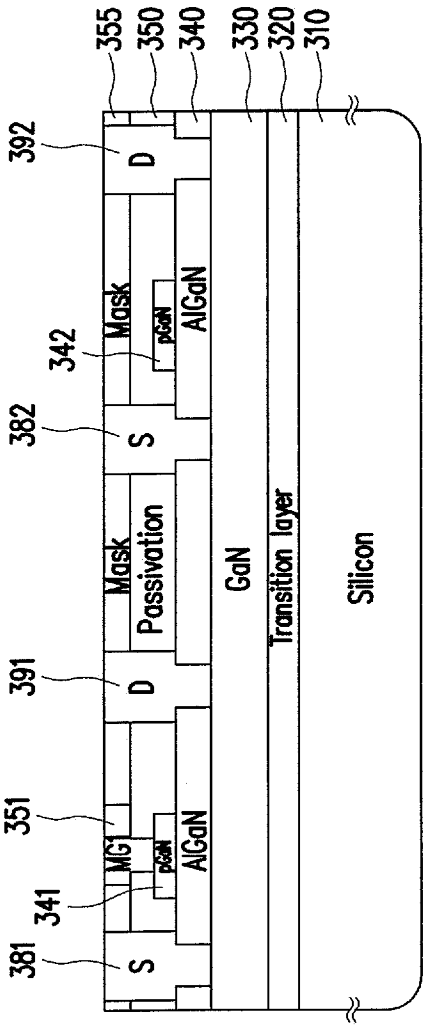
AlGaN
342
382
S
Passivation
GaN
Transition layer
Silicon
391
D
357
341
pGaN
AlGaN
381
S

FIG. 3H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D
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AlGaN
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Passivation
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Transition layer
Silicon
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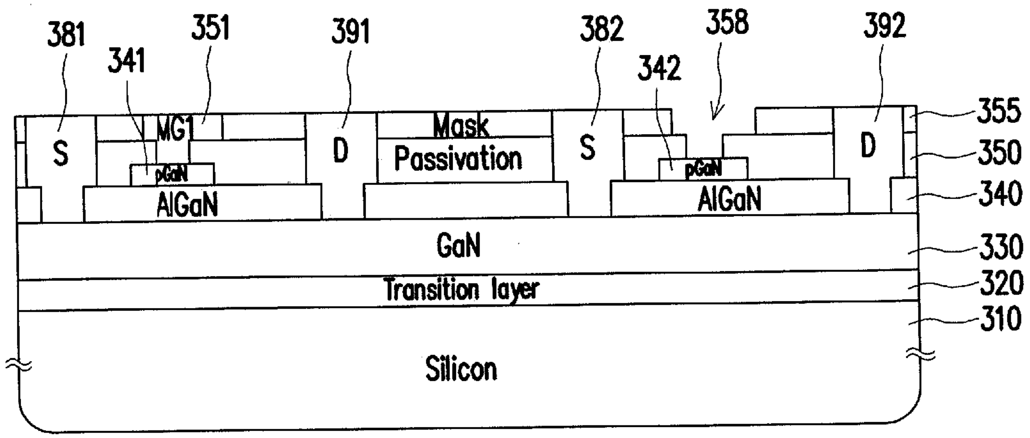
D
351
MG1
341
pGaN
AlGaN
381
S

FIG. 3I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391
382
342
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392
S
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AlGaN
D
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Passivation
S
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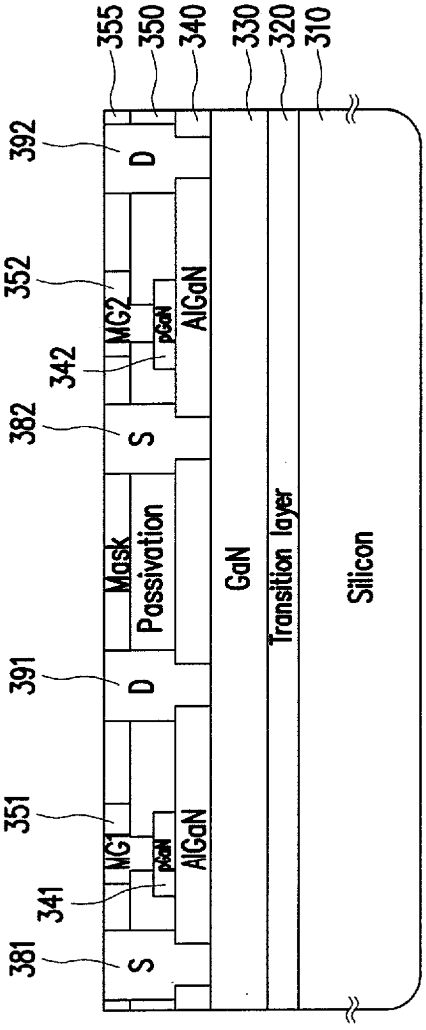
AlGaN
D
355
350
340
GaN
330
Transition layer
320
310
Silicon

FIG. 3J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320
310
392
D
352
MG2
pGaN
AlGaN
342
382
S
Mask
Passivation
GaN
Transition layer
Silicon
391
D
351
MG1
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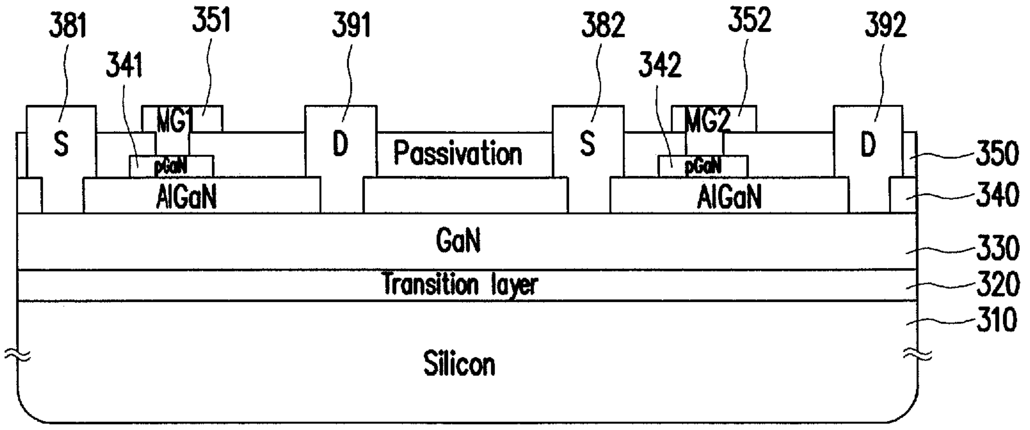
AlGaN
341
381
S

FIG. 3K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382
342
352
392
S
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D
Passivation
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MG2
pGaN
D
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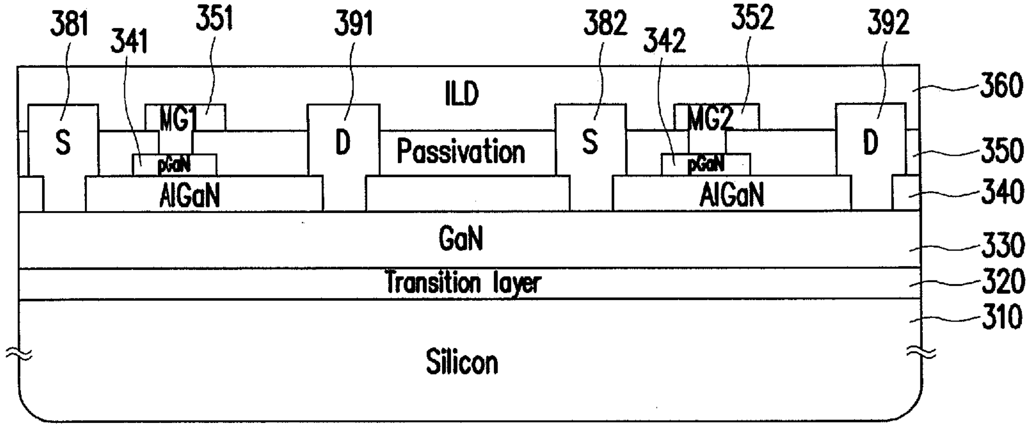
AlGaN
GaN
Transition layer
Silicon
350
340
330
320
310

FIG. 3L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S
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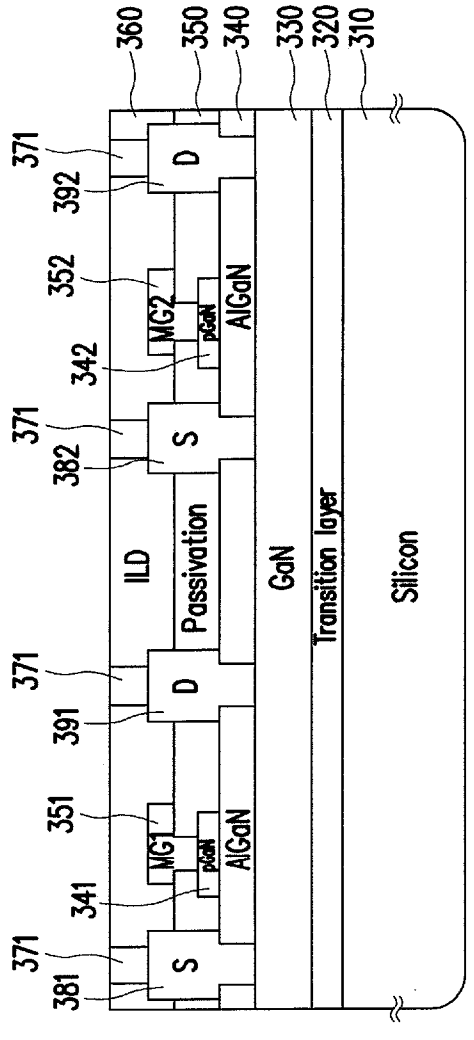
Transition layer
Silicon

FIG. 3M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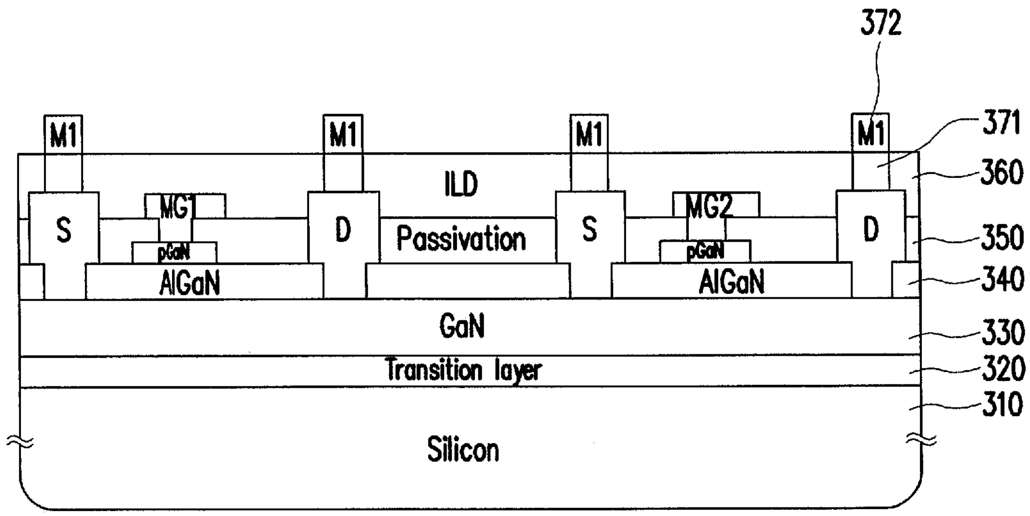
320
310

FIG. 3N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M1
M1
M1
371
360
ILD
MG1
MG2
S
D
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AlGaN
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GaN
330
Transition layer
320
310
Silicon

FIG. 30

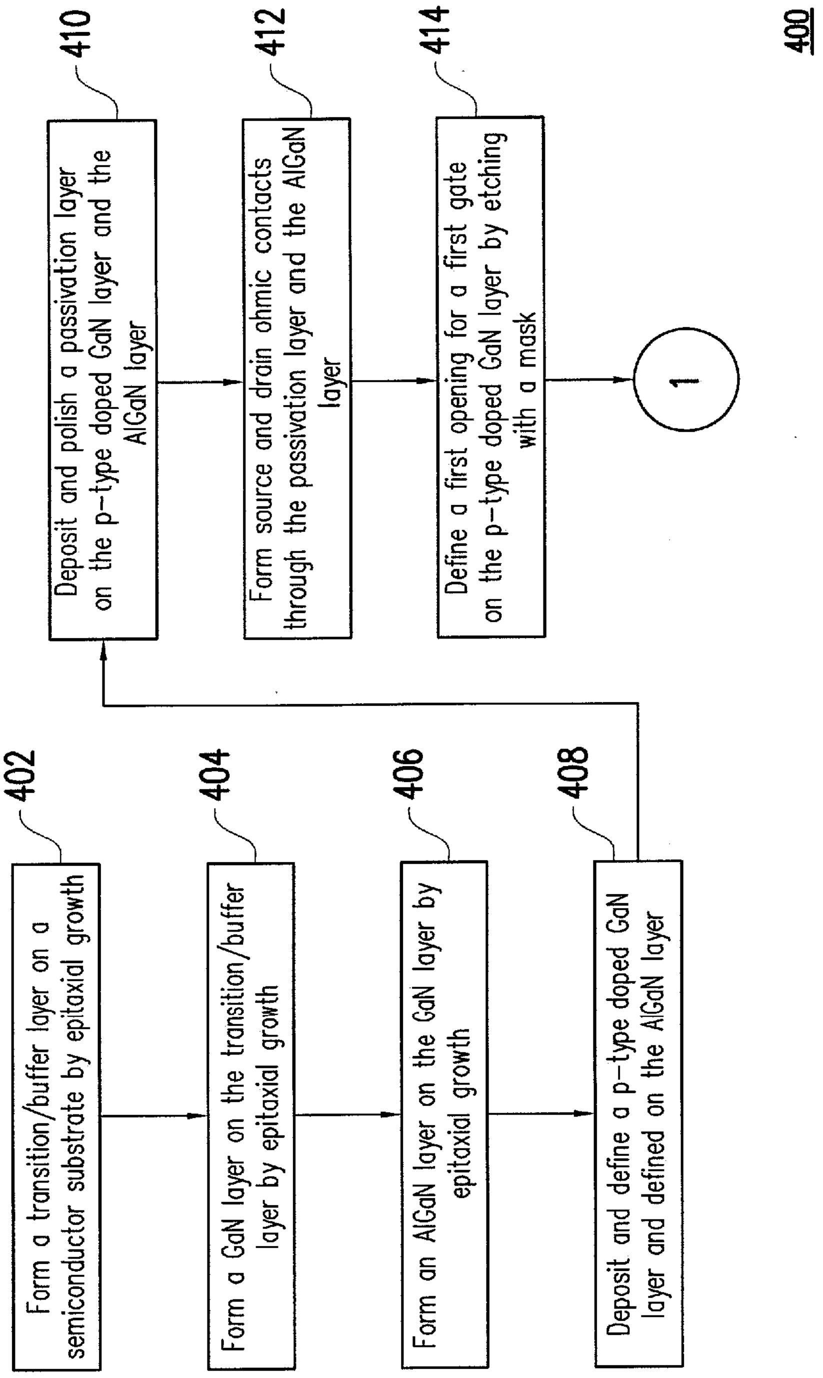
Form a transition/buffer layer on a semiconductor substrate by epitaxial growth
402
Form a GaN layer on the transition/buffer layer by epitaxial growth
404
Form an AlGaN layer on the GaN layer by epitaxial growth
406
Deposit and define a p-type doped GaN layer and defined on the AlGaN layer
408
Deposit and polish a passivation layer on the p-type doped GaN layer and the AlGaN layer
410
Form source and drain ohmic contacts through the passivation layer and the AlGaN layer
412
Define a first opening for a first gate on the p-type doped GaN layer by etching with a mask
414
1
400

FIG. 4A

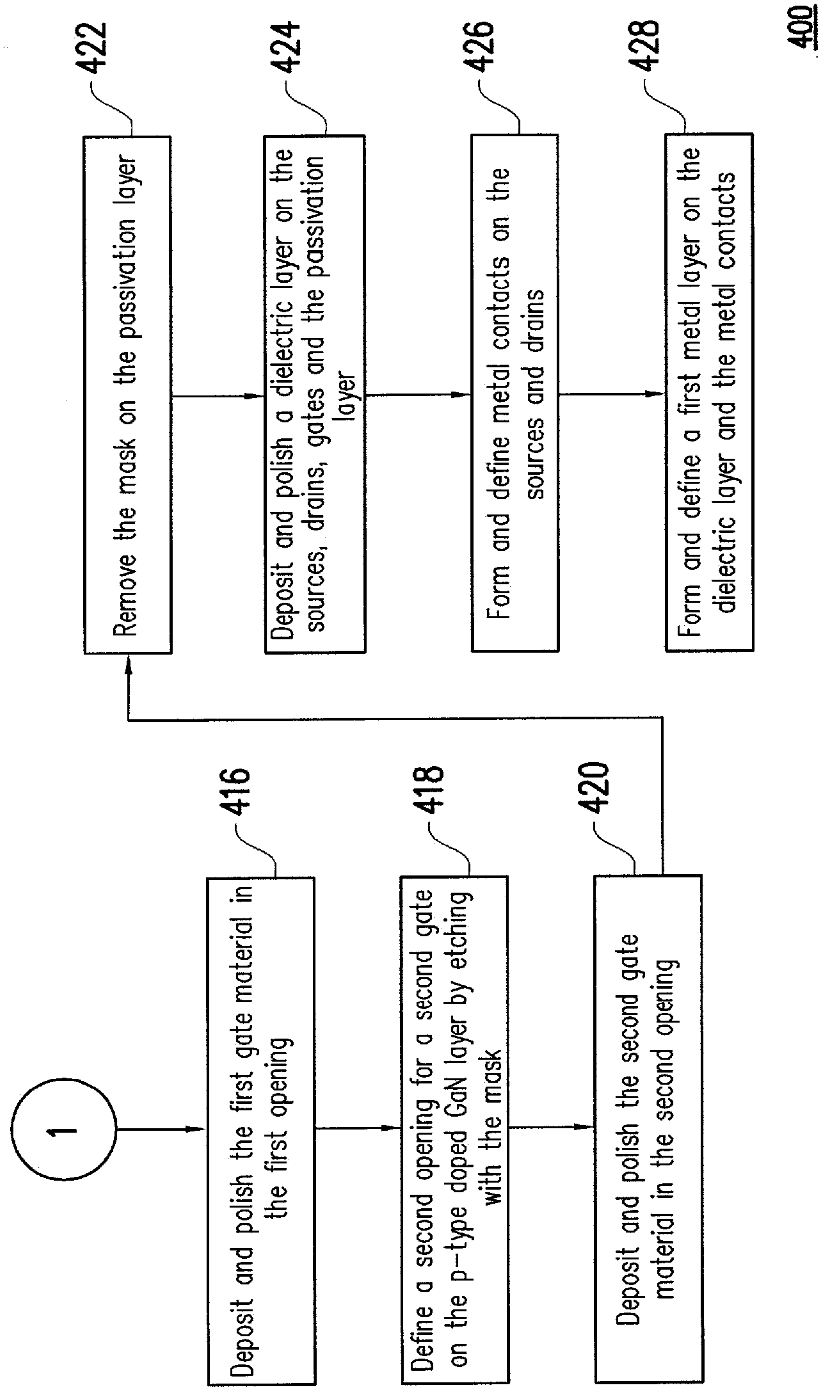
1
416
Deposit and polish the first gate material in the first opening
418
Define a second opening for a second gate on the p-type doped GaN layer by etching with the mask
420
Deposit and polish the second gate material in the second opening
422
Remove the mask on the passivation layer
424
Deposit and polish a dielectric layer on the sources, drains, gates and the passivation layer
426
Form and define metal contacts on the sources and drains
428
Form and define a first metal layer on the dielectric layer and the metal contacts
400

FIG. 4B

APPARATUS AND CIRCUITS WITH DUAL THRESHOLD VOLTAGE TRANSISTORS AND METHODS OF FABRICATING THE SAME

RELATED APPLICATION

[0001] This application claims priority to U.S. Provisional Patent Application No. 62/753,484, entitled "APPARATUS WITH DUAL THRESHOLD VOLTAGE TRANSISTORS AND METHOD OF FABRICATING THE SAME," and filed on Oct. 31, 2018, the entirety of which is incorporated by reference herein.

BACKGROUND

[0002] In an integrated circuit (IC), an enhancement-mode N-type transistor, e.g. enhancement-mode high-electron-mobility transistor (E-HEMT), may be used as a pull-up device to minimize static current. In order to achieve near full-rail pull-up voltage and fast slew rate, a significantly large over-drive voltage is needed for an N-Type enhancement-mode transistor. That is, the voltage difference between gate and source (Vgs) should be much larger than the threshold voltage (Vt), i.e. (Vgs−Vt>>0). It is imperative to use a multi-stage E-HEMT based driver for integrated circuit to minimize static current. Nevertheless, multi-stage E-HEMT based drivers will not have enough over-drive voltage (especially for the last-stage driver) due to one Vt drop across each stage of E-HEMT pull-up device and one forward voltage (Vf) drop across boot-strap diode. Although one can reduce the Vt for the pull-up E-HEMT transistors and Vf of diode-connected E-HEMT rectifier of multi-stage drivers to provide significantly enough over-drive voltage and dramatically reduce static current, the noise immunity will be compromised.

[0003] In an existing semiconductor wafer, transistors formed on the wafer have identical structure such that they have a same threshold voltage Vt. When Vt of one transistor is reduced, Vt's of other transistors on the wafer are reduced accordingly. As Vt being reduced in this case, a power switch HEMT driven by the HEMT-based driver will have a poor noise immunity because the power switch HEMT cannot withstand a large back-feed-through impulse voltage to its gate. Thus, existing apparatus and circuits including multiple transistors are not entirely satisfactory.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that various features are not necessarily drawn to scale. In fact, the dimensions and geometries of the various features may be arbitrarily increased or reduced for clarity of discussion. Like reference numerals denote like features throughout specification and drawings.

[0005] FIG. **1** illustrates an exemplary circuit having a multi-stage boot-strapped driver, in accordance with some embodiments of the present disclosure.

[0006] FIG. **2** illustrates a cross-sectional view of an exemplary semiconductor device including dual threshold voltage transistors, in accordance with some embodiments of the present disclosure.

[0007] FIGS. **3**A, **3**B, **3**C, **3**D, **3**E, **3**F, **3**G, **3**H, **3**I, **3**J, **3**K, **3**L, **3**M, **3**N and **3**O illustrate cross-sectional views of an exemplary semiconductor device during various fabrication stages, in accordance with some embodiments of the present disclosure.

[0008] FIG. **4**A and FIG. **4**B show a flow chart illustrating an exemplary method for forming a semiconductor device including dual threshold voltage transistors, in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0009] The following disclosure describes various exemplary embodiments for implementing different features of the subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0010] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly. Terms such as "attached," "affixed," "connected" and "interconnected," refer to a relationship wherein structures are secured or attached to one another either directly or indirectly through intervening structures, as well as both movable or rigid attachments or relationships, unless expressly described otherwise.

[0011] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0012] Reference will now be made in detail to the present embodiments of the disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0013] An enhancement-mode high-electron-mobility transistor (HEMT), e.g. a gallium nitride (GaN) HEMT, has superior characteristics to enable high performance and smaller form factor in power conversion and radio frequency power amplifier and power switch applications compared to silicon based transistors. But there is no viable p-type

HEMT available mostly due to much lower p-type mobility and partly due to two dimensional hole gas (2DHG) band structure. While n-type GaN HEMTs are used in an integrated circuit, to minimize static current, the pull-up devices are mostly based on enhancement-mode n-type transistors rather than depletion-mode n-type transistors.

[0014] A multi-stage HEMT based driver can be used for an integrated circuit to minimize static current. But multi-stage HEMT based drivers will not have enough over-drive voltage (especially for the last-stage driver) due to one threshold voltage (Vt) drop across each stage of HEMT pull-up device and one forward voltage (Vf) drop across boot-strap diode. Although one can reduce the Vt for the pull-up HEMT transistors and Vf of diode-connected HEMT rectifier of multi-stage drivers to provide significantly enough over-drive voltage and dramatically reduce static current, the noise immunity will be compromised.

[0015] Instead of reducing a single value of the threshold voltage (Vt) of the HEMT transistors in an IC, the present teaching discloses apparatus and circuits including dual-Vt transistors and their fabrication process. In one embodiment, two transistors formed on a same wafer have different Vt's. In particular, two transistors have different metal gate materials for their gates respectively to obtain different Vt's from each other. While a lower work-function material, e.g. tungsten (W) or titanium/tungsten/titanium-nitride (Ti/W/TiN) metal stack, can be used for implementing a high-Vt HEMT; a higher work-function material, e.g. nickel (Ni) or titanium/nickel/titanium-nitride (Ti/Ni/TiN) metal stack, can be used for implementing a low-Vt HEMT. In an exemplary method of fabricating the dual-Vt transistors, the two metal gates can be formed on a polarization modulation layer by depositing and polishing different work-function materials with a mask.

[0016] The disclosed apparatus can adjust the work function differences in the metal-gate to create dual-Vt (or various-Vt) transistors on a same semiconductor wafer; and generate different amount of 2-Dimensional Electron Gas (2-DEG) for transistors at different locations of the same wafer at thermal equilibrium.

[0017] The present disclosure is applicable to any transistor based IC. The proposed apparatus and methods can enable a transistor based IC to reduce the static current significantly and have significantly large over-drive voltages for drivers of concern; without compromising noise immunity while increasing over-drive voltages and reducing static currents. In addition, the disclosed apparatus and methods can provide IC designers the flexibility of using different Vt devices for specific functions of improving performance, reducing static current, improving noise immunity, etc.

[0018] FIG. **1** illustrates an exemplary circuit **100** having a multi-stage boot-strapped driver, in accordance with some embodiments of the present disclosure. As shown in FIG. **1**, the circuit **100** includes a driver having multiple stages **110**, **120**, **130** serially connected to drive a power switch HEMT **175**. Each stage includes multiple transistors.

[0019] The stage **110** in this example includes transistors **141**, **151**, **152**, **153**, **154**, **155**, **156**. In one embodiment, among these transistors, the transistor **154** is a low voltage depletion-mode high electron mobility transistor (LV D-HEMT) **192**; while each of the other transistors **141**, **151**, **152**, **153**, **155**, **156** is a low voltage enhancement-mode high electron mobility transistor (LV E-HEMT) **191**.

[0020] As shown in FIG. **1**, the gate of the transistor **151** is electrically connected to an input pin **131** of the circuit **100**. The input pin **131** has an input voltage Vin ranged from a low logic state voltage (e.g. 0V) to a high logic state voltage (e.g. 6V). When the circuit **100** is turned off, the Vin is 0. The circuit **100** is turned on after the Vin is increased to 6V. The transistor **151** has a source electrically connected to ground Vss **111** which has a ground voltage 0V; and has a drain electrically connected to a source of the transistor **154**. The transistor **152** in this example has a gate electrically connected to the input pin **131**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **155**. Similarly, the transistor **153** in this example has a gate electrically connected to the input pin **131**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **156**.

[0021] The transistor **154** in this example has a gate electrically connected to its own source, which is electrically connected to the drain of the transistor **151**. Drain of the transistor **154** is electrically connected to a source of the transistor **141**. The transistor **155** in this example has a gate electrically connected to the source of the transistor **154** and electrically connected to the drain of the transistor **151**. The transistor **155** has a source electrically connected to the drain of the transistor **152**, and a drain electrically connected to a power supply pin VDD **101** which has a positive power supply voltage (e.g. 6V). Similarly, the transistor **156** in this example has a gate electrically connected to the source of the transistor **154** and electrically connected to the drain of the transistor **151**, a source electrically connected to the drain of the transistor **153**, and a drain electrically connected to the power supply pin VDD **101** which has a positive power supply voltage 6V.

[0022] The transistor **141** in this example has a gate electrically connected to its own drain, which is electrically connected to the power supply pin VDD **101** which has a positive power supply voltage 6V. The transistor **141** connected in this specific configuration is functioning like a rectifier or diode and is conventionally called as a diode-connected transistor. Source of the transistor **141** is electrically connected to the drain of the transistor **154**. The stage **110** further includes a capacitor **121** coupled between the source of the transistor **141** and the source of the transistor **155**.

[0023] The stage **120** in this example includes transistors **142**, **161**, **162**, **163**, **164**, **165**, **166**. In one embodiment, among these transistors, the transistor **164** is a low voltage depletion-mode high electron mobility transistor (LV D-HEMT) **192**; while each of the other transistors **142**, **161**, **162**, **163**, **165**, **166** is a low voltage enhancement-mode high electron mobility transistor (LV E-HEMT) **191**.

[0024] As shown in FIG. **1**, the gate of the transistor **161** is electrically connected to a node **181**, which is electrically connected to the source of the transistor **156** and the drain of the transistor **153**. The node **181** has a voltage ranged between Vss and VDD (0 and 6V). When the circuit **100** is turned off, the Vin is 0, such that the transistor **153** is turned off and the transistor **156** is turned on. The node **181** has the same voltage 6V as the power supply pin VDD **101**. When the circuit **100** is turned on and the Vin has a voltage of 6V, the transistor **153** is turned on and the transistor **156** is turned off. The node **181** has the same voltage 0V as the ground Vss **111**.

[0025] The transistor **161** has a source electrically connected to ground Vss **111** which has a ground voltage 0V; and has a drain electrically connected to a source of the transistor **164**. The transistor **162** in this example has a gate electrically connected to the node **181**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **165**. Similarly, the transistor **163** in this example has a gate electrically connected to the node **181**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **166**.

[0026] The transistor **164** in this example has a gate electrically connected to its own source, which is electrically connected to the drain of the transistor **161**. Drain of the transistor **164** is electrically connected to a source of the transistor **142**. The transistor **165** in this example has a gate electrically connected to a node **185**, which is electrically connected to the source of the transistor **164** and electrically connected to the drain of the transistor **161**. The transistor **165** has a source electrically connected to the drain of the transistor **162**, and a drain electrically connected to the source of the transistor **142**. The transistor **166** in this example has a gate electrically connected to a node **186**, which is electrically connected to the source of the transistor **165** and electrically connected to the drain of the transistor **162**, a source electrically connected to the drain of the transistor **163**, and a drain electrically connected to a power supply pin VDD **102** which has a positive power supply voltage (e.g. 6V).

[0027] The transistor **142** in this example has a gate electrically connected to its own drain (i.e. diode-connected to act like a rectifier or diode), which is electrically connected to the power supply pin VDD **102** which has a positive power supply voltage 6V. Source of the transistor **142** is electrically connected to the drain of the transistor **164** and the drain of the transistor **165**. The stage **120** further includes a capacitor **122** coupled between a node **184** electrically connected to the source of the transistor **142** and a node **183** electrically connected to the source of the transistor **166**.

[0028] The stage **130** in this example includes transistors **143**, **171**, **172**, **173**, **174**. In one embodiment, each of these transistors is a low voltage enhancement-mode high electron mobility transistor (LV E-HEMT) **191**. As shown in FIG. **1**, the gate of the transistor **171** is electrically connected to a node **182**, which is electrically connected to the node **181**, the source of the transistor **156** and the drain of the transistor **153**. Same as the node **181**, the node **182** has a voltage ranged between Vss and VDD (0 and 6V). When the circuit **100** is turned off, the Vin is 0, such that the transistor **153** is turned off and the transistor **156** is turned on. The node **181** and the node **182** have the same voltage 6V as the power supply pin VDD **101**. When the circuit **100** is turned on and the Vin has a voltage of 6V, the transistor **153** is turned on and the transistor **156** is turned off. The node **181** and the node **182** have the same voltage 0V as the ground Vss **111**.

[0029] The transistor **171** has a source electrically connected to ground Vss **111** which has a ground voltage 0V; and has a drain electrically connected to a source of the transistor **173**. The transistor **172** in this example has a gate electrically connected to the node **182**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **174**.

[0030] The transistor **173** in this example has a gate electrically connected to the node **186**, which is electrically connected to the source of the transistor **165**. The transistor **173** has a source electrically connected to the drain of the transistor **171**, and a drain electrically connected to a source of the transistor **143**. The transistor **174** in this example has a gate electrically connected to a node **187**, which is electrically connected to the source of the transistor **173** and electrically connected to the drain of the transistor **171**. The transistor **174** has a source electrically connected to the drain of the transistor **172**, and a drain electrically connected to a power supply pin VDD **103** which has a positive power supply voltage (e.g. 6V).

[0031] The transistor **143** in this example has a gate electrically connected to its own drain (i.e. diode-connected to act like a rectifier or diode), which is electrically connected to the power supply pin VDD **103** which has a positive power supply voltage 6V. Source of the transistor **143** is electrically connected to the drain of the transistor **173**. The stage **130** further includes a capacitor **123** coupled between a node **189** electrically connected to the source of the transistor **143** and a node **188** electrically connected to the source of the transistor **174**.

[0032] As such, the stages **110**, **120**, **130** are serially connected to form a multi-stage driver that drives a power switch transistor **175**. In one embodiment, the power switch HEMT **175** is a high voltage enhancement-mode high electron mobility transistor (HV E-HEMT) **193**. As shown in FIG. **1**, the power switch HEMT **175** has a gate electrically connected to the node **188**, a source electrically connected to ground Vss **112** which has a ground voltage 0V, and a drain electrically connected to an output pin **133** of the circuit **100**. In some embodiments, the circuit **100** can serve as a low-side driver in a half-bridge or full-bridge power converter, where the output pin **133** serves as a low-side voltage output (LoVout).

[0033] Most transistors in FIG. **1** are enhancement-mode N-type transistors. That is, the circuit **100** uses mostly enhancement-mode N-type transistors as pull-up devices to minimize static current. In order to achieve near full-rail pull-up voltage and fast slew rate, a significantly large over-drive voltage is needed for the N-Type enhancement-mode transistor. That is, the voltage difference between gate and source (Vgs) should be much larger than the threshold voltage (Vt), i.e. (Vgs−Vt>>0). While the multi-stage driver of the circuit **100** can minimize static current, each stage of E-HEMT pull-up device consumes at least one Vt voltage drop.

[0034] As discussed above, the node **181** has a voltage ranged between Vss and VDD (0 and 6V). When the circuit **100** is turned off, the Vin is 0, such that the transistor **153** is turned off and the transistor **156** is turned on. The node **181** has the same voltage 6V as the power supply pin VDD **101**, which enables the transistors **161**, **162**, **163** to be turned on. As such, the node **185** is electrically connected to the ground Vss **111**, and has a voltage close to 0V. As such, the transistor **165** is turned off, and the node **186** is electrically connected to the ground Vss **111** and has a voltage 0V. Accordingly, the transistor **166** is turned off, and the node **183** is electrically connected to the ground Vss **111** and has a voltage 0V. In this case, the capacitor **122** is charged by the power supply pin VDD **102** via the transistor **142**. In this example, the transistor **142** is a diode-connected HEMT used as a rectifying diode, which naturally has a forward voltage (Vf). That is, the voltage at the node **184** will maximally be charged to 6V−Vf. In a first example, assuming the forward voltages and threshold voltages of all transistors in FIG. **1** are equal to 1.5V, the maximum voltage at the node **184** when the circuit **100** is turned off is 6V−1.5V=4.5V.

[0035] When the circuit **100** is turned on and the Vin has a voltage of 6V, the transistor **153** is turned on and the transistor **156** is turned off. The node **181** has the same voltage 0V as the ground Vss **111**, which enables the transistors **161**, **162**, **163** to be turned off. As such, the node **185** is electrically connected to the node **184**, and has a same voltage as the node **184**. This induces the transistor **165** to be turned on, which enables the node **186** to be charged by the voltage at the node **184**. This in turn induces the transistor **166** to be turned on, which enables the node **183** to be charged by the power supply pin VDD **102**. As such, the voltage at the node **183** can maximally be charged to 6V, same as the voltage of the power supply pin VDD **102**. Based on the 4.5V voltage difference stored by the capacitor **122** when the circuit **100** is off, the voltage at the node **184** can maximally be charged and increased to 6V+4.5V=10.5V, i.e. the voltage at the node **184** is boot-strapped to 10.5V. Accordingly, the node **185**, which is electrically connected to both the source and the gate of the transistor **164**, is charged to 10.5V as well.

[0036] While the node **186** is also charged by the voltage 10.5V at the node **184**, the voltage of the node **186** cannot reach 10.5V. Because the node **186** is electrically connected to the source of the transistor **165**, to keep the transistor **165** on, the gate source voltage difference Vgs of the transistor **165** must be larger than the threshold voltage (Vt) of the transistor **165**. As it is assumed Vt=1.5V in the first example, the maximum voltage the node **186** can reach in the first example when the circuit **100** is turned on is 10.5V−Vt=10.5V−1.5V=9V. As such, an enhancement-mode high-electron-mobility transistor (E-HEMT) pull-up device consumes at least one Vt voltage drop.

[0037] The node **182** is electrically connected to the node **181** and has a same voltage as that of the node **181**. That is, when the circuit **100** is turned off, the node **182** has the voltage 6V; when the circuit **100** is turned on, the node **182** has the voltage 0V. When the circuit **100** is turned off, the 6V voltage at the node **182** enables the transistors **171**, **172** to be turned on. As such, the node **187** is electrically connected to the ground Vss **111**, and has a voltage 0V. Here, the transistor **173** is turned off due to the 0V voltage at the node **186** when the circuit **100** is turned off as discussed above. Because the node **187** has the voltage 0V, the transistor **174** is turned off, and the node **188** is electrically connected to the ground Vss **111** and has a voltage 0V. In this case, the capacitor **123** is charged by the power supply pin VDD **103** via the transistor **143**. In this example, the transistor **143** is a diode-connected HEMT used as a rectifying diode, which naturally has a forward voltage (Vf). That is, the voltage at the node **189** will maximally be charged to 6V-Vf. In the first example, assuming the forward voltages and threshold voltages of all transistors in FIG. **1** are equal to 1.5V, the maximum voltage at the node **189** when the circuit **100** is turned off is 6V−1.5V=4.5V.

[0038] When the circuit **100** is turned on, the node **182**, like the node **181**, has the same voltage 0V as the ground Vss **111**, which enables the transistors **171**, **172** to be turned off. As discussed above, the node **186**, which is electrically connected to the gate of the transistor **173**, has a maximum voltage of 9V when the circuit **100** is turned on. As such, the transistor **173** is turned on and the node **187** is charged by the node **189**. This induces the transistor **174** to be turned on, which enables the node **188** to be charged by the power supply pin VDD **103**. As such, the voltage at the node **188** can maximally be charged to 6V, same as the voltage of the power supply pin VDD **102**. Based on the 4.5V voltage difference stored by the capacitor **123** when the circuit **100** is off, the voltage at the node **189** can maximally be charged and increased to 6V+4.5V=10.5V, i.e. the voltage at the node **189** is boot-strapped to 10.5V.

[0039] While the node **187** is charged by the voltage 10.5V at the node **189**, the voltage of the node **187** cannot reach 10.5V. Because the node **187** is electrically connected to the source of the transistor **173**, to keep the transistor **173** on, the gate source voltage difference Vgs of the transistor **173** must be larger than the threshold voltage (Vt) of the transistor **173**. The gate of the transistor **173** is electrically connected to the node **186**, which has a maximum voltage 9V when the circuit **100** is turned on. As it is assumed Vt=1.5V in the first example, the maximum voltage the node **187** can reach in the first example when the circuit **100** is turned on is 9V−Vt=9V−1.5V=7.5V. Now the transistor **174** has a gate source voltage difference Vgs=7.5V−6V=1.5V, which is exactly equal to the threshold voltage Vt=1.5V of the transistor **174**. This leaves no voltage margin at the last stage of the multi-stage boot-strapped driver. That is, in the first example where Vf=Vt=1.5V, there is not enough overdrive voltage to drive the power switch HEMT **175**. Even if the power switch HEMT **175** can be driven, it would be significantly slow as the current flowing through the transistor **174** and the node **188** would be very slow due to no Vgs margin compared to the Vt. The above conclusion has not even taken into consideration of the Vt variation (e.g. 3-σ variation of 0.5V), which typically exists in all process technologies. After counting the 3-σ variation of 0.5V, the circuit **100**, under the Vt=1.5V assumption, may not be able to drive the power switch HEMT **175** at all.

[0040] In a second example, it is assumed the forward voltages and threshold voltages of all transistors in FIG. **1** are equal to 1V. In this case, when the circuit **100** is turned off, the node **181** has the same voltage 6V, which enables the transistors **161**, **162**, **163** to be turned on. As such, the node **185** is electrically connected to the ground Vss **111** and has a voltage 0V. As such, the transistor **165** is turned off, and the node **186** is electrically connected to the ground Vss **111** and has a voltage 0V. Accordingly, the transistor **166** is turned off, and the node **183** is electrically connected to the ground Vss **111** and has a voltage 0V. The capacitor **122** is charged by the power supply pin VDD **102** via the transistor **142**. Because the transistor **142** is a diode-connected HEMT used as a rectifying diode which naturally has a forward voltage (Vf), the node **184** can have a maximum voltage of 6V−Vf=6V−1V=5V.

[0041] When the circuit **100** is turned on, the node **181** has the same voltage 0V as the ground Vss **111**, which enables the transistors **161**, **162**, **163** to be turned off. As such, the node **185** is electrically connected to the node **184**, and has a same voltage as the node **184**. This induces the transistor

165 to be turned on, which enables the node **186** to be charged by the voltage at the node **184**. This in turn induces the transistor **166** to be turned on, which enables the node **183** to be charged by the power supply pin VDD **102**. As such, the node **183** has a maximum voltage of 6V, same as the voltage of the power supply pin VDD **102**. Based on the 5V voltage difference stored by the capacitor **122** when the circuit **100** is off, the voltage at the node **184** can maximally be charged and increased to 6V+5V=11V, i.e. the voltage at the node **184** is boot-strapped to 11V. Accordingly, the node **185**, which is electrically connected to both the source and the gate of the transistor **164**, is charged to 11V as well. While the node **186** is also charged by the voltage 11V at the node **184**, the voltage of the node **186** cannot reach 11V. Because the node **186** is electrically connected to the source of the transistor **165**, to keep the transistor **165** on, the gate source voltage difference Vgs of the transistor **165** must be larger than the threshold voltage (Vt) of the transistor **165**. As it is assumed Vt=1V in the second example, the maximum voltage the node **186** can reach in the second example when the circuit **100** is turned on is 11V−Vt=11V−1V=10V.

[0042] The node **182** is electrically connected to the node **181** and has a same voltage as that of the node **181**. That is, when the circuit **100** is turned off, the node **182** has the voltage 6V; when the circuit **100** is turned on, the node **182** has the voltage 0V. When the circuit **100** is turned off, the 6V voltage at the node **182** enables the transistors **171**, **172** to be turned on. As such, the node **187** is electrically connected to the ground Vss **111**, and has a voltage 0V. Here, the transistor **173** is turned off due to the 0V voltage at the node **186** when the circuit **100** is turned off as discussed above. Because the node **187** has the voltage 0V, the transistor **174** is turned off, and the node **188** is electrically connected to the ground Vss **111** and has a voltage 0V. In this case, the capacitor **123** is charged by the power supply pin VDD **103** via the transistor **143**. Because the transistor **143** is a diode-connected HEMT used as a rectifying diode which naturally has a forward voltage (Vf), the node **189** has a maximum voltage of 6V−Vf=6V−1V=5V.

[0043] When the circuit **100** is turned on, the node **182**, like the node **181**, has the same voltage 0V as the ground Vss **111**, which enables the transistors **171**, **172** to be turned off. As discussed above, the node **186**, which is electrically connected to the gate of the transistor **173**, has a maximum voltage of 10V when the circuit **100** is turned on. As such, the transistor **173** is turned on and the node **187** is charged by the node **189**. This induces the transistor **174** to be turned on, which enables the node **188** to be charged by the power supply pin VDD **103**. As such, the voltage at the node **188** can maximally be charged to 6V, same as the voltage of the power supply pin VDD **102**. Based on the 5V voltage difference stored by the capacitor **123** when the circuit **100** is off, the voltage at the node **189** can maximally be charged and increased to 6V+5V=11V, i.e. the voltage at the node **189** is boot-strapped to 11V.

[0044] While the node **187** is charged by the voltage 11V at the node **189**, the voltage of the node **187** cannot reach 11V. Because the node **187** is electrically connected to the source of the transistor **173**, to keep the transistor **173** on, the gate source voltage difference Vgs of the transistor **173** must be larger than the threshold voltage (Vt) of the transistor **173**. The gate of the transistor **173** is electrically connected to the node **186**, which has a maximum voltage 10V when the circuit **100** is turned on. As it is assumed Vt=1V in the second example, the maximum voltage the node **187** can reach in the second example when the circuit **100** is turned on is 10V−Vt=10V−1V=9V. Now the transistor **174** has a gate source voltage difference Vgs=9V−6V=3V, which is much larger than the threshold voltage Vt=1V of the transistor **174**. This leaves enough voltage margin at the last stage of the multi-stage boot-strapped driver. That is, in the second example where Vf=Vt=1V, there is enough overdrive voltage to drive the power switch HEMT **175**. However, since all transistors, including the power switch HEMT **175**, in FIG. **1** are using a same Vt, a reduced Vt at the power switch HEMT **175** may cause the noise immunity of the output power switch **175** become significantly worse due to not being able to withstand a large back-feed-through impulse (di/dt) voltage to the gate of the output power switch **175**. Because there is inevitable parasitic capacitance between the drain and the gate of the power switch HEMT **175**, a voltage impulse will feed back from the drain of the power switch HEMT **175** to the gate of the power switch HEMT **175** through the parasitic capacitance. This could accidently turn on the power switch HEMT **175** so long as the noise voltage is larger than the reduced Vt of the power switch HEMT **175**, even when the circuit **100** is turned off.

[0045] As such, in a third example, the forward voltages and threshold voltages of all transistors in FIG. **1** are not all the same. In the third example, it is assumed that the transistors **142**, **143**, **165**, **166**, **173**, **174** have a smaller Vt of 1V, while the other transistors in FIG. **1** have a larger Vt of 1.5V. In this case, when the circuit **100** is turned off, the node **181** has the same voltage 6V, which enables the transistors **161**, **162**, **163** to be turned on. As such, the node **185** is electrically connected to the ground Vss **111** and has a voltage 0V. As such, the transistor **165** is turned off, and the node **186** is electrically connected to the ground Vss **111** and has a voltage 0V. Accordingly, the transistor **166** is turned off, and the node **183** is electrically connected to the ground Vss **111** and has a voltage 0V. The capacitor **122** is charged by the power supply pin VDD **102** via the transistor **142**. Because the transistor **142** has a forward voltage Vf equal to its Vt, the node **184** can have a maximum voltage of 6V−Vf=6V−1V=5V.

[0046] When the circuit **100** is turned on, the node **181** has the same voltage 0V as the ground Vss **111**, which enables the transistors **161**, **162**, **163** to be turned off. As such, the node **185** is electrically connected to the node **184**, and has a same voltage as the node **184**. This induces the transistor **165** to be turned on, which enables the node **186** to be charged by the voltage at the node **184**. This in turn induces the transistor **166** to be turned on, which enables the node **183** to be charged by the power supply pin VDD **102**. As such, the node **183** has a maximum voltage of 6V, same as the voltage of the power supply pin VDD **102**. Based on the 5V voltage difference stored by the capacitor **122** when the circuit **100** is off, the voltage at the node **184** can maximally be charged and increased to 6V+5V=11V, i.e. the voltage at the node **184** is boot-strapped to 11V. Accordingly, the node **185**, which is electrically connected to both the source and the gate of the transistor **164**, is charged to 11V as well. While the node **186** is also charged by the voltage 11V at the node **184**, the voltage of the node **186** cannot reach 11V. Because the node **186** is electrically connected to the source of the transistor **165**, to keep the transistor **165** on, the gate source voltage difference Vgs of the transistor **165** must be larger than the Vt=1V of the transistor **165**. So the maximum voltage the node **186** can reach in the third example when the circuit **100** is turned on is 11V−1V=10V.

[0047] The node **182** is electrically connected to the node **181** and has a same voltage as that of the node **181**. That is, when the circuit **100** is turned off, the node **182** has the voltage 6V; when the circuit **100** is turned on, the node **182** has the voltage 0V. When the circuit **100** is turned off, the 6V voltage at the node **182** enables the transistors **171**, **172** to be turned on. As such, the node **187** is electrically connected to the ground Vss **111**, and has a voltage 0V. Here, the transistor **173** is turned off due to the 0V voltage at the node **186** when the circuit **100** is turned off as discussed above. Because the node **187** has the voltage 0V, the transistor **174** is turned off, and the node **188** is electrically connected to the ground Vss **111** and has a voltage 0V. In this case, the capacitor **123** is charged by the power supply pin VDD **103** via the diode-connected transistor **143**. Because the diode-connected transistor **143** has a forward voltage Vf equal to its Vt, the node **189** has a maximum voltage of 6V−Vf=6V−1V=5V.

[0048] When the circuit **100** is turned on, the node **182**, like the node **181**, has the same voltage 0V as the ground Vss **111**, which enables the transistors **171**, **172** to be turned off. As discussed above, the node **186**, which is electrically connected to the gate of the transistor **173**, has a maximum voltage of 10V when the circuit **100** is turned on. As such, the transistor **173** is turned on and the node **187** is charged by the node **189**. This induces the transistor **174** to be turned on, which enables the node **188** to be charged by the power supply pin VDD **103**. As such, the voltage at the node **188** can maximally be charged to 6V, same as the voltage of the power supply pin VDD **102**. Based on the 5V voltage difference stored by the capacitor **123** when the circuit **100** is off, the voltage at the node **189** can maximally be charged and increased to 6V+5V=11V, i.e. the voltage at the node **189** is boot-strapped to 11V.

[0049] While the node **187** is charged by the voltage 11V at the node **189**, the voltage of the node **187** cannot reach 11V. Because the node **187** is electrically connected to the source of the transistor **173**, to keep the transistor **173** on, the gate source voltage difference Vgs of the transistor **173** must be larger than the threshold voltage Vt=1V of the transistor **173**. Because the gate of the transistor **173** is electrically connected to the node **186**, which has a maximum voltage 10V when the circuit **100** is turned on, the maximum voltage the node **187** can reach in the third example when the circuit **100** is turned on is 10V−Vt=10V−1V=9V. Now the transistor **174** has a gate source voltage difference Vgs=9V−6V=3V, which is much larger than the threshold voltage Vt=1V of the transistor **174**. This leaves enough voltage margin at the last stage of the multi-stage boot-strapped driver. That is, in the third example where the transistors **142**, **143**, **165**, **166**, **173**, **174** have a smaller Vt=1V, there is enough over-drive voltage to drive the power switch HEMT **175**. In addition, since all other transistors, including the power switch HEMT **175**, in FIG. **1** are having a larger Vt=1.5V, the noise immunity of the output power switch **175** will be better than the second example, because a larger Vt of the power switch HEMT **175** can significantly withstand impulse voltage noise fed back from the drain of the power switch HEMT **175** to the gate of the power switch HEMT **175**.

[0050] In various embodiments, the power switch HEMT **175** may have an even larger Vt like 2V. The disclosed circuit design for dual-Vt or multi-Vt transistors can reduce both Vt of the pull-up E-HEMT transistors and Vf of the diode-connected E-HEMT rectifiers of the multi-stage driver to provide enough over-drive voltage and dramatically reduce static current, without compromising the noise immunity of the output power switch. To use dual-Vt or multi-Vt transistors in a same IC, different metal gate materials can be used for different transistors formed on a same wafer. While a lower work-function material, e.g. tungsten (W) or titanium/tungsten/titanium-nitride (Ti/W/TiN) metal stack, can be used for implementing a high-Vt transistor; a higher work-function material, e.g. nickel (Ni) or titanium/nickel/titanium-nitride (Ti/Ni/TiN) metal stack, can be used for implementing a low-Vt transistor.

[0051] FIG. **2** illustrates a cross-sectional view of an exemplary semiconductor device **200** including dual threshold voltage transistors, in accordance with some embodiments of the present disclosure. As shown in FIG. **2**, the semiconductor device **200** in this example includes a silicon layer **210** and a transition layer **220** disposed on the silicon layer **210**. The semiconductor device **200** further includes a first layer **230** comprising a first III-V semiconductor material formed over the transition layer **220**.

[0052] The semiconductor device **200** further includes a second layer **240** (a polarization layer) comprising a second III-V semiconductor material disposed on the first layer **230**. The second III-V semiconductor material is different from the first III-V semiconductor material. For example, the first III-V semiconductor material may be gallium nitride (GaN); while the second III-V semiconductor material may be aluminum gallium nitride (AlGaN).

[0053] As shown in FIG. **2**, the semiconductor device **200** further includes a first transistor **201** and a second transistor **202** formed over the first layer **230**. The first transistor **201** comprises a first gate structure **251** comprising a first material, a first source region **281** and a first drain region **291**. The second transistor **202** comprises a second gate structure **252** comprising a second material, a second source region **282** and a second drain region **292**. According to various embodiments, the first material is different from the second material.

[0054] The semiconductor device **200** further includes a polarization modulation layer **241**, **242** disposed on the second layer **240**, and a passivation layer **250** disposed partially on the polarization modulation layer and partially on the second layer **240**. In one embodiment, the polarization modulation layer comprises p-type doped GaN (pGaN).

[0055] The sources **281**, **282** and the drains **291**, **292** of the two transistors **201**, **202** are formed through the second layer **240** and the passivation layer **250**, and disposed on the first layer **230**. The first gate structure **251** is disposed on the pGaN portion **241** and between the first source region **281** and the first drain region **291**. The second gate structure **252** is disposed on the pGaN portion **242** and between the second source region **282** and the second drain region **292**.

[0056] In one embodiment, the first transistor **201** and the second transistor **202** are high electron mobility transistors to be used in a same multi-stage driver circuit. For example, the first transistor **201** is used as a power switch transistor and has a first threshold voltage. The second transistor **202** is used as a driver transistor and has a second threshold voltage that is lower than the first threshold voltage. Accordingly, the first material of the first gate structure **251** has a lower work-function than the second material of the second gate structure **252**. For example, the first material comprises tungsten (W) and/or a titanium/tungsten/titanium-nitride (Ti/W/TiN) metal stack; and the second material comprises nickel (Ni) and/or a titanium/nickel/titanium-nitride (Ti/Ni/TiN) metal stack.

[0057] In addition, the semiconductor device **200** includes an interlayer dielectric (ILD) layer **260** disposed partially on the passivation layer **250** and partially on the first transistor **201** and the second transistor **202**. The semiconductor device **200** also includes metal contacts **271** disposed on and in contact with the sources **281**, **282** and the drains **291**, **292** respectively, and includes a first metal layer **272** on the metal contacts **271**.

[0058] FIGS. **3**A, **3**B, **3**C, **3**D, **3**E, **3**F, **3**G, **3**H, **3**I, **3**J, **3**K, **3**L, **3**M, **3**N and **3**O illustrate cross-sectional views of an exemplary semiconductor device during various fabrication stages, in accordance with some embodiments of the present disclosure. In some embodiments, the semiconductor device may be included in an integrated circuit (IC). In addition, FIGS. **3**A through **3**O are simplified for a better understanding of the concepts of the present disclosure. For example, although the figures illustrate two transistors, it is understood the semiconductor device may include more than two transistors, and the IC may include a number of other devices comprising resistors, capacitors, inductors, fuses, etc., which are not shown in FIGS. **3**A through **3**O, for purposes of clarity of illustration.

[0059] FIG. **3**A is a cross-sectional view of the semiconductor device including a substrate **310**, which is provided at one of the various stages of fabrication, according to some embodiments of the present disclosure. The substrate **310** may be formed of silicon, as shown in FIG. **3**A, or another semiconductor material.

[0060] FIG. **3**B is a cross-sectional view of the semiconductor device including a transition or buffer layer **320**, which is formed on the substrate **310** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The transition or buffer layer **320** may be formed by epitaxial growth. According to various embodiments, the transition or buffer layer **320** includes a nucleation layer of aluminum nitride (AlN) and serves as a buffer to reduce the stress between the substrate **310** and the layer on top of the transition or buffer layer **320**. In one embodiment, the transition or buffer layer **320** and the operation step shown in FIG. **3**B is optional and can be removed.

[0061] FIG. **3**C is a cross-sectional view of the semiconductor device including a first III-V semiconductor material layer **330**, which is formed optionally on the transition or buffer layer **320** or directly on the substrate **310** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The first III-V semiconductor material layer **330** may be formed by epitaxial growth. According to various embodiments, the first III-V semiconductor material layer **330** includes a gallium nitride (GaN). When the first III-V semiconductor material layer **330** is formed on the transition or buffer layer **320**, the transition or buffer layer **320** can reduce the stress between the substrate **310** and the first III-V semiconductor material layer **330**. After transistors are formed over the first III-V semiconductor material layer **330**, the first III-V semiconductor material layer **330** serves as a channel layer for the transistors.

[0062] FIG. **3**D is a cross-sectional view of the semiconductor device including a second III-V semiconductor material layer **340**, which is formed on the first III-V semiconductor material layer **330** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The second III-V semiconductor material layer **340** may be formed by epitaxial growth. According to various embodiments, the second III-V semiconductor material layer **340** includes an aluminum gallium nitride (AlGaN). After transistors are formed over the first III-V semiconductor material layer **330** and the second III-V semiconductor material layer **340**, a 2-dimensional electron gas (2-DEG) will be formed at the interface between the first III-V semiconductor material layer **330** and the second III-V semiconductor material layer **340**.

[0063] FIG. **3**E is a cross-sectional view of the semiconductor device including a p-type doped GaN (pGaN) layer **341**, **342**, which is formed on the second III-V semiconductor material layer **340** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The pGaN layer **341**, **342** is patterned to form island regions shown in FIG. **3**E. The patterning of the pGaN layer includes, e.g., (i) forming a masking layer (e.g., photoresist, etc.) over the pGaN layer, the masking layer including openings over the portions of the pGaN layer that are to be removed, and (ii) removing the portions of the pGaN layer that are left exposed by the masking layer (e.g., via a wet or dry etch procedure). The pGaN layer **341**, **342** may be called a polarization modulation layer, which modulates the dipole concentration in the AlGaN layer **340** as result in changing the 2-DEG concentration in the AlGaN/GaN interface channel. While the polarization modulation layer is formed for an enhancement-mode (normally off) AlGaN/GaN HEMT, the polarization modulation layer is not needed in a depletion-mode (normally on) AlGaN/GaN HEMT.

[0064] FIG. **3**F is a cross-sectional view of the semiconductor device including a passivation layer **350**, which is formed on the second III-V semiconductor material layer **340** and on the polarization modulation layer at one of the various stages of fabrication, according to some embodiments of the present disclosure. The passivation layer **350** is formed over the AlGaN layer **340** and over the remaining portions of the polarization modulation layer **341**, **342**. According to various embodiments, the passivation layer **350** is formed using a deposition procedure (e.g., chemical deposition, physical deposition, etc.). The passivation layer **350** may comprise silicon oxide, silicon nitride, silicon oxynitride, carbon doped silicon oxide, carbon doped silicon nitride, carbon doped silicon oxynitride, zinc oxide, zirconium oxide, hafnium oxide, titanium oxide, or another suitable material. In one embodiment, after depositing the passivation layer **350**, the passivation layer **350** undergoes a polishing and/or etching procedure. The polishing and/or etching procedure includes, e.g. a chemical-mechanical planarization (CMP) (i.e., chemical-mechanical polishing) process that is used to polish the surface of the passivation layer **350** and remove topographical irregularities.

[0065] FIG. **3**G is a cross-sectional view of the semiconductor device including source and drain contacts **381**, **391**, **382**, **392**, which are formed through the second III-V semiconductor material layer **340** and the passivation layer **350** and disposed on the first III-V semiconductor material layer **330** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The source and drain contacts may be formed as non-rectifying electrical junctions, i.e. ohmic contacts.

[0066] FIG. 3H is a cross-sectional view of the semiconductor device including a mask **355**, which is formed on the passivation layer **350** at one of the various stages of fabrication, according to some embodiments of the present disclosure. At this stage, the mask **355** has a pattern to expose a portion of the passivation layer **350** on top of the pGaN portion **341** between the first pair of source **381** and drain **391**. As such, a first opening **357** is formed on the pGaN portion **341** by etching the passivation layer **350** with the patterned mask **355**.

[0067] FIG. 3I is a cross-sectional view of the semiconductor device including a first gate **351**, which is deposited and polished in the first opening **357** between the first source **381** and the first drain **391** at one of the various stages of fabrication, according to some embodiments of the present disclosure. According to various embodiments, the first gate **351** may be formed of different metal materials with different work functions. As the work-function of the material in the first gate **351** decreases, the threshold voltage Vt of the first transistor formed of the first gate **351**, the first source **381** and the first drain **391** will increase. As the work-function of the material in the first gate **351** increases, the threshold voltage Vt of the first transistor formed of the first gate **351**, the first source **381** and the first drain **391** will decrease.

[0068] FIG. 3J is a cross-sectional view of the semiconductor device including a patterned mask **355**, which is formed on the passivation layer **350** at one of the various stages of fabrication, according to some embodiments of the present disclosure. At this stage, the patterned mask **355** has a pattern to expose a portion of the passivation layer **350** on top of the pGaN portion **342** between the second pair of source **382** and drain **392**. As such, a second opening **358** is formed on the pGaN portion **342** by etching the passivation layer **350** with the patterned mask **355**.

[0069] FIG. 3K is a cross-sectional view of the semiconductor device including a second gate **352**, which is deposited and polished in the second opening **358** between the second source **382** and the second drain **392** at one of the various stages of fabrication, according to some embodiments of the present disclosure. According to various embodiments, the second gate **352** may be formed of different metal materials with different work functions. In particular, the material of the second gate **352** may have a different work function compared to the material of the first gate **351**. For example, when the material of the second gate **352** has a larger work function compared to the material of the first gate **351**, the second transistor formed of the second gate **352**, the second source **382** and the second drain **392** will have a lower threshold voltage Vt compared to the first transistor formed of the first gate **351**, the first source **381** and the first drain **391**. That is, the two transistors formed on a same substrate have different threshold voltages and can be used as HEMTs in a same IC as shown in FIG. **1**.

[0070] FIG. 3L is a cross-sectional view of the semiconductor device, where the mask **355** is removed from the passivation layer **350** after the metal gates are formed, at one of the various stages of fabrication, according to some embodiments of the present disclosure. After the mask **355** is removed, each of the source regions **381**, **382**, the drain regions **391**, **392**, and the gate structures **351**, **352** has an exposed portion on top of the passivation layer **350**.

[0071] FIG. 3M is a cross-sectional view of the semiconductor device including an interlayer dielectric (ILD) layer **360**, which is formed on the passivation layer **350**, at one of the various stages of fabrication, according to some embodiments of the present disclosure. The ILD layer **360** covers the passivation layer **350** and the exposed portions of the source regions **381**, **382**, the drain regions **391**, **392**, and the gate structures **351**, **352** that are formed at the stage shown in FIG. 3L. The ILD layer **360** is formed of a dielectric material and may be patterned with holes for metal interconnects or contacts for the source and drain contacts **381**, **382**, **391**, **392** as well as the gate structures **351**, **352**.

[0072] FIG. 3N is a cross-sectional view of the semiconductor device including metal contacts **371**, each of which is formed on a source or drain contact, at one of the various stages of fabrication, according to some embodiments of the present disclosure. As discussed above, the ILD layer **360** is patterned with holes each of which is on one of the source and drain contacts **381**, **382**, **391**, **392**. As such, the metal contacts **371** can be formed in these holes to be in contact with the source and drain contacts **381**, **382**, **391**, **392**, respectively.

[0073] FIG. 3O is a cross-sectional view of the semiconductor device including a first metal layer **372**, which is formed on the metal contacts **371**, at one of the various stages of fabrication, according to some embodiments of the present disclosure. The first metal layer **372** includes metal material and is formed over the ILD layer **360** and in contact with the metal contacts **371**.

[0074] FIG. **4**A and FIG. **4**B show a flow chart illustrating an exemplary method **400** for forming a semiconductor device including dual threshold voltage transistors, in accordance with some embodiments of the present disclosure. As shown in FIG. **4**A, at operation **402**, a transition/buffer layer is formed on a semiconductor substrate by epitaxial growth. A GaN layer is formed at operation **404** on the transition/buffer layer by epitaxial growth. At operation **406**, an AlGaN layer is formed on the GaN layer by epitaxial growth. At operation **408**, a p-type doped GaN layer is deposited and defined on the AlGaN layer. At operation **410**, a passivation layer is deposited and polished on the p-type doped GaN layer and the AlGaN layer. Source and drain ohmic contacts are formed at operation **412** through the passivation layer and the AlGaN layer. At operation **414**, a first opening is defined for a first gate on the p-type doped GaN layer by etching with a mask. The process then goes to the operation **416** in FIG. **4**B.

[0075] As shown in FIG. **4**B, at operation **416**, the first gate material is deposited and polished in the first opening. A second opening is defined at operation **418** for a second gate on the p-type doped GaN layer by etching with the mask. At operation **420**, the second gate material is deposited and polished in the second opening. At operation **422**, the mask on the passivation layer is removed. At operation **424**, a dielectric layer is deposited and polished on the sources, drains, gates and the passivation layer. Metal contacts are formed and defined at operation **426** on the sources, drains and gates. At operation **428**, a first metal layer is formed and defined on the dielectric layer and the metal contacts. The order of the operations shown in FIG. **4**A and FIG. **4**B may be changed according to different embodiments of the present disclosure.

[0076] In an embodiment, a semiconductor structure is disclosed. The semiconductor structure includes: a substrate; a first layer comprising a first III-V semiconductor material formed over the substrate; a first transistor formed over the first layer, and a second transistor formed over the first layer. The first transistor comprises a first gate structure comprising a first material, a first source region and a first drain region. The second transistor comprises a second gate structure comprising a second material, a second source region and a second drain region. The first material is different from the second material.

[0077] In another embodiment, a circuit is disclosed. The circuit includes a first transistor including a first gate, a first source and a first drain; and a second transistor including a second gate, a second source and a second drain. The first transistor and the second transistor are formed on a same semiconductor wafer. The second gate is made of a material that is different from that of the first gate.

[0078] In yet another embodiment, a method for forming a semiconductor structure is disclosed. The method includes: forming a first layer comprising a first III-V semiconductor material over a semiconductor substrate; forming a first transistor over the first layer, wherein the first transistor comprises a first gate structure comprising a first material, a first source region and a first drain region; and forming a second transistor over the first layer, wherein the second transistor comprises a second gate structure comprising a second material, a second source region and a second drain region, wherein the first material is different from the second material.

[0079] The foregoing outlines features of several embodiments so that those ordinary skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor structure, comprising:
a substrate;
a first layer comprising a first III-V semiconductor material formed over the substrate;
a first transistor formed over the first layer, wherein the first transistor comprises a first gate structure comprising a first material, a first source region and a first drain region; and
a second transistor formed over the first layer, wherein the second transistor comprises a second gate structure comprising a second material, a second source region and a second drain region, wherein the first material is different from the second material.

2. The semiconductor structure of claim **1**, wherein:
the first transistor and the second transistor are high electron mobility transistors to be used in a same multi-stage driver circuit.

3. The semiconductor structure of claim **1**, wherein:
the first transistor has a first threshold voltage; and
the second transistor has a second threshold voltage that is lower than the first threshold voltage.

4. The semiconductor structure of claim **3**, wherein:
the first material has a lower work-function than the second material.

5. The semiconductor structure of claim **4**, wherein:
the first material comprises at least one of: tungsten (W) and titanium/tungsten/titanium-nitride (Ti/W/TiN) metal stack; and
the second material comprises at least one of: nickel (Ni) and titanium/nickel/titanium-nitride (Ti/Ni/TiN) metal stack.

6. The semiconductor structure of claim **1**, further comprising a second layer comprising a second III-V semiconductor material disposed on the first layer, wherein:
the second III-V semiconductor material is different from the first III-V semiconductor material;
the first gate structure is formed over the second III-V semiconductor material and between the first source region and the first drain region; and
the second gate structure is formed over the second III-V semiconductor material and between the second source region and the second drain region.

7. The semiconductor structure of claim **6**, wherein:
the first semiconductor material comprises gallium nitride (GaN); and
the second III-V semiconductor material comprises aluminum gallium nitride (AlGaN).

8. The semiconductor structure of claim **6**, further comprising a polarization modulation layer disposed on the second layer, wherein:
the polarization modulation layer comprises p-type doped GaN; and
the first gate structure and the second gate structure are disposed on the polarization modulation layer.

9. A circuit, comprising:
a first transistor including a first gate, a first source and a first drain; and
a second transistor including a second gate, a second source and a second drain, wherein:
the first transistor and the second transistor are formed on a same semiconductor wafer, and
the second gate is made of a material that is different from that of the first gate.

10. The circuit of claim **9**, wherein:
the first transistor has a first threshold voltage; and
the second transistor has a second threshold voltage that is different from the first threshold voltage.

11. The circuit of claim **9**, wherein:
at least one of the first source and the first drain is electrically connected to a ground voltage; and
at least one of the second source and the second drain is electrically connected to a positive power supply voltage.

12. The circuit of claim **11**, wherein:
the first threshold voltage is higher than the second threshold voltage.

13. The circuit of claim **12**, wherein:
the first gate is made of a first material;
the second gate is made of a second material; and
the first material has a lower work-function than the second material.

14. The circuit of claim **12**, wherein:
at least one of the first source and the first drain is electrically connected to an output pin of the circuit.

15. The circuit of claim **12**, wherein the first transistor is at least one of:
a high voltage enhancement-mode high electron mobility transistor (HV E-HEMT);

a low voltage enhancement-mode high electron mobility transistor (LV E-HEMT); and

a low voltage depletion-mode high electron mobility transistor (LV D-HEMT).

16. The circuit of claim **12**, wherein the second transistor is a low voltage enhancement-mode high electron mobility transistor (LV E-HEMT).

17. The circuit of claim **9**, wherein the first gate is physically coupled to the second source.

18. A method for forming a semiconductor structure, comprising:

forming a first layer comprising a first III-V semiconductor material over a semiconductor substrate;

forming a first transistor over the first layer, wherein the first transistor comprises a first gate structure comprising a first material, a first source region and a first drain region; and

forming a second transistor over the first layer, wherein the second transistor comprises a second gate structure comprising a second material, a second source region and a second drain region, wherein the first material is different from the second material.

19. The method of claim **18**, wherein:

the first transistor and the second transistor are high electron mobility transistors to be used in a same multi-stage driver circuit;

the first transistor has a first threshold voltage;

the second transistor has a second threshold voltage that is lower than the first threshold voltage; and

the first material has a lower work-function than the second material.

20. The method of claim **18**, further comprising disposing a second layer comprising a second III-V semiconductor material on the first layer, wherein:

the first III-V semiconductor material comprises gallium nitride (GaN);

the second III-V semiconductor material comprises aluminum gallium nitride (AlGaN);

the first gate structure is formed over the second III-V semiconductor material and between the first source region and the first drain region; and

the second gate structure is formed over the second III-V semiconductor material and between the second source region and the second drain region.

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