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(54) **ELECTRONIC CIRCUIT COMPRISING DIODES**

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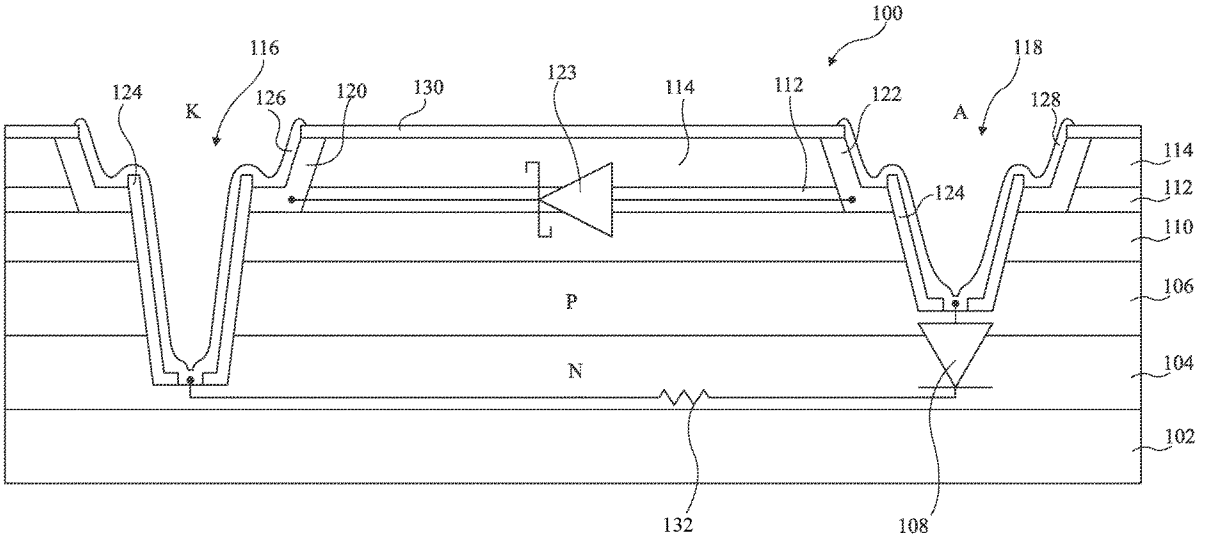
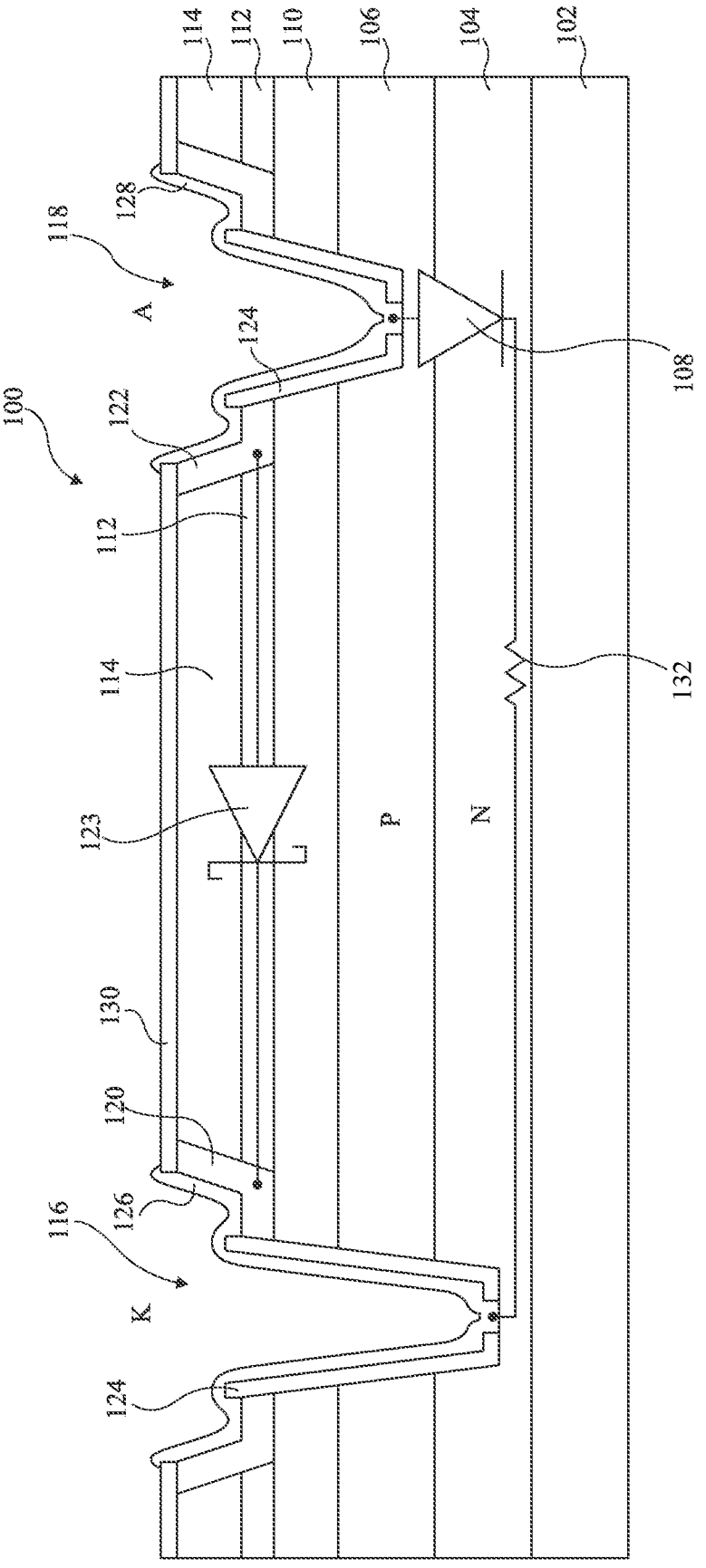
(57) **ABSTRACT**

The present description concerns an electronic device comprising a stack of a Schottky diode and of a bipolar diode, connected in parallel by a first electrode located in a first cavity and a second electrode located in a second cavity.




114
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K
124

Fig 1

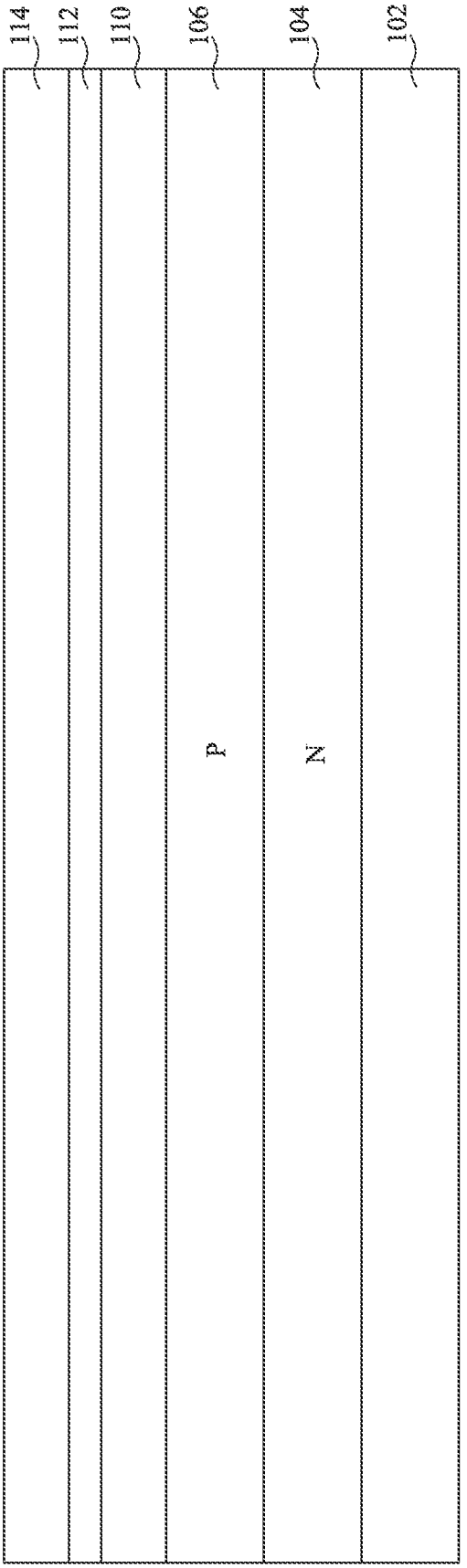


Fig 2

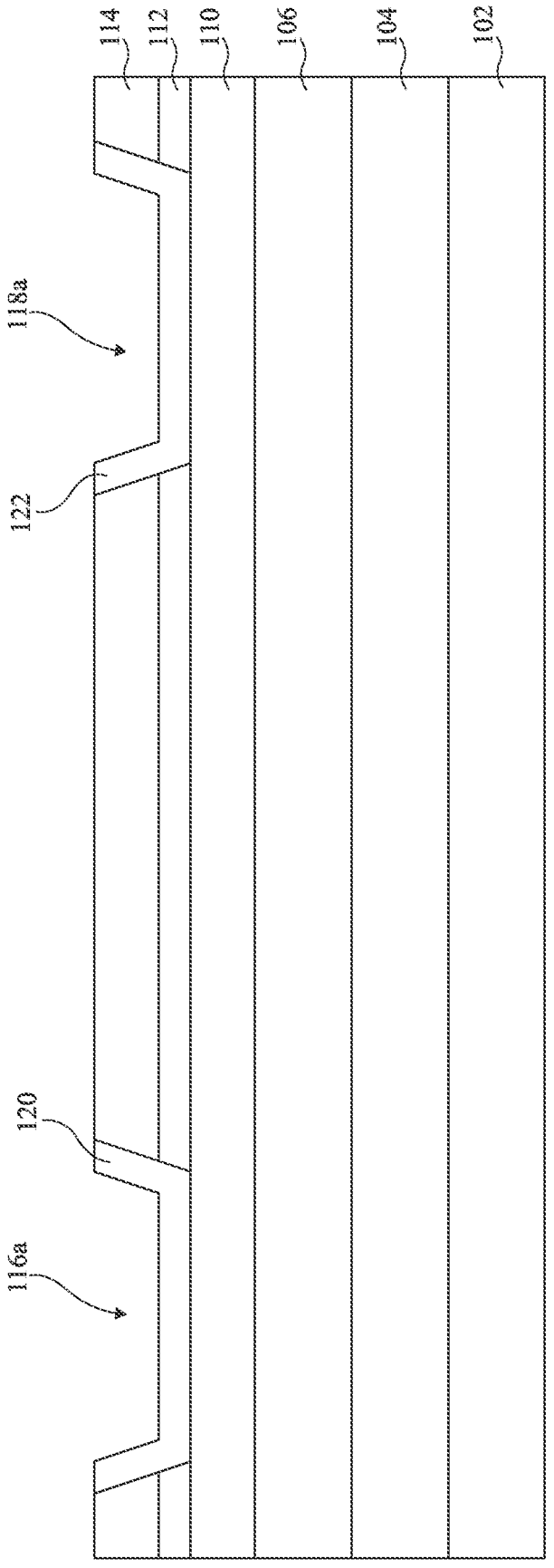


Fig 3

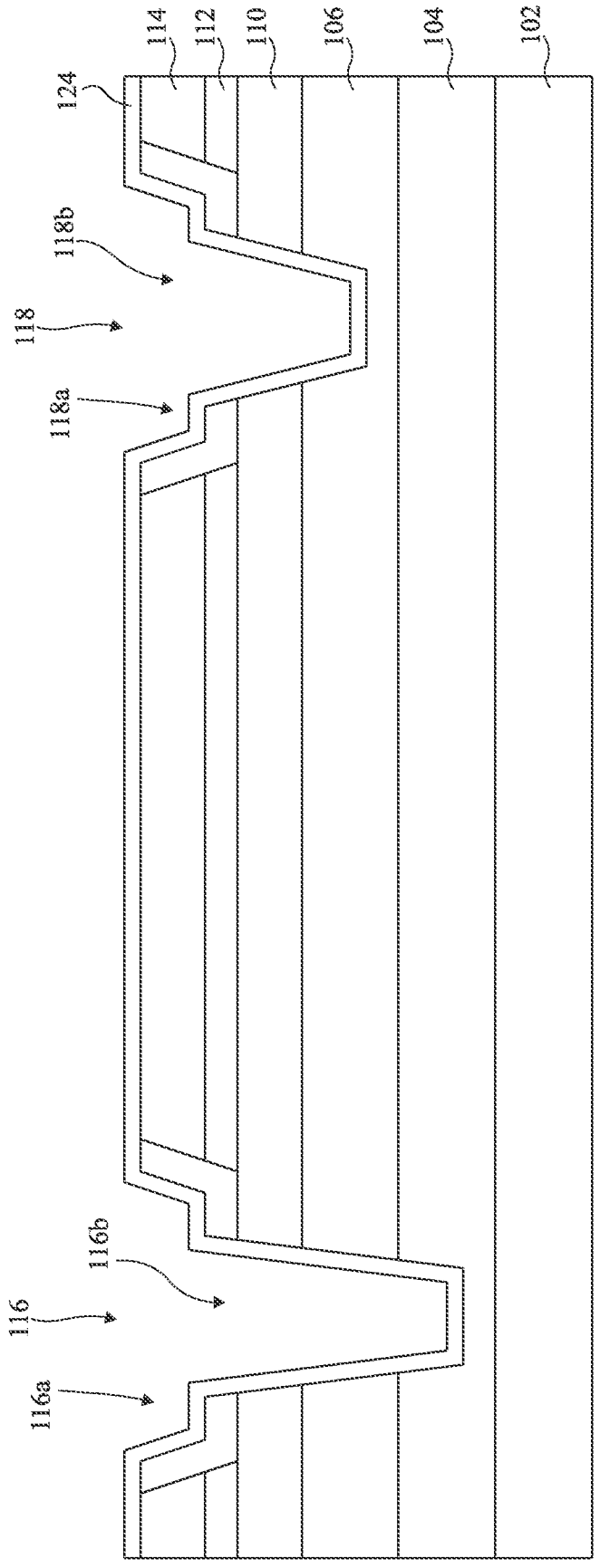


Fig 4

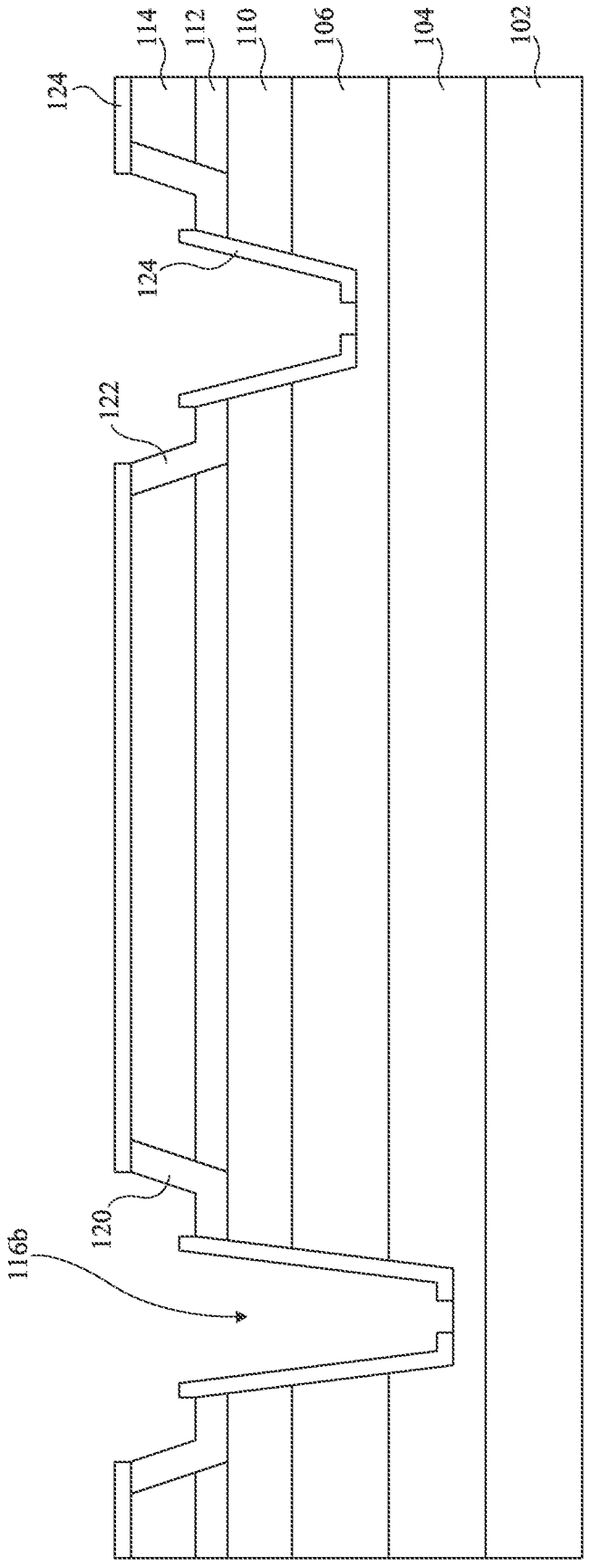


Fig 5

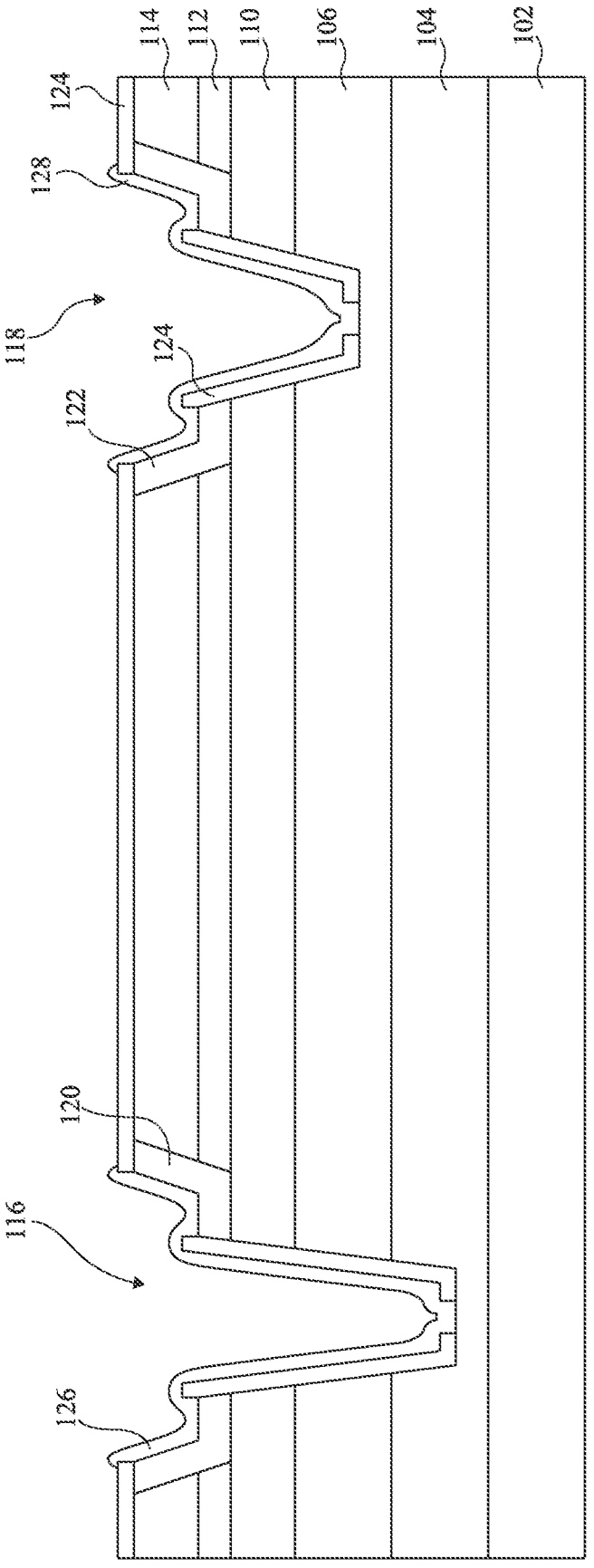
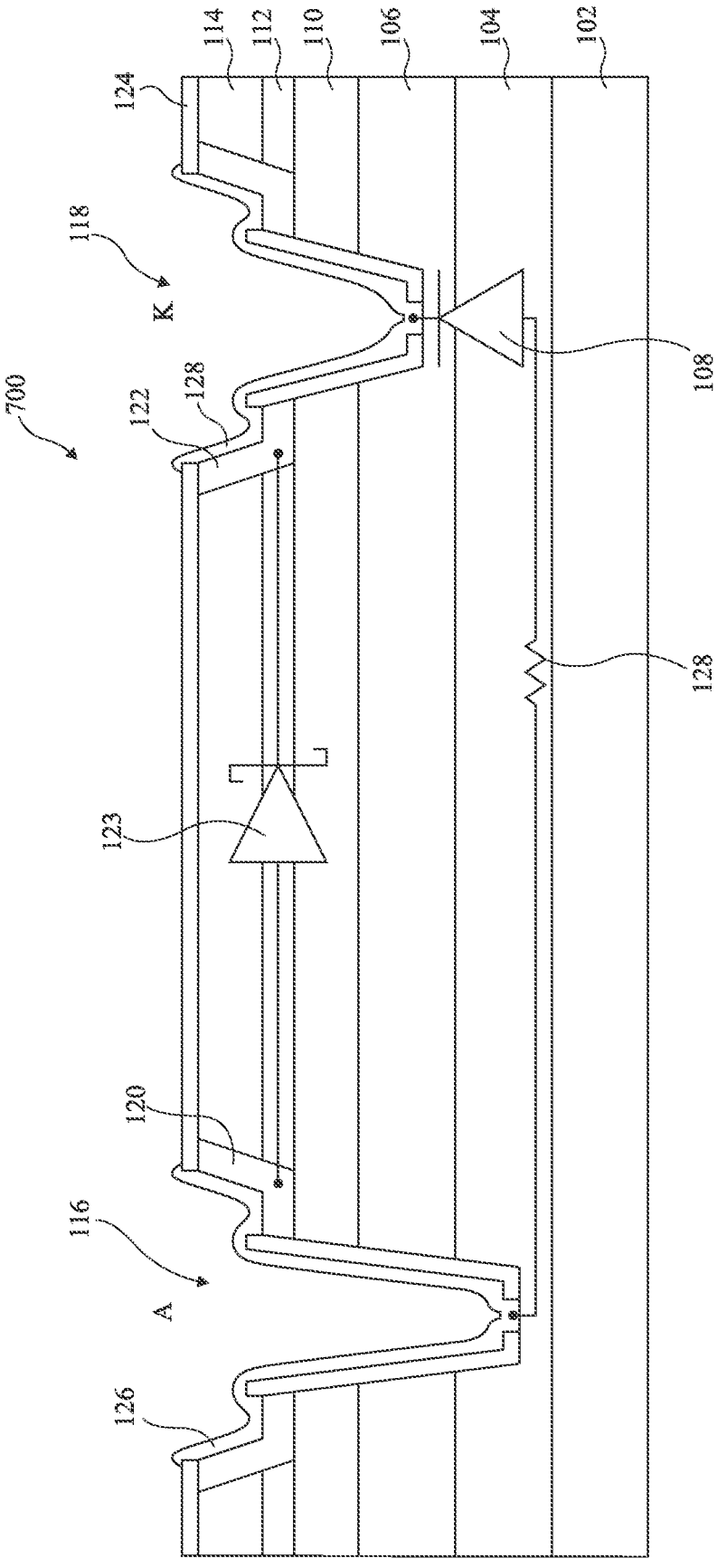


Fig 6


114
112
110
106
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102
124
118
K
700
122
128
108
128
123
120
116
A
126

Fig 7

ELECTRONIC CIRCUIT COMPRISING DIODES

BACKGROUND

Technical Field

[0001] The present disclosure generally relates to electronic circuits and, more specifically, to electronic circuits comprising diodes.

Description of the Related Art

[0002] Schottky diodes are diodes formed of a metal/semiconductor junction. Such diodes have the advantage over so-called bipolar diodes of being fast and of having a relatively low forward voltage drop. However, they are not able to withstand overcharges as well as bipolar diodes.

BRIEF SUMMARY

[0003] Applicant has found that it is advantageous to connect in parallel a bipolar diode and a Schottky diode.

[0004] An embodiment provides an electronic device comprising a stack of a Schottky diode and of a bipolar diode, connected in parallel by a first electrode located in a first cavity and a second electrode located in a second cavity.

[0005] According to an embodiment, the stack comprises first, second, and third semiconductor layers.

[0006] According to an embodiment, the bipolar diode comprises the first semiconductor layer in contact with the second semiconductor layer, the second layer being of the conductivity type opposite to that of the first layer.

[0007] According to an embodiment, the first cavity reaches the first semiconductor layer and the second cavity reaches the second semiconductor layer.

[0008] According to an embodiment, the first and second semiconductor layers are made of gallium nitride.

[0009] According to an embodiment, the Schottky diode comprises the third semiconductor layer in contact with the first and second electrodes, the material of a portion of one of these electrodes being capable of forming the Schottky diode.

[0010] According to an embodiment, the third semiconductor layer is made of AlGaN.

[0011] According to an embodiment, one of the first and second electrodes is the cathode electrode of the Schottky diode and of the bipolar diode and the other one of the first and second electrodes is the anode electrode of the Schottky diode and of the bipolar diode.

[0012] Another embodiment provides a method of manufacturing an electronic device comprising a stack of a Schottky diode and of a bipolar diode, comprising a step of forming first and second cavities having first and second electrodes connecting in parallel the Schottky diode and the bipolar diode located therein.

[0013] According to an embodiment, the method comprises:

[0014] forming first and second semiconductor layers of the bipolar diode and a third semiconductor layer of the Schottky diode;

[0015] forming first and second cavities; and

[0016] forming first and second electrodes in the cavities to connect the Schottky diode and the bipolar diode in parallel.

[0017] According to an embodiment, the first cavity reaches the first semiconductor layer and the second cavity reaches the second semiconductor layer.

[0018] According to an embodiment, the method comprises depositing an insulating layer on the walls and the bottom of the first and second cavities.

[0019] According to an embodiment, the method comprises, before the forming of the first and second cavities, forming first and second intermediate cavities reaching the lower surface of the third semiconductor layer, the rest of the first and second cavities being formed afterwards from the bottom of the first and second intermediate cavities.

[0020] According to an embodiment, the method comprises forming a first conductive layer on the walls and the bottom of each of the first and second intermediate cavities.

[0021] According to an embodiment, the method comprises removing the insulating layer from at least a portion of the bottom of the first and second cavities and from the first conductive layers.

[0022] According to an embodiment, the method comprises forming a second conductive layer in each of the first and second cavities, to connect, in the first cavity, the first semiconductor layer to the first conductive layer of the first intermediate cavity and, in the second cavity, the second semiconductor layer to the first conductive layer of the second intermediate cavity.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0023] The foregoing and other features and advantages will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings, in which:

[0024] FIG. **1** schematically shows an embodiment of a Schottky diode and of a bipolar diode in parallel;

[0025] FIG. **2** schematically shows the result of a step of manufacturing of the embodiment of FIG. **1**;

[0026] FIG. **3** schematically shows the result of another step of manufacturing of the embodiment of FIG. **1**;

[0027] FIG. **4** schematically shows the result of another step of manufacturing of the embodiment of FIG. **1**;

[0028] FIG. **5** schematically shows the result of another step of manufacturing of the embodiment of FIG. **1**;

[0029] FIG. **6** schematically shows the result of another step of manufacturing of the embodiment of FIG. **1**; and

[0030] FIG. **7** schematically shows another embodiment of a Schottky diode and a bipolar diode in parallel.

DETAILED DESCRIPTION

[0031] The same elements have been designated with the same reference numerals in the different drawings. In particular, the structural and/or functional elements common to the different embodiments may be designated with the same reference numerals and may have identical structural, dimensional, and material properties.

[0032] For clarity, only those steps and elements which are useful to the understanding of the described embodiments have been shown and are detailed.

[0033] Throughout the present disclosure, the term "connected" is used to designate a direct connection between circuit elements, whereas the term "coupled" is used to designate a connection between circuit elements that may be direct, or may be via one or more intermediate elements.

Unless indicated otherwise, when the term "coupled" is used, the connection can be implemented by a direct connection.

[0034] In the following description, when reference is made of qualifiers of absolute positions, such as terms "front", "back", "top", "bottom", "left-hand", "right-hand", etc., or relative positions, such as terms "above", "under", "upper", "lower", etc., or to qualifiers of orientation, such as terms "horizontal", "vertical", etc., reference is made, unless otherwise specified, to the orientation of the considered elements in the drawings.

[0035] The terms "approximately", "substantially", and "in the order of" are used herein to designate a tolerance of plus or minus 10%, preferably of plus or minus 5%, of the value in question.

[0036] FIG. **1** schematically and partially shows an embodiment of a device **100** comprising a Schottky diode and a bipolar diode. FIG. **1** also partially shows an equivalent diagram of device **100**.

[0037] Device **100** comprises a stack of semiconductor layers. The stack comprises a layer **102**, for example, made of aluminum gallium nitride (AlGaN), located on a substrate, not shown. Layer **102** is covered with an N-type gallium nitride layer **104** and with a P-type gallium nitride layer **106**. Layer **106** is for example doped with magnesium. Layer **108** is for example doped with silicon or germanium. Layers **104** and **106** form a PN junction which forms a bipolar diode **108**. More specifically, layer **104** forms the cathode of bipolar diode **108** and layer **106** forms the anode of diode **108**. Layer **106** is covered with a layer **110**, for example, made of gallium nitride. Layer **110** is covered with a layer **112**, for example, made of AlGaN and with a passivation layer **114**, for example, made of silicon nitride or of gallium nitride.

[0038] Device **100** further comprises cavities **116** and **118** extending in the stack. Cavities **116** and **118** comprise an upper portion and a lower portion. The upper portion of each cavity **116** or **118** stops substantially at the level of the lower surface of layer **112**. The lower portion of cavity **116** extends through layers **110** and **106** and stops in layer **104**. The lower portion of cavity **118** extends through layer **110** and stops in layer **106**. The opening of the upper portion for example has dimensions greater than the dimensions of the opening of the lower portion. The walls and the bottom of the upper portion of cavities **116** and **118** are covered with a conductive layer **120** or **122**. The layer **120** or **122** of each cavity **116** or **118** is in contact with semiconductor layer **112**. The material of layer **122** of cavity **118** is a metal selected to form a Schottky diode **123** between layer **122** and layer **112**. Layer **122** thus forms the anode of Schottky diode **123**. Layer **120** is an ohmic electrode in contact with layer **112** and forming the cathode of Schottky diode **123**. Cavities **116** and **118** cross layer **112**, and thus Schottky diode **123**.

[0039] The walls of the lower portions of cavities **116** and **118** are covered with an insulating layer **124**. The bottom of the lower portions of cavities **116** and **118** are partially covered with layer **124**. A portion of the bottom of the lower portion of each cavity **116** or **118** is thus exposed. A conductive layer **126** covers the walls and the bottom of cavity **116** and a conductive layer **128** covers the walls and the bottom of cavity **118**. Layer **126** thus forms an electric connection between layer **104**, through the bottom of cavity **116** and electrode **120**. Conductive layer **128** forms an electric connection between layer **106**, through the bottom of cavity **118**, and electrode **122**. Thus, the anodes (A) of diodes **108** and **123** are connected together at the level of cavity **118** and the cathodes (K) of diodes **108** and **123** are connected together at the level of cavity **116**.

[0040] Device **100** further comprises an insulating layer **130** covering layer **114** around cavities **116** and **118** as well as the portion of conductive layers **120** and **122** located in the same plane as the upper surface of layer **114**.

[0041] Cavities **116***a* and **118***a* are for example separated by a distance in the range from approximately 10 μm to approximately 25 μm. The distance between the bottom of cavity **116** and the bottom of cavity **118** may cause the presence of a resistor **132** in series with diode **108**.

[0042] FIG. **2** schematically shows the result of a step of manufacturing of the embodiment of FIG. **1**. During this step, the stack of layers is formed on the substrate, not shown. More specifically, the following are successively formed:

[0043] layer **102**, for example, made of AlGaN, on the substrate, not shown;

[0044] layer **104**, made of gallium nitride, on layer **102**;

[0045] layer **106**, made of gallium nitride, on layer **104**, of type P, formed by epitaxy and having a thickness in the range from approximately 50 to approximately 400 nm, preferably, approximately 200 nm;

[0046] layer **110**, for example, made of gallium nitride, having a thickness in the range from approximately 50 to approximately 400 nm, preferably approximately 100 nm;

[0047] layer **112**, for example, made of AlGaN, having a thickness in the range from 10 to 30 nm, preferably approximately 24 nm;

[0048] passivation layer **114**, for example, made of silicon nitride or of gallium nitride.

[0049] FIG. **3** shows the result of another step of manufacturing of the embodiment of FIG. **1**. During this step, cavities **116***a* and **118***a* are formed in layers **112** and **114** to reach the lower surface of layer **112**, and thus the upper surface of layer **110**.

[0050] Cavity **116***a* is located at the location where cavity **116** is desired to be formed and will form the upper portion of cavity **116**. Conductive layer **120** is deposited on the walls and on the bottom of cavities **116***a*. Conductive layer **120** is in contact with layer **112** at the level of the walls of cavity **116**.

[0051] Cavity **118***a* is located at the location where cavity **118** is desired to be formed and will form the upper portion of cavity **118**. Conductive layer **122** is deposited on the walls and on the bottom of cavities **118***a*. Conductive layer **122** is in contact with layer **112** at the level of the walls of cavity **118**.

[0052] FIG. **4** shows the result of another step of manufacturing of the embodiment of FIG. **1**. During this step, a cavity **116***b* is formed from the bottom of cavity **116***a* and a cavity **118***b* is formed from the bottom of cavity **118***a*. The dimensions of the openings of cavities **116***b* and **118***b* are smaller than the dimensions of the bottom of cavities **116***b* and **118***b*. Cavities **116***a* and **116***b* form together cavity **116** and cavities **118***a* and **118***b* form together cavity **118**.

[0053] Cavities **116***b* and **118***b* are for example formed in a plurality of etch steps. During a first step, cavity **116***b* is for example etched to reach layer **104** and, during a second step, cavity **118***b* is for example etched to reach layer **106**. As a variation, cavities **116***b* and **118***b* are for example both

etched to reach layer **106** during a first etch step, and cavity **116***b* is deepened during a second etch step.

[0054] Insulating layer **124** covers the device and particularly the bottom and the walls of cavities **116***a*, **118***a*, **118***b*, and **116***b*.

[0055] FIG. **5** shows the result of another step of manufacturing of the embodiment of FIG. **1**. During this step, insulating layer **124** is partially etched. More particularly, layer **124** is at least partially etched in the bottom of cavities **116***b* and **118***b* and is partially etched above conductive layers **120** and **122**. Thus, layer **104** and layer **120** are accessible from cavity **116**. Similarly, layer **106** and layer **122** are accessible from cavity **118**.

[0056] This step may possibly comprise the doping of layer **104** from the bottom of cavity **116***b* to allow a better connection with an electrode.

[0057] FIG. **6** shows the result of another step of manufacturing of the embodiment of FIG. **1**. During this step, conductive layer **126** is formed, for example, conformally, on the walls and the bottom of cavities **116***a* and **116***b*. Layer **104** and layer **120** are thus electrically connected. Similarly, conductive layer **128** is formed, for example conformally, on the walls and the bottom of cavities **118***a* and **118***b*. Layer **106** and layer **122** are thus electrically connected.

[0058] Conductive layers **126** and **128** are for example formed by etching of a same conductive layer covering, for example conformally, the device.

[0059] FIG. **7** schematically shows another embodiment of a device **700** comprising a Schottky diode and a bipolar diode.

[0060] Device **700** is similar to device **100** of FIG. **1** and comprises same elements located similarly.

[0061] In device **700**, layer **106** is located between layer **102** and layer **104**, unlike device **100** of FIG. **1** where layer **104** is located between layer **102** and layer **106**. Thus, conductive layer **126** of cavity **116** is connected to the anode of diode **108** and not to the cathode. Similarly, the conductive layer **128** of cavity **118** is connected to the cathode of diode **108** and not to the anode.

[0062] Further, in the embodiment of FIG. **7**, conductive layer **120** forms a Schottky contact with layer **112**, and conductive layer **122** forms an ohmic contact with layer **112**. Thus, conductive layer **120** forms the anode of diode **123** and conductive layer **122** forms the cathode.

[0063] Thus, the anodes (A) of diodes **108** and **123** are connected together at the level of cavity **116** and the cathodes (K) of diodes **108** and **123** are connected together at the level of cavity **118**.

[0064] The other elements of device **700** are similar to those of device **100** and are thus not detailed again.

[0065] Various embodiments and variations have been described. It should be clear to those skilled in the art that certain characteristics of these various embodiments and variations may be combined, and other variations will occur to those skilled in the art.

[0066] Finally, the practical implementation of the described embodiments and variations is within the abilities of those skilled in the art based on the functional indications given hereinabove.

[0067] The various embodiments described above can be combined to provide further embodiments. These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

1. An electronic device comprising:

a first electrode located in a first cavity of a semiconductor body;

a second electrode located in a second cavity of the semiconductor body; and

a stack of a first circuit leg and a second circuit leg connected in parallel between the first electrode and the second electrode, the first circuit leg including a Schottky diode and the second circuit leg including a bipolar diode.

2. The device of claim **1**, wherein the stack comprises first, second and third semiconductor layers.

3. The device of claim **2**, wherein the bipolar diode comprises the first semiconductor layer in contact with the second semiconductor layer, the second semiconductor layer being of the conductivity type opposite to the first semiconductor layer.

4. The device of claim **2**, wherein the first cavity reaches the first semiconductor layer and the second cavity reaches the second semiconductor layer.

5. The device of claim **2**, wherein the first and second semiconductor layers are made of gallium nitride.

6. The device of claim **2**, wherein the Schottky diode comprises the third semiconductor layer in contact with the first and second electrodes, and a metal electrode in contact with the third semiconductor layer and the second electrode.

7. The device of claim **6**, wherein the third semiconductor layer is made of AlGaN.

8. The device of claim **1**, wherein the first electrode is a cathode electrode of the Schottky diode and of the bipolar diode and the second electrode is the anode electrode of the Schottky diode and of the bipolar diode.

9. A method, comprising:

manufacturing an electronic device, the manufacturing including:

forming a first electrode in a first cavity of a semiconductor body;

forming a second electrode in a second cavity of the semiconductor body; and

forming a stack of a first circuit leg and second circuit leg connected in parallel between the first electrode and the second electrode, the first circuit leg including a Schottky diode and the second circuit leg including a bipolar diode.

10. The method of claim **9**, comprising:

forming the semiconductor body, wherein forming the semiconductor body includes forming first, second, and third semiconductor layers, the bipolar diode including the first and second semiconductor layers and the Schottky diode including the third semiconductor layer; and

forming the first and second cavities in the semiconductor body.

11. The method of claim **10**, wherein the first cavity reaches the first semiconductor layer and the second cavity reaches the second semiconductor layer.

12. The method of claim **10**, forming the first and second cavities includes:

forming first and second intermediate cavities reaching a lower surface of the third semiconductor layer, and

etching through a portion of a bottom of each of the first and second intermediate cavities.

13. The method of claim **12**, comprising forming a first conductive layer on side walls and the bottom of the first intermediate cavity and forming a second conductive layer on side walls and the bottom of the second intermediate cavity.

14. The method of claim **9**, comprising depositing an insulating layer on side walls and bottoms of the first and second cavities.

15. The method of claim **14**, comprising removing the insulating layer from at least a portion of the bottom of each of the first and second cavities and from at least portions of the first and second conductive layers.

16. The method of claim **13**, wherein:

forming the first electrode includes forming a third conductive layer in the first cavity, the third conductive layer connecting the first semiconductor layer to the first conductive layer; and

forming the second electrode includes forming a fourth conductive layer in the second cavity, the fourth conductive layer connecting the second semiconductor layer to the second conductive layer.

17. An electronic device comprising:

a Schottky diode extending in a semiconductor body between first and second cavities of the semiconductor body;

a bipolar diode extending in the semiconductor body between first and second cavities;

a first conductor in the first cavity and connecting first ends of the Schottky diode and the bipolar diode to each other; and

a second conductor in the second cavity and connecting second ends of the Schottky diode and the bipolar diode to each other.

18. The device of claim **17**, wherein:

the semiconductor body comprises first, second and third semiconductor layers;

the bipolar diode comprises the first semiconductor layer in contact with the second semiconductor layer, the second semiconductor layer being of the conductivity type opposite to the first semiconductor layer; and

the Schottky diode comprises the third semiconductor layer.

19. The device of claim **18**, wherein the first cavity reaches the first semiconductor layer and the second cavity reaches the second semiconductor layer without reaching the first semiconductor layer.

20. The device of claim **18**, wherein the Schottky diode includes a metal electrode extending in the second cavity and in contact with the third semiconductor layer and the second conductor.

* * * * *