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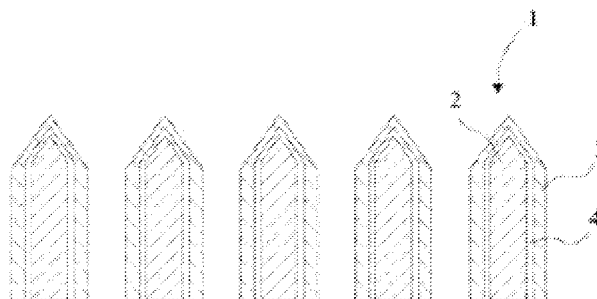


FIG. 1

(57) Abstract: A light emitting diode (LED) device includes a semiconductor nanowire core, and an In(Al)GaN active region quantum well shell located radially around the semiconductor nanowire core. The active quantum well shell contains indium rich regions having at least 5 atomic percent higher indium content than indium poor regions in the same shell. The active region quantum well shell has a non-uniform surface profile having at least 3 peaks. Each of the at least 3 peaks is separated from an adjacent one of the at least 3 peaks by a valley, and each of the at least 3 peaks extends at least 2 nm in a radial direction away from an adjacent valley.



### III-NITRIDE NANOWIRE LED WITH STRAIN MODIFIED SURFACE ACTIVE REGION AND METHOD OF MAKING THEREOF

#### RELATED APPLICATION

This application claims benefit of U.S. Provisional Patent Application Serial  
5 No. 61/917,046, filed December 17, 2013, the entire content of which is incorporated herein by reference.

#### FIELD

The embodiments of the invention are directed generally to semiconductor  
devices, such as nanowire light emitting diodes (LED), and specifically to nanowire  
10 LEDs with a non-uniform active region.

#### BACKGROUND

Nanowire light emitting diodes (LED) are of increasing interest as an  
alternative to planar LEDs. In comparison with LEDs produced with conventional  
planar technology, nanowire LEDs offer unique properties due to the one-dimensional  
15 nature of the nanowires, improved flexibility in materials combinations due to less lattice matching restrictions and opportunities for processing on larger substrates.

U.S. Patent 8,138,493 issued on March 20, 2012, which is incorporated herein by  
reference in its entirety, notes that it is difficult to fabricate light emitting diodes in the  
infra-red to green wavelength region using conventional planar technology in the GaN  
20 system and these give much lower efficiency than blue color emitting LEDs. This can be attributed to that: a) a miscibility gap for an InGa<sub>x</sub>N material in the red and green wavelength region since In<sub>x</sub>Ga<sub>1-x</sub>N with approximately 0.4 < x < 0.8 is not theoretically expected to be a stable material; and b) the high inherent defect density of the planar layers of the LED structure reduces photonic recombination efficiency by a much higher  
25 degree for high In content InGa<sub>x</sub>N than low In content InGa<sub>x</sub>N that is used in blue LEDs. The 8,138,493 patent solves this problem by providing a nanostructured LED device comprising InGa<sub>x</sub>N quantum dots between a nanowire core and a nanowire shell that provide light emission in the infra-red to green wavelength region with improved

emission. By way of example one such nanostructured LED device comprises a nanowire core made of GaN and InGaN quantum dots embedded in a GaN based shell.

## SUMMARY

An embodiment of the invention provides a light emitting diode (LED) device and a method of making the LED device. The device includes a semiconductor nanowire core and an In(Al)GaN active region quantum well shell located radially around the semiconductor nanowire core. In one embodiment, the active quantum well shell contains indium rich regions having at least 5 atomic percent higher indium content than indium poor regions in the same shell. In another embodiment, the active region quantum well shell has a non-uniform surface profile having at least 3 peaks. Each of the at least 3 peaks is separated from an adjacent one of the at least 3 peaks by a valley, and each of the at least 3 peaks extends at least 2 nm in a radial direction away from an adjacent valley.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically illustrates a side cross sectional view of a basis of a nanowire LED.

FIG. 2 schematically illustrates a side cross sectional view of a nanowire LED structure on a buffer layer.

FIGS. 3A and 3B are formal line drawings of electron microscope micrographs of a nanowire LED device in which the active region shell is formed on a smooth, uniform radial surface.

FIG. 4 schematically illustrates a side cross sectional view of a nanowire LED device in which the active region shell is formed on a non-uniform radial surface and contains indium rich regions.

FIGS. 5A, 5B, 6B, 7B and 8 are formal line drawings of electron microscope micrographs of a nanowire LED device shown in FIG. 4. FIGS. 6A and 7A are tables showing the composition of selected regions in respective FIGS. 6B and 7B.

## DETAILED DESCRIPTION OF THE EMBODIMENTS OF THE INVENTION

In one embodiment, the active region shell is formed on a non-uniform surface such that the active region shell has a non-uniform profile (e.g., a non-straight radial sidewall and/or a non-uniform thickness in the horizontal direction as a function of height in the vertical direction). This “bumpy” surface reduces or eliminates the defects (e.g., stacking faults) in the outer shell.

The formation of the active region shell comprising one or more In(Al)GaN/(Al)GaN quantum wells on a non-uniform surface causes indium rich In(Al)GaN regions (e.g., InGaN or InAlGaN regions having more than 10 atomic percent indium, such as 15 to 35 atomic percent indium) to be formed by self assembly during the formation of the active region. These indium rich regions are believed to be responsible for high brightness, high efficiency emission in the longer wavelength spectral region (e.g., green to yellow 495-590 nm peak emission wavelength region and/or orange to red 591-650 nm peak emission wavelength region) depending on the indium content of the regions.

However, in contrast to separately formed quantum dots which are separately formed between portions of the active region shell, the indium rich regions are integrally formed in-situ during the formation of the active region shell. Thus, the indium rich regions comprise integral portions of the active region quantum well shell rather than discrete nanoparticles or quantum dots embedded in the active regions quantum well shell. For example, discrete nanoparticles often have a different grain structure and/or orientation than the surrounding semiconductor layer, and a sharp transition or grain boundary between the nanoparticle and surrounding layer grains, visible in an electron microscopy micrograph. In contrast, the integral indium rich regions do not necessarily have a different crystal orientation than the surrounding indium poor regions of the surrounding active region shell and do not necessarily have a sharp transition or grain boundary.

For example, InGaN active regions containing about 10 atomic percent indium emit light with a peak wavelength of about 450 nm in the blue spectral range, InGaN active regions containing about 20 atomic percent indium emit light with a peak

wavelength of about 520 nm in the green spectral range, and InGaN active regions containing about 30 atomic percent indium emit light with a peak wavelength of about 610 nm in the red spectral range. Of course the indium concentration in the In(Al)GaN active region can be varied between 5 atomic percent and 35 atomic percent, such as 15 to 30 atomic percent, to achieve the desired color emission (e.g., blue, green, yellow, orange or red) between about 430 nm and about 650 nm, such as 450 to 620 nm.

It should be noted that the indium rich In(Al)GaN regions may be formed in the active region quantum well without using the non-uniform surface under the quantum well as long as the quantum well itself has a non-uniform thickness (i.e., is a bumpy radial quantum well shell).

Large (about 10%) lattice mismatch between InN ( $a = .354$  nm) and GaN ( $a = .319$  nm) makes it difficult to incorporate high concentrations of indium in the GaN lattice without causing structural defects in a resulting InGaN layer. However, by forming the indium rich In(Al)GaN regions in an indium poor (e.g., having 10 atomic percent or less, such as 5-10 at.% indium) active region In(Al)GaN quantum well, such as a radial quantum well parallel to m-plane (i.e., vertical plane) of the GaN/InGaN core/radial shell nanowire, the structural defects in the resulting InGaN active region shell can be reduced.

One embodiment of the invention includes a series of nanometer-scale discontinuities along the m-plane to enhance the deposition of the indium along the length of the nanowire in the In(Al)GaN active region shell. This results in “bumpy” surface composed of nanometer scale peaks (comprising the indium rich regions) and valleys (comprising the indium poor regions) along the m-plane instead of maintaining a straight quantum well surface parallel to the m-plane. For example, in this “bumpy” surface the nanoscale features project at least partially along the diagonal p-plane, 10-11, from the vertical portion of the active region quantum well which is parallel the m-plane.

In the art of nanotechnology, nanowires are usually interpreted as nanostructures having a lateral size (e.g., diameter for cylindrical nanowires or width

for pyramidal or hexagonal nanowires) of nano-scale or nanometer dimensions, whereas its longitudinal size is unconstrained. Such nanostructures are commonly also referred to as nanowhiskers, one-dimensional nano-elements, nanorods, nanotubes, etc. The nanowires can have a diameter or width of up to about 2 micron.

5 The small size of the nanowires provides unique physical, optical and electronic properties. These properties can for example be used to form devices utilizing quantum mechanical effects (e.g., using quantum wires) or to form heterostructures of compositionally different materials that usually cannot be combined due to large lattice mismatch. As the term nanowire implies, the one dimensional nature may be

10 associated with an elongated shape. Since nanowires may have various cross-sectional shapes, the diameter is intended to refer to the effective diameter. By effective diameter, it is meant the average of the major and minor axis of the cross-section of the structure.

All references to upper, top, lower, downwards etc. are made as considering

15 the substrate being at the bottom and the nanowires extending upwards from the substrate. Vertical refers to a direction perpendicular to the plane formed by the substrate, and horizontal to a direction parallel to the plane formed by the substrate. This nomenclature is introduced for the easy of understanding only, and should not be considered as limiting to specific assembly orientation etc.

20 Any suitable nanowire LED structure as known in the art may be used in the methods of the invention. Nanowire LEDs are typically based on one or more pn- or p-i-n-junctions. The difference between a pn junction and a p-i-n-junction is that the latter has a wider active region. The wider active region allows for a higher probability of recombination in the i-region. Each nanowire comprises a first

25 conductivity type (e.g., n-type) nanowire core and an enclosing second conductivity type (e.g., p-type) shell for forming a pn or pin junction that in operation provides an active region for light generation. While the first conductivity type of the core is described herein as an n-type semiconductor core and the second conductivity type shell is described herein as a p-type semiconductor shell, it should be understood that

30 their conductivity types may be reversed.

FIG. 1 schematically illustrates the basis for a nanowire LED structure that is modified in accordance with embodiments of the invention. In principle, one single nanowire is enough for forming a nanowire LED, but due to the small size, nanowires are preferably arranged in arrays comprising hundreds, thousands, tens of thousands, or more, of nanowires side by side to form the LED structure. For illustrative purposes the individual nanowire LED devices will be described herein as being made up from nanowire LEDs 1 having an n-type nanowire core 2 and a p-type shell 3 at least partly enclosing the nanowire core 2 and an intermediate active region 4, which may comprise a single intrinsic or lightly doped (e.g., doping level below  $10^{16} \text{ cm}^{-3}$ ) semiconductor layer or one or more quantum wells, such as 3-10 quantum wells comprising a plurality of semiconductor layers of different band gaps. However, for the purpose of embodiments of the invention nanowire LEDs are not limited to this. For example the nanowire core 2, the active region 4 and the p-type shell 3 may be made up from a multitude of layers or segments. In alternative embodiments, only the core 2 may comprise a nanostructure or nanowire by having a width or diameter below 2 micron, while the shell 3 may have a width or diameter above one micron.

The III-V semiconductors are of particular interest due to their properties facilitating high speed and low power electronics and optoelectronic devices such as lasers and LEDs. The nanowires can comprise any semiconductor material, and suitable materials for the nanowire include but are not limited to: GaAs (p), InAs, Ge, ZnO, InN, GaInN, GaN AlGaInN, BN, InP, InAsP, GaInP, InGaP:Si, InGaP:Zn, GaInAs, AlInP, GaAlInP, GaAlInAsP, GaInSb, InSb, Si. Possible donor dopants for e.g. GaP are Si, Sn, Te, Se, S, etc, and acceptor dopants for the same material are Zn, Fe, Mg, Be, Cd, etc. It should be noted that the nanowire technology makes it possible to use nitrides such as GaN, InN and AlN, which facilitates fabrication of LEDs emitting light in wavelength regions not easily accessible by conventional technique. Other combinations of particular commercial interest include, but are not limited to GaAs, GaInP, GaAlInP, GaP systems. Typical doping levels range from  $10^{18}$  to  $10^{20} \text{ cm}^{-3}$ . A person skilled in the art is though familiar with these and other materials and realizes that other materials and material combinations are possible.

Preferred materials for nanowire LEDs are III-V semiconductors such as a III-nitride semiconductor (e.g., GaN, AlInGaN, AlGaN and InGaN, etc.) or other semiconductor (e.g., InP, GaAs). In order to function as a LED, the n-side and p-side of each nanowire LED 1 has to be contacted, and the present invention provides  
5 methods and compositions related to contacting the n-side and the p-side of the nanowires in a LED structure.

Although the exemplary fabrication method described herein preferably utilizes a nanowire core to grow semiconductor shell layers on the cores to form a core-shell nanowire, as described for example in U.S. Patent 7,829,443, to Seifert et  
10 al., incorporated herein by reference for the teaching of nanowire fabrication methods, it should be noted that the invention is not so limited.

For example, in alternative embodiments, only the core may constitute the nanostructure (e.g., nanowire) while the shell may optionally have dimensions which are larger than typical nanowire shells. Furthermore, the device can be shaped to  
15 include many facets, and the area ratio between different types of facets may be controlled. This is exemplified by the "pyramid" facets and the vertical sidewall facets. The LEDs can be fabricated so that the emission layer formed on templates with dominant pyramid facets or sidewall facets. The same is true for the contact layer, independent of the shape of the emission layer.

FIG. 2 illustrates an exemplary structure that provides a support for the  
20 nanowires. By growing the nanowires on a growth substrate 5, optionally using a growth mask, or dielectric masking layer, 6 (e.g., a nitride layer, such as silicon nitride dielectric masking layer) to define the position and determine the bottom interface area of the nanowires, the substrate 5 functions as a carrier for the nanowires  
25 that protrude from the substrate 5, at least during processing. The bottom interface area of the nanowires comprises the root area of the core 2 inside each opening in the dielectric masking layer 6. The substrate 5 may comprise different materials, such as III-V or II-VI semiconductors, Si, Ge, Al<sub>2</sub>O<sub>3</sub>, SiC, Quartz, glass, etc., as discussed in Swedish patent application SE 1050700-2 (assigned to GLO AB), which is  
30 incorporated by reference herein in its entirety. Other suitable materials for the



substrate include, but are not limited to: GaAs, GaP, GaP:Zn, GaAs, InAs, InP, GaN, GaSb, ZnO, InSb, SOI (silicon-on-insulator), CdS, ZnSe, CdTe. In one embodiment, the nanowire cores 2 are grown directly on the growth substrate 5.

Preferably, the substrate 5 is also adapted to function as a current transport layer connecting to the n-side of each nanowire LED 1. This can be accomplished by having a substrate 5 that comprises a semiconductor buffer layer 7 arranged on the surface of the substrate 5 facing the nanowire LEDs 1, as shown in FIG. 2, by way of example a III-nitride layer, such as a GaN and/or AlGaN buffer layer 7 on a Si substrate 5. The buffer layer 7 is usually matched to the desired nanowire material, and thus functions as a growth template in the fabrication process. For an n-type core 2, the buffer layer 7 is preferably also doped n-type. The buffer layer 7 may comprise a single layer (e.g., GaN), several sublayers (e.g., GaN and AlGaN) or a graded layer which is graded from high Al content AlGaN to a lower Al content AlGaN or GaN.

The method described in the 7,829,443 patent includes providing the growth mask 6 on a support (e.g., on the buffer layer 7). Openings are then formed in the growth mask 6 to expose the buffer layer. The openings are preferably well controlled, both in regards to their diameter and their relative positioning. Several techniques known in the art can be used for the procedure including, but not limited to electron beam lithography (EBL), nanoimprint lithography, optical lithography and reactive ion etching (RIE) or wet chemical etching methods. Preferably the openings are about 75-125 nm, such as about 100 nm in diameter and pitched 0.5-5  $\mu\text{m}$  apart. The openings define the position and the diameter of the nanowire cores 2 to be produced.

Then, the nanowire cores 2 are grown by a CVD based process where the precursor source flows are continuous. The precursor source flow rates are adjusted to achieve a low supersaturation in the growth zone. The V/III-ratio should be 100 or less, such as in the range of 1-100, preferably in the range of 1-50, and even more preferably in the range of 5-50. It should be noted that this V/III-ratio is considerably lower than the ratios used for bulk film growth. In other words, the nanowire cores 2 are grown at a low V/III ratio at a relatively low temperature (e.g., below 800 C).

Then, one or more shells 3, 4 shown in Figures 1 and 2 are grown on the core 2 by increasing the temperature above 800 C, such as 900-1200 C, and increasing the V/III ratio to a higher amount than that used for the core growth (e.g., a V/III ratio higher than 100, such as 200-1000). For example, the n-GaN nanowire core 2 may be grown by MOCVD using ammonia and TMG (trimethylgallium) gas sources and an optional doping source gas (e.g., a Mg containing source gas). The NH<sub>3</sub> flow rate may be 0.2 to 3.0 sccm during core 2 growth and 50-100 sccm during shell 3, 4 growth. TMG (trimethylgallium) flow rate may be between 0.12 and 1.2 μmol/min.

If desired, an intermediate n-GaN shell 8 may be formed on the n-GaN core 2 before forming the active region shell 4. The n-GaN shell 8 may be formed at the high temperature (above 800 C, such as 900-1200 C) and high V/III ratio higher than 100, such as 200-1000. This shell 8 is shown in Figures 3A and 3B and has a smooth (i.e., straight) outer sidewall (i.e., the m-plane radial sidewall).

In one embodiment, when the quantum well active region shell 4 is formed on a smooth radial surface of the intermediate n-GaN shell 8, a number of defects, which are believed to be horizontal stacking faults 9, are formed in an outer shell 3 (e.g., a p-type GaN and/or AlGa<sub>x</sub>N shell) which surrounds the active region shell 4, as shown in Figures 3A and 3B.

Thus, in one embodiment illustrated in Figure 4, the active region shell is formed on a non-uniform (e.g., “bumpy”) surface such that the active region shell 4 has a non-uniform profile and the localized indium rich In(Al)Ga<sub>x</sub>N regions 21. The “bumpy” surface can be initiated in the underlayer 8 under (e.g., radially inward from) the active region quantum well shell 4, such as in the intermediate shell or in a barrier layer underneath the active region quantum well shell 4. This forms a strain modified surface active region shell 4. Preferably, the underlayer 8 has a lower indium content than the active region quantum well 4 (i.e., underlayer 8 has a wider band gap than active region quantum well 4) to avoid absorbing the quantum well emission. For example, the underlayer 8 may have no indium (e.g., consist of GaN or AlGa<sub>x</sub>N) or it may comprise an InGa<sub>x</sub>N or InAlGa<sub>x</sub>N underlayer having less than 10 at.% indium such as 1-5 at.% indium.

By controlling the bumpiness of the underlayer 8, a more homogeneous, high indium content active quantum well layer(s) 4 can be subsequently grown without introducing defects. The degree of bumpiness of the underlayer 8 can be controlled by the growth conditions, such as temperature, MOCVD pressure, MOCVD reactant  
5 flow rates and/or the In/Ga ratio of the underlayer. For example, the degree of bumpiness increases with increasing indium content and a lower growth temperature.

The bumpiness and growth conditions of the underlayer 8 may control the composition of the quantum well active region 4 from homogeneous to the creation of discreet indium rich regions embedded in an In(Al)GaN quantum well of lower  
10 indium content. The thickness of the quantum well would be similar to or less than the peak-valley height described below.

While a single quantum well active region 4 is shown in Figure 4, a multiple quantum well active region 4 may also be formed. Separating the bumpy quantum wells 4 with a bumpy GaN or lower In content InGaN or InAlGaN barrier layers  
15 provides the growth of a multiple quantum well active region 4 structure on the outer shell 8 of the nanowires with decreased amount of defects and with each quantum well having localized indium rich regions 21.

For example, the non-uniform surface or profile in the underlayer 8 and/or in the active region shell 4 may have a peak 12 to adjacent valley 13 separation of 10 to  
20 30 nm, and peak 12 to adjacent valley 13 depth (i.e., variation in thickness) of 3 to 5 nm. Preferably, the active layer region shell 4 has a thickness greater than 5 nm to avoid producing stacking faults. If the underlayer 8 has more than 15% indium, then it also preferably has a thickness greater than 5 nm to avoid producing stacking faults.

As used herein, a non-uniform surface means a non-straight or non-smooth  
25 (i.e., bumpy or rough) surface, with at least 3 peaks (e.g., bulges) 12 extending at least 2 nm, such as 3 to 5 nm away from at least one valley (e.g., recess) 13 in the radial (i.e., m-plane) surface along the horizontal direction. A non-uniform profile means that the quantum well(s) in the active region shell have a non-straight radial surface (i.e., sidewall) and/or a non-uniform thickness along the radial (i.e., horizontal)  
30 direction as a function of height in the vertical direction. A non-uniform thickness

means that the radial (i.e., horizontal) thickness of the active region shell (e.g., quantum well) 4 varies by at least 15%, such as by 20-40% at different vertical positions in the shell 4 and have roughly non-parallel radial sidewalls.

Increasing the film thickness of In-containing bumpy layers (e.g., the active region shell) above 5nm will disproportionately deposit indium on the peaks 12 compared to the valleys 13 and form localized indium rich In(Al)GaN regions 21 in the active region shell 4 on the peaks 12 in the underlayer 8. As shown in Figure 4, the indium rich regions 21 in the active region shell 4 correspond to the peaks 22 in the active region shell 4, and the indium rich regions 21 are separated by the indium poor regions 24 corresponding to the valleys 23 in the active region shell 4. Preferably, the difference in indium content between the indium rich and indium poor regions in shell 4 is at least 5 atomic percent, such as 10 to 25 atomic percent.

This results in an inhomogeneous active layer 4 which can yield multiple emission peaks if the electrical contact is put directly on the m-plane 14 of the nanowire. As shown in Figure 4, preferably the p-side electrical contact 16 to the p-type GaN shell 3 is made on the sloped p-plane 15 at the tip of the shell 3, while the n-side electrical contact 17 is made to the c-plane of the n-type GaN nanowire core 2 through the n-type GaN or AlGaN substrate 7. Thus, the lower emission peaks coming from the m-plane 14 are not visible in the EL spectrum. Therefore, the volume of high In content material (i.e., regions 21) that emits longer wavelength green, yellow, orange or red light can increase without introducing the deleterious stacking fault defects.

For example, as shown in Figures 5A and 5B, the non-uniform surface may be achieved by forming the intermediate shell 8 at a low temperature (e.g., 800 C or below), while maintaining the high V/III ratio. This causes the outer radial surface 10 of the intermediate shell 8 to become non-uniform. The active region shell 4 and the outer p-type shell (or shells) 3 are then formed over the intermediate shell 8. As can be seen in Figures 5A and 5B, this growth on a non-uniform surface produces the active regions shell 4 with the non-uniform profile and reduces or eliminates the defects (e.g., stacking faults) 9 in the outer shell(s) 3.

As shown in Figures 5A and 5B, the active region shell 4 has a non-uniform thickness. For example, the quantum well containing shell 4 has a thickness that ranges from 7.6 nm at location #5 to 12.2 nm at location #3. Thus, the shell 4 radial thickness varies by over 30% (i.e., 30-38%) and by over 4 nm along the vertical  
5 direction.

The formation of the active region shell 4 with the non-uniform profile comprising one or more InGaN/GaN quantum wells on the non-uniform surface 10 results in localized indium rich InGaN regions 21 being formed by self assembly during the formation of the active region shell. Specifically, it is believed that the  
10 regions 21 are formed in the thicker (i.e., bulging) regions of the active region shell 4. Figures 6A and 7A illustrate tables showing Al, Ga, and In content in atomic percent in various locations of the nanowire LEDs shown in respective Figures 6B and 7B. As shown in Figures 6A and 6B, regions # 1, 2, 3 and 7 in the InGaN/GaN quantum well active regions 4 contain over 15 atomic percent indium, such as 17.5 to  
15 23.9 at% indium (i.e., 20.5, 17.5, 19.9 and 23.9, respectively). Thus, indium concentration varies by over 5 atomic percent (e.g., 5 to 6.4 atomic percent) between regions # 2 and 7. Regions # 4-6 are located in the AlGaN outer shell(s) and have no indium and a variable concentration of aluminum.

As shown in Figures 7A and 7B, regions # 1, 2 and 3 in the InGaN/GaN  
20 quantum well active regions 4 contain over 14 atomic percent indium, such as 14.1 to 18.3 at% indium (i.e., 18.0, 18.3 and 14.1, respectively). Thus, indium concentration varies by over 4 atomic percent between regions # 2 and 3. Regions # 4-7 are located in the AlGaN outer shell(s) and have no indium and a variable concentration of aluminum.

25 These indium rich regions 21 are believed to be responsible for high brightness, high efficiency emission in the green to yellow wavelength spectral region.

Furthermore, the formation of the active region shell 4 on the non-uniform surface 10 is believed to result in a much greater thickness of the active region 4 on the  
30 radial surfaces (i.e., the non-polar {10-10} m-plane) than on the pyramidal, slanted upper

surfaces (i.e., the semi-polar {1-101} p-plane) of the intermediate shell 8. The radial thickness of the active region shell 4 over the m-plane of the intermediate shell 8 is at least 3 times, such as 3-10 times thicker than the thickness over the p-plane, 10-11, of the intermediate shell 8 at the top of the device. This improves the LED device performance because of the improved emission from the m-plane portions of the InGaN quantum wells compared to the emission from the p-plane, 10-11, portions of the same quantum wells. Thus, the increased m-plane thickness of the quantum wells compared to their p-plane, 10-11, thickness means that a higher ratio of radiation is emitted from the m-plane portion than the p-plane, 10-11, portion of the quantum wells than in the prior art devices with thicker p-plane, 10-11, portions of the quantum wells.

Figure 8 illustrates an alternative embodiment of the invention. In this embodiment, the device contains three intermediate shells 8A, 8B and 8C. In interior intermediate shell 8A comprises an n-GaN shell. The middle shell 8B comprises an n-InGaN shell with a non-uniform surface and the outer shell 8C comprises a n-GaN shell with a non-uniform surface. Both shells 8B and 8C may be formed with the high V/III flow ratio and a low temperature (e.g., below 800 C) to form the non-uniform surface for growth of the active region shell 4 on the outer intermediate shell 8.

As shown in Figure 8, the active region shell 4 has a non-uniform thickness. For example, the quantum well containing shell 4 has a thickness that ranges from 6.8 nm at location #4 to 12.5 nm at location #3. Thus, the shell 4 radial thickness varies by over 40% (i.e., 40-45.6%) and by over 5 nm (e.g., 5 to 5.7 nm).

Although the present invention is described in terms of nanowire LEDs, it should be appreciated that other nanowire based semiconductor devices, such as field-effect transistors, diodes and, in particular, devices involving light absorption or light generation, such as, photodetectors, solar cells, lasers, etc., can be implemented on any nanowire structures.

All publications and patents cited in this specification are herein incorporated by reference as if each individual publication or patent were specifically and individually indicated to be incorporated by reference and are incorporated herein by

reference to disclose and describe the methods and/or materials in connection with which the publications are cited. The citation of any publication is for its disclosure prior to the filing date and should not be construed as an admission that the present invention is not entitled to antedate such publication by virtue of prior invention.

- 5 Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

What is claimed is:

1. A nanowire device, comprising:  
a semiconductor nanowire core; and  
a first semiconductor shell located radially around the semiconductor  
5 nanowire core,  
wherein:  
the first semiconductor shell has a non-uniform surface profile having  
at least 3 peaks;  
each of the at least 3 peaks is separated from an adjacent one of the at  
10 least 3 peaks by a valley; and  
each of the at least 3 peaks extends at least 2 nm in a radial direction  
away from an adjacent valley.
2. The device of claim 1, wherein the device comprises a light emitting  
15 diode (LED) device and the first semiconductor shell comprises an active region  
quantum well shell.
3. The device of claim 2, further comprising a second semiconductor  
shell located radially between the semiconductor nanowire core and the first  
semiconductor shell.
- 20 4. The device of claim 3, wherein:  
the second semiconductor shell has a non-uniform surface profile having at  
least 3 peaks;  
each of the at least 3 peaks is separated from an adjacent one of the at least 3  
peaks by a valley; and  
25 each of the at least 3 peaks extends at least 2 nm in a radial direction away  
from an adjacent valley.
5. The device of claim 4, wherein the second semiconductor shell  
comprises an underlayer barrier shell of the active region quantum well.
6. The device of claim 4, wherein the second semiconductor shell  
30 comprises an underlayer shell located radially inward from the active region.



7. The device of claim 4, wherein:  
a radial thickness of the first semiconductor shell varies by at least 15 percent in a nanowire axial direction between the peaks and the valleys.  
a peak to adjacent valley separation in the first semiconductor shell in the  
5 nanowire axial direction is 10 to 30 nm;  
each of the at least 3 peaks in the first semiconductor shell extends 3 to 5 nm in a radial direction away from an adjacent valley;  
the first semiconductor shell has a thickness of greater than 5 nm in the radial direction;  
10 a peak to adjacent valley separation in the second semiconductor shell in a nanowire axial direction is 10 to 30 nm; and  
each of the at least 3 peaks in the second semiconductor shell extends 3 to 5 nm in a radial direction away from an adjacent valley.
8. The device of claim 4, further comprising:  
15 an insulating mask layer located over a semiconductor surface of a support, wherein the semiconductor nanowire core comprises a first conductivity type semiconductor nanowire core extending substantially perpendicular from the semiconductor surface of the support through an opening in the insulating mask layer;  
at least one second conductivity type semiconductor shell extending over and  
20 around the active region quantum well shell;  
a first electrode layer that contacts the second conductivity type semiconductor shell; and  
a second electrode layer which is electrically connects to the semiconductor nanowire core.
- 25 9. The device of claim 8, wherein:  
the first conductivity type comprises n-type;  
the second conductivity type comprises p-type;  
the support comprises a n-GaN or n-AlGaIn n-type semiconductor buffer layer on a substrate;  
30 the semiconductor nanowire core comprises a n-GaN nanowire core;

the active region quantum well shell comprises an InGaN shell between GaN barrier shells; and

the first electrode comprises a transparent conductive oxide (TCO).

10. The device of claim 4, wherein:

5 each of the at least 3 peaks in the first semiconductor shell comprises a nanometer scale discontinuity along an m-plane of the first semiconductor shell that projects at least partially along a p-plane; and

10 the active quantum well shell comprises an In(Al)GaN semiconductor shell which contains indium rich regions located at the peaks having at least 5 atomic percent higher indium content than indium poor regions located at the valleys.

11. The device of claim 10, wherein the active quantum well shell comprises an InGaN semiconductor shell in which the indium rich regions contain more than 10 atomic percent indium and the indium poor regions contain less than 10 atomic percent indium.

15 12. The device of claim 11, wherein indium rich regions contain 15 to 30 atomic percent indium and the indium poor regions contain 1 to 5 atomic percent indium.

13. The device of claim 12, wherein the LED has a 495 to 590 nm peak emission wavelength or a 591 to 650 nm peak emission wavelength.

20 14. The device of claim 13, wherein the LED has an about 520 nm peak emission wavelength and the indium rich regions contain about 20 atomic percent indium.

25 15. The device of claim 13, wherein the LED has an about 610 nm peak emission wavelength and the indium rich regions contain about 30 atomic percent indium.

16. A light emitting diode (LED) device, comprising:  
a semiconductor nanowire core; and

a first semiconductor shell comprising an In(Al)GaN active region quantum well shell located radially around the semiconductor nanowire core,

wherein:

5 the active region quantum well shell contains indium rich regions having at least 5 atomic percent higher indium content than indium poor regions in the active region quantum well shell; and

wherein the indium rich regions comprise integral portions of the active region quantum well shell rather than discrete nanoparticles embedded in the active region quantum well shell.

10 17. The device of claim 16, wherein the active quantum well shell comprises an InGaN semiconductor shell in which the indium rich regions contain more than 10 atomic percent indium and the indium poor regions contain less than 10 atomic percent indium.

15 18. The device of claim 17, wherein indium rich regions contain 15 to 30 atomic percent indium and the indium poor regions contain 1 to 5 atomic percent indium.

19. The device of claim 18, wherein the LED has a 495 to 590 nm peak emission wavelength or a 591 to 650 nm peak emission wavelength.

20 20. The device of claim 19, wherein the LED has an about 520 nm peak emission wavelength and the indium rich regions contain about 20 atomic percent indium.

21. The device of claim 19, wherein the LED has an about 610 nm peak emission wavelength and the indium rich regions contain about 30 atomic percent indium.

25 22. The device of claim 16, wherein:  
the first semiconductor shell has a non-uniform surface profile having at least 3 peaks which comprise the indium rich regions;  
each of the at least 3 peaks is separated from an adjacent one of the at least 3 peaks by a valley which comprises the indium poor region; and

each of the at least 3 peaks extends at least 2 nm in a radial direction away from an adjacent valley.

23. The device of claim 22, further comprising a second semiconductor shell located radially between the semiconductor nanowire core and the first semiconductor shell.

24. The device of claim 23, wherein:  
the second semiconductor shell has a non-uniform surface profile having at least 3 peaks;  
10 each of the at least 3 peaks is separated from an adjacent one of the at least 3 peaks by a valley; and  
each of the at least 3 peaks extends at least 2 nm in a radial direction away from an adjacent valley.

25. The device of claim 24, wherein the second semiconductor shell comprises an underlayer barrier shell of the active region quantum well.

26. The device of claim 24, wherein the second semiconductor shell comprises an underlayer shell located radially inward from the active region.

27. The device of claim 24, wherein:  
a radial thickness of the first semiconductor shell varies by at least 15 percent  
20 in a nanowire axial direction between the peaks and the valleys.

a peak to adjacent valley separation in the first semiconductor shell in the nanowire axial direction is 10 to 30 nm;

each of the at least 3 peaks in the first semiconductor shell extends 3 to 5 nm in a radial direction away from an adjacent valley;

25 the first semiconductor shell has a thickness of greater than 5 nm in the radial direction;

a peak to adjacent valley separation in the second semiconductor shell in a nanowire axial direction is 10 to 30 nm; and

30 each of the at least 3 peaks in the second semiconductor shell extends 3 to 5 nm in a radial direction away from an adjacent valley.

28. The device of claim 24, further comprising:  
an insulating mask layer located over a semiconductor surface of a support,  
wherein the semiconductor nanowire core comprises a first conductivity type  
semiconductor nanowire core extending substantially perpendicular from the  
5 semiconductor surface of the support through an opening in the insulating mask layer;  
at least one second conductivity type semiconductor shell extending over and  
around the active region quantum well shell;  
a first electrode layer that contacts the second conductivity type semiconductor  
shell; and  
10 a second electrode layer which is electrically connects to the semiconductor  
nanowire core.

29. The device of claim 28, wherein:  
the first conductivity type comprises n-type;  
the second conductivity type comprises p-type;  
15 the support comprises a n-GaN or n-AlGaN n-type semiconductor buffer layer  
on a substrate;  
the semiconductor nanowire core comprises a n-GaN nanowire core;  
the active region quantum well shell comprises an InGaN shell between GaN  
barrier shells; and  
20 the first electrode comprises a transparent conductive oxide (TCO).

30. The device of claim 24, wherein each of the at least 3 peaks in the first  
semiconductor shell comprises a nanometer scale discontinuity along an m-plane of  
the first semiconductor shell that projects at least partially along a p-plane.

31. A method of making nanowire device, comprising:  
25 forming a semiconductor nanowire core; and  
forming a first semiconductor shell located radially around the semiconductor  
nanowire core,  
wherein:  
the first semiconductor shell has a non-uniform surface profile having  
30 at least 3 peaks;

each of the at least 3 peaks is separated from an adjacent one of the at least 3 peaks by a valley; and

each of the at least 3 peaks extends at least 2 nm in a radial direction away from an adjacent valley.

5

32. The method of claim 31, wherein the device comprises a light emitting diode (LED) device and the first semiconductor shell comprises an active region quantum well shell.

33. The method of claim 32, further comprising forming a second semiconductor shell radially around the semiconductor nanowire core prior to forming the first semiconductor shell.

34. The method of claim 33, wherein:  
the second semiconductor shell has a non-uniform surface profile having at least 3 peaks;  
each of the at least 3 peaks is separated from an adjacent one of the at least 3 peaks by a valley;  
each of the at least 3 peaks extends at least 2 nm in a radial direction away from an adjacent valley; and  
the first semiconductor shell is formed on the second semiconductor shell and assumes the non-uniform surface profile of the second semiconductor shell.

35. The method of claim 34, wherein the second semiconductor shell comprises an underlayer barrier shell of the active region quantum well.

36. The method of claim 34, wherein the second semiconductor shell comprises an underlayer shell located radially inward from the active region.

37. The method of claim 34, wherein:  
a radial thickness of the first semiconductor shell varies by at least 15 percent in a nanowire axial direction between the peaks and the valleys.  
a peak to adjacent valley separation in the first semiconductor shell in the nanowire axial direction is 10 to 30 nm;

each of the at least 3 peaks in the first semiconductor shell extends 3 to 5 nm in a radial direction away from an adjacent valley;

the first semiconductor shell has a thickness of greater than 5 nm in the radial direction;

5 a peak to adjacent valley separation in the second semiconductor shell in a nanowire axial direction is 10 to 30 nm; and

each of the at least 3 peaks in the second semiconductor shell extends 3 to 5 nm in a radial direction away from an adjacent valley.

38. The method of claim 34, further comprising:

10 forming an insulating mask layer located over a semiconductor surface of a support, wherein forming the semiconductor nanowire core comprises epitaxially growing a first conductivity type semiconductor nanowire core extending substantially perpendicular from the semiconductor surface of the support through an opening in the insulating mask layer;

15 forming at least one second conductivity type semiconductor shell extending over and around the active region quantum well shell;

forming a first electrode layer that contacts the second conductivity type semiconductor shell; and

20 forming a second electrode layer which is electrically connects to the semiconductor nanowire core.

39. The method of claim 38, wherein:

the first conductivity type comprises n-type;

the second conductivity type comprises p-type;

25 the support comprises a n-GaN or n-AlGaN n-type semiconductor buffer layer on a substrate;

the semiconductor nanowire core comprises a n-GaN nanowire core;

the active region quantum well shell comprises an InGaN shell between GaN barrier shells; and

the first electrode comprises a transparent conductive oxide (TCO).

30 40. The method of claim 34, wherein:

each of the at least 3 peaks in the first semiconductor shell comprises a nanometer scale discontinuity along an m-plane of the first semiconductor shell that projects at least partially along a p-plane; and

the active quantum well shell comprises an In(Al)GaN semiconductor shell  
5 which contains indium rich regions located at the peaks having at least 5 atomic percent higher indium content than indium poor regions located at the valleys.

41. The method of claim 40, wherein the active quantum well shell comprises an InGaN semiconductor shell in which the indium rich regions contain more than 10 atomic percent indium and the indium poor regions contain less than 10  
10 atomic percent indium.

42. The method of claim 41, wherein indium rich regions contain 15 to 30 atomic percent indium and the indium poor regions contain 1 to 5 atomic percent indium.

43. The method of claim 42, wherein the LED has a 495 to 590 nm peak  
15 emission wavelength or a 591 to 650 nm peak emission wavelength.

44. The method of claim 43, wherein the LED has an about 520 nm peak emission wavelength and the indium rich regions contain about 20 atomic percent indium.

45. The method of claim 43, wherein the LED has an about 610 nm peak  
20 emission wavelength and the indium rich regions contain about 30 atomic percent indium.

46. A method of making a light emitting diode (LED) device, comprising:  
forming a semiconductor nanowire core; and  
forming a first semiconductor shell radially around the semiconductor  
25 nanowire core, the first semiconductor shell comprising an In(Al)GaN active region quantum well shell with indium rich regions which are integrally formed in-situ during the formation of the first semiconductor shell,  
wherein indium rich regions having at least 5 atomic percent higher indium content than indium poor regions in the first semiconductor shell.



47. The method of claim 46, wherein the active quantum well shell comprises an InGaN semiconductor shell in which the indium rich regions contain more than 10 atomic percent indium and the indium poor regions contain less than 10  
5 atomic percent indium.

48. The method of claim 47, wherein indium rich regions contain 15 to 30 atomic percent indium and the indium poor regions contain 1 to 5 atomic percent indium.

49. The method of claim 48, wherein the LED has a 495 to 590 nm peak  
10 emission wavelength or a 591 to 650 nm peak emission wavelength.

50. The method of claim 49, wherein the LED has an about 520 nm peak emission wavelength and the indium rich regions contain about 20 atomic percent indium.

51. The method of claim 49, wherein the LED has an about 610 nm peak  
15 emission wavelength and the indium rich regions contain about 30 atomic percent indium.

52. The method of claim 46, wherein:  
the first semiconductor shell has a non-uniform surface profile having  
at least 3 peaks which comprise the indium rich regions;  
20 each of the at least 3 peaks is separated from an adjacent one of the at least 3 peaks by a valley which comprises the indium poor region; and  
each of the at least 3 peaks extends at least 2 nm in a radial direction away from an adjacent valley.

53. The method of claim 52, further comprising forming a second  
25 semiconductor shell radially around the semiconductor nanowire core prior to forming the first semiconductor shell.

54. The method of claim 53, wherein:

the second semiconductor shell has a non-uniform surface profile having at least 3 peaks;

each of the at least 3 peaks is separated from an adjacent one of the at least 3 peaks by a valley; and

5 each of the at least 3 peaks extends at least 2 nm in a radial direction away from an adjacent valley.

55. The method of claim 54, wherein the second semiconductor shell comprises an underlayer barrier shell of the active region quantum well.

56. The method of claim 54, wherein the second semiconductor shell  
10 comprises an underlayer shell located radially inward from the active region.

57. The method of claim 54, wherein:  
a radial thickness of the first semiconductor shell varies by at least 15 percent in a nanowire axial direction between the peaks and the valleys.

a peak to adjacent valley separation in the first semiconductor shell in the  
15 nanowire axial direction is 10 to 30 nm;

each of the at least 3 peaks in the first semiconductor shell extends 3 to 5 nm in a radial direction away from an adjacent valley;

the first semiconductor shell has a thickness of greater than 5 nm in the radial direction;

20 a peak to adjacent valley separation in the second semiconductor shell in a nanowire axial direction is 10 to 30 nm; and

each of the at least 3 peaks in the second semiconductor shell extends 3 to 5 nm in a radial direction away from an adjacent valley.

58. The method of claim 54, further comprising:  
25 forming an insulating mask layer located over a semiconductor surface of a support, wherein forming the semiconductor nanowire core comprises epitaxially growing a first conductivity type semiconductor nanowire core extending substantially perpendicular from the semiconductor surface of the support through an opening in the insulating mask layer;

forming at least one second conductivity type semiconductor shell extending over and around the active region quantum well shell;

forming a first electrode layer that contacts the second conductivity type semiconductor shell; and

5 forming a second electrode layer which is electrically connects to the semiconductor nanowire core.

59. The method of claim 58, wherein:

the first conductivity type comprises n-type;

the second conductivity type comprises p-type;

10 the support comprises a n-GaN or n-AlGaN n-type semiconductor buffer layer on a substrate;

the semiconductor nanowire core comprises a n-GaN nanowire core;

the active region quantum well shell comprises an InGaN shell between GaN barrier shells; and

15 the first electrode comprises a transparent conductive oxide (TCO).

60. The method of claim 54, wherein each of the at least 3 peaks in the first semiconductor shell comprises a nanometer scale discontinuity along an m-plane of the first semiconductor shell that projects at least partially along a p-plane.

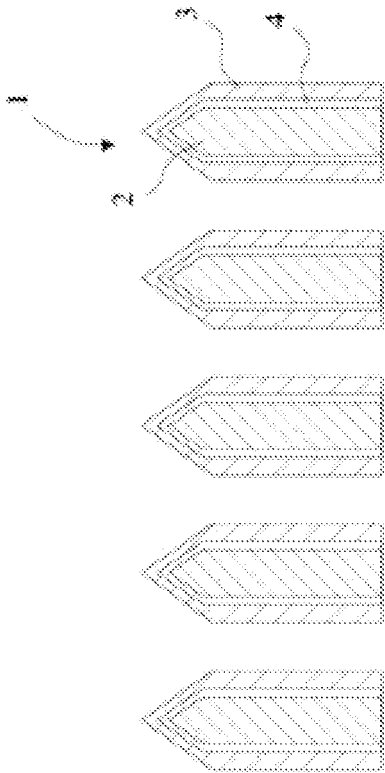


FIG. 1

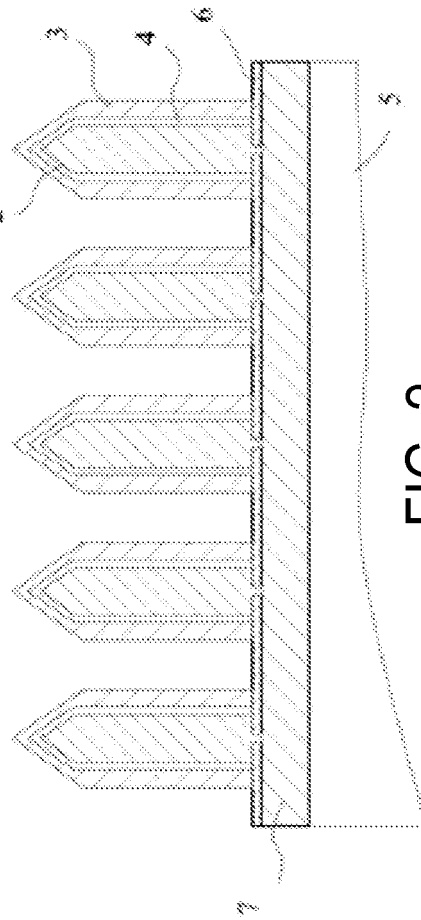


FIG. 2

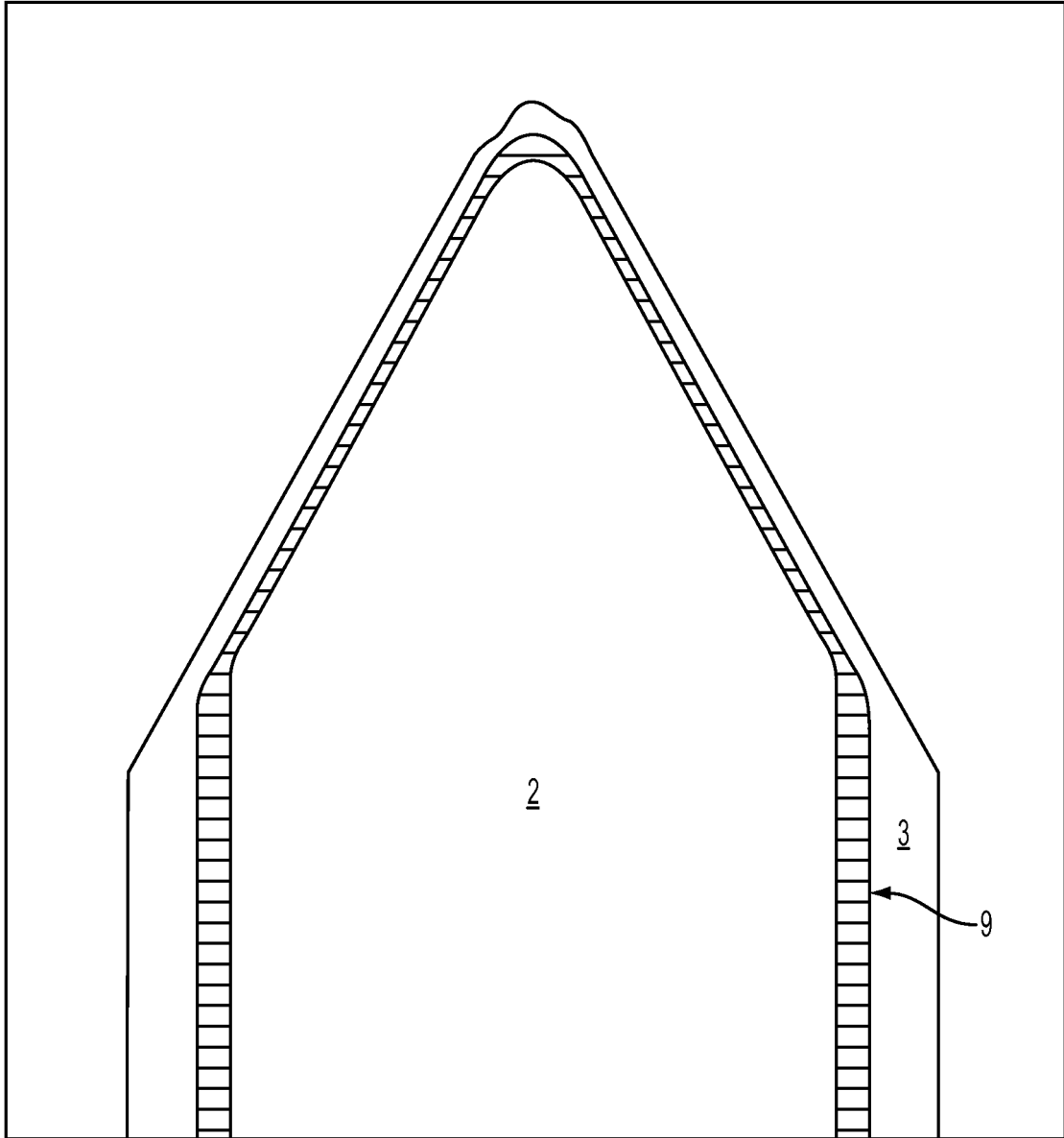


FIG. 3A

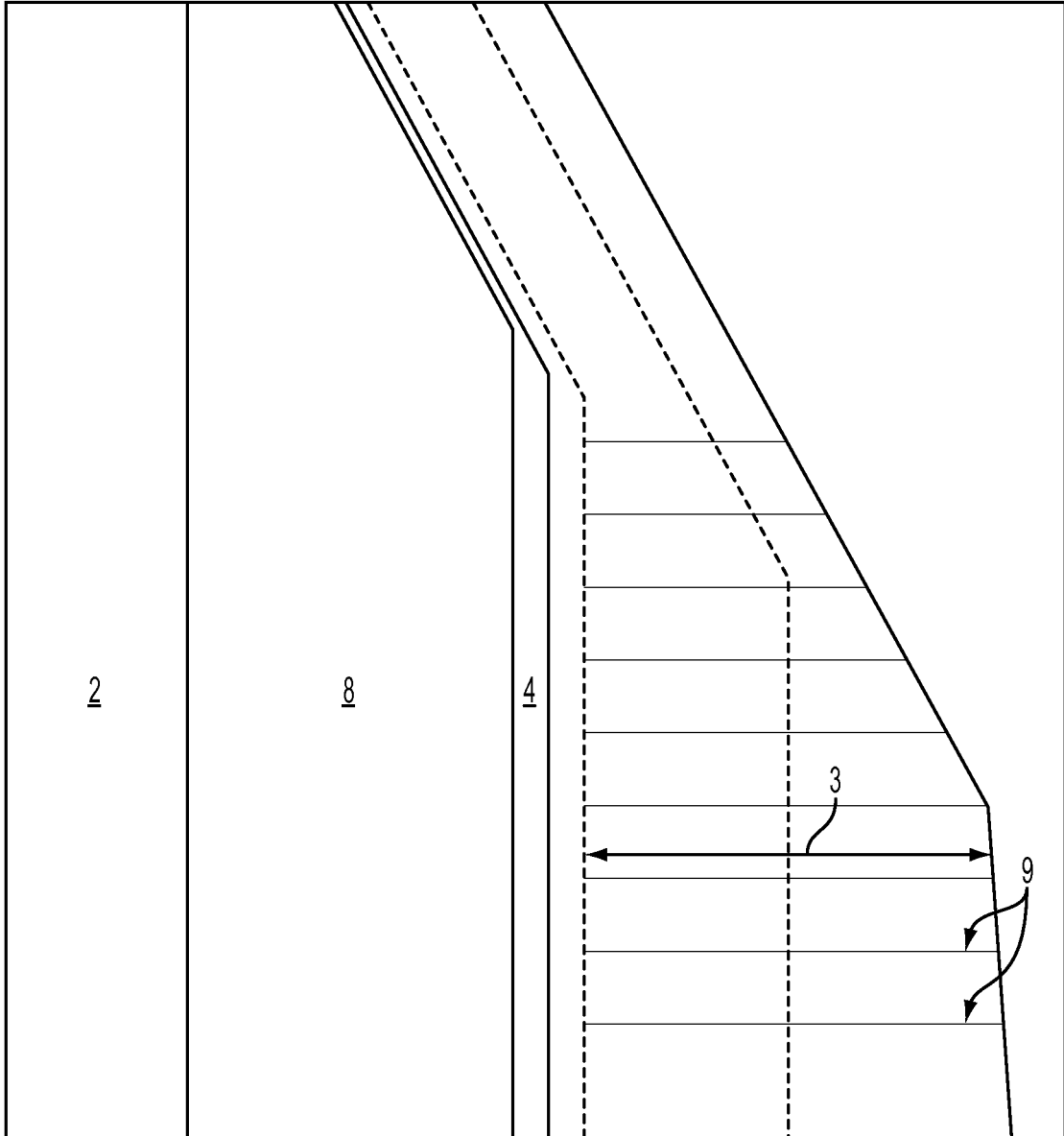


FIG. 3B

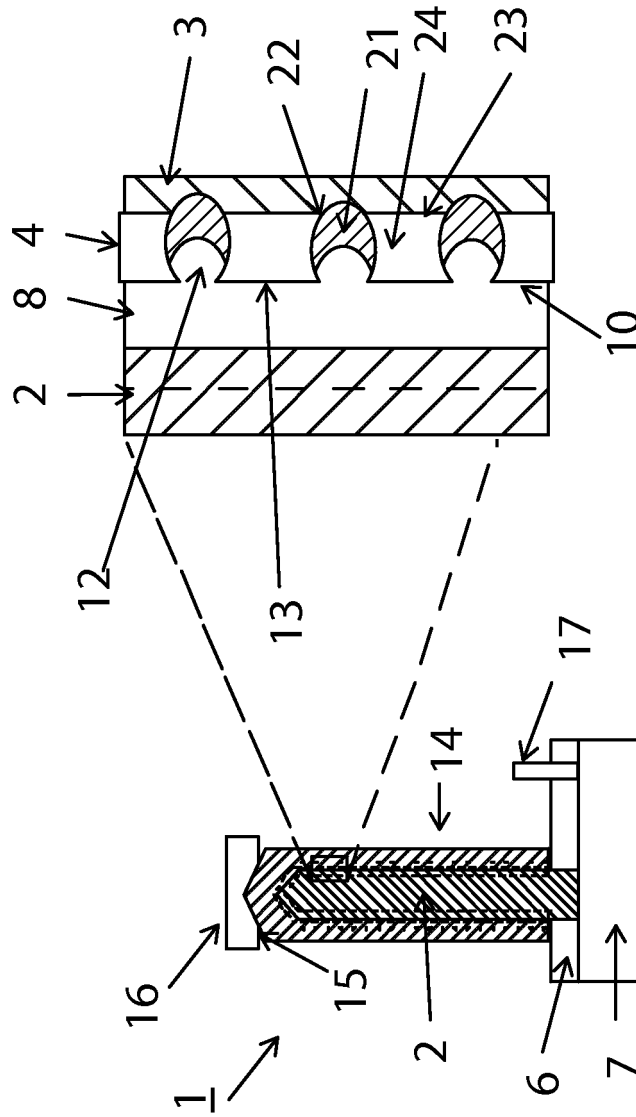


FIG. 4

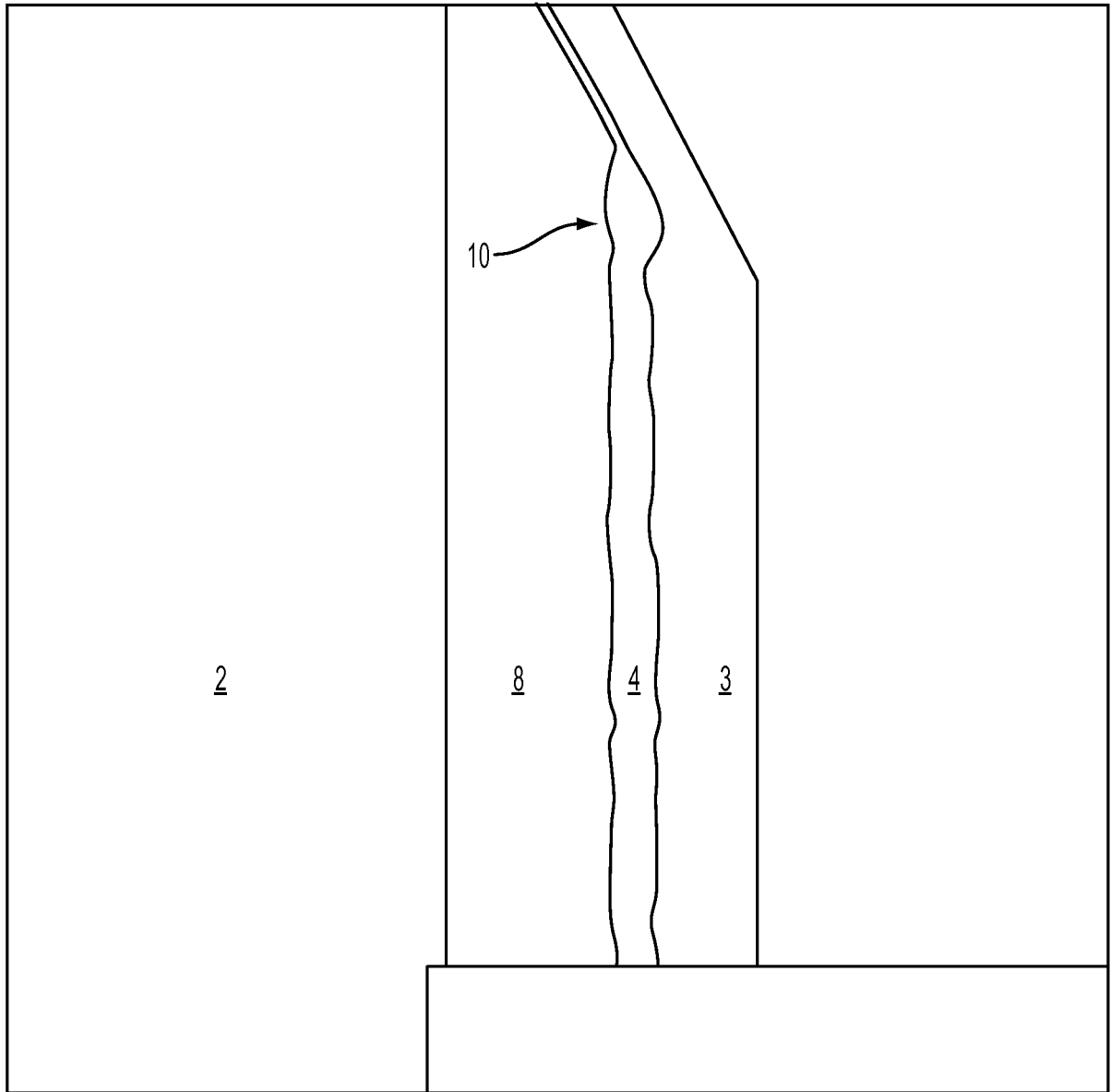


FIG. 5A



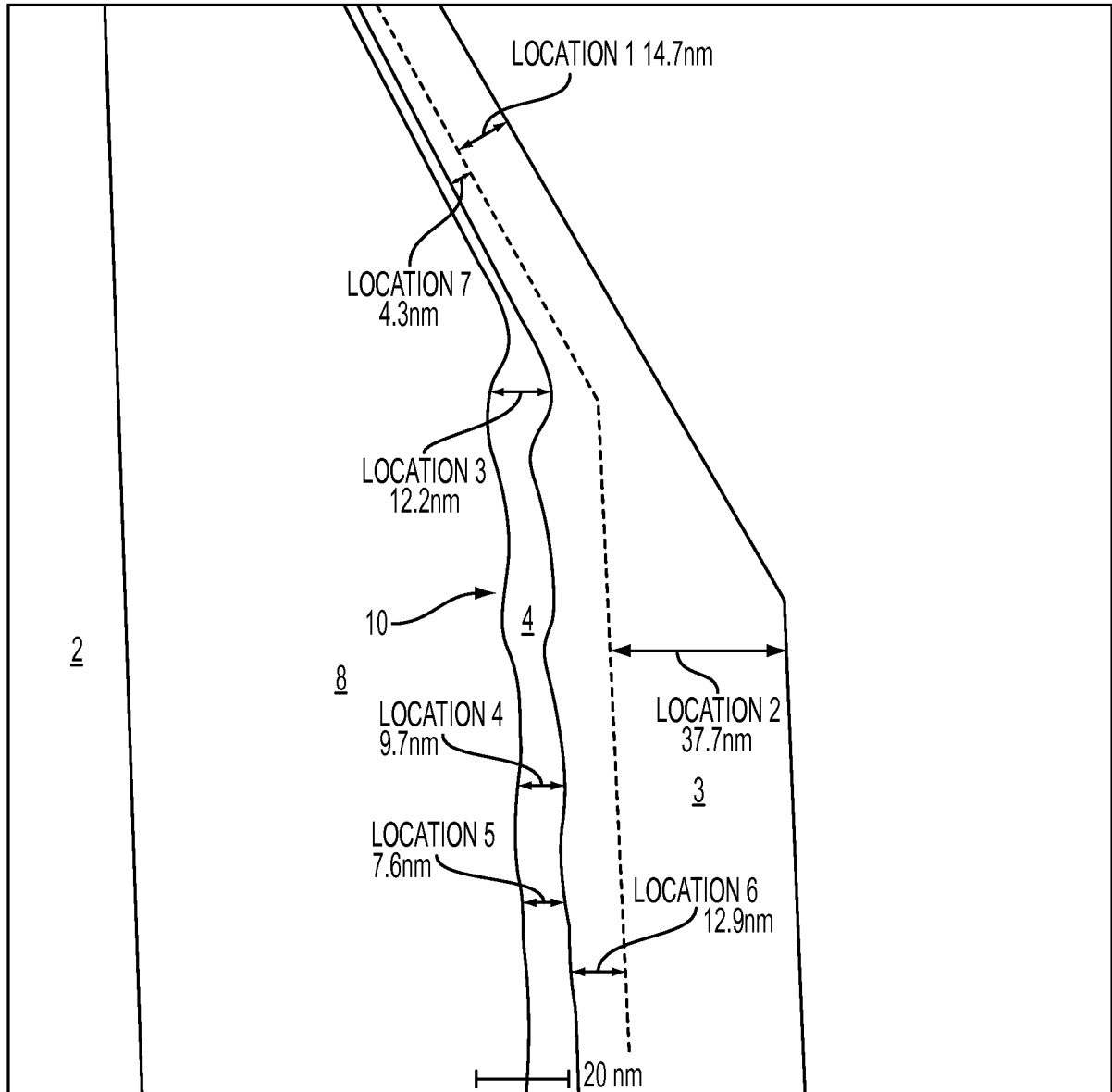


FIG. 5B

Spectrum	In stats.	Al	Ga	In
1	Yes	2.0	77.4	20.5
2	Yes	0.7	81.9	17.5
3	Yes	0.5	79.6	19.9
4	Yes	31.2	69.1	-0.3
5	Yes	15.1	85.7	-0.8
6	Yes	9.9	90.0	0.1
7	Yes	-0.1	76.2	23.9
Mean		8.5	80.0	11.6
Std. deviation		11.6	6.8	11.3
Max.		31.2	90.0	23.9
Min.		-0.1	69.1	-0.8

FIG. 6A

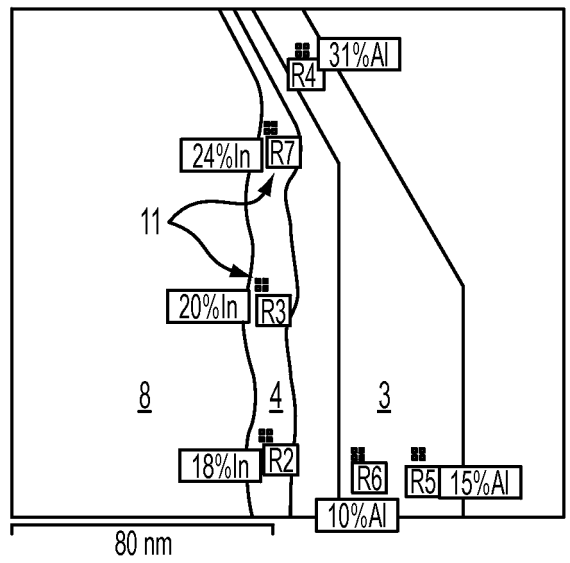


FIG. 6B

Spectrum	In stats.	Al	Ga	In
Spectrum 1	Yes	0.8	81.2	18.0
Spectrum 2	Yes	1.3	80.2	18.3
Spectrum 3	Yes	7.9	78.0	14.1
Spectrum 4	Yes	40.6	59.6	-0.2
Spectrum 5	Yes	37.1	62.6	0.4
Spectrum 6	Yes	14.5	86.4	-0.9
Spectrum 7	Yes	11.6	88.6	-0.2
Mean		16.3	76.7	7.1
Std. deviation		16.2	11.3	9.2
Max.		40.6	88.6	18.3
Min.		0.8	59.6	-0.9

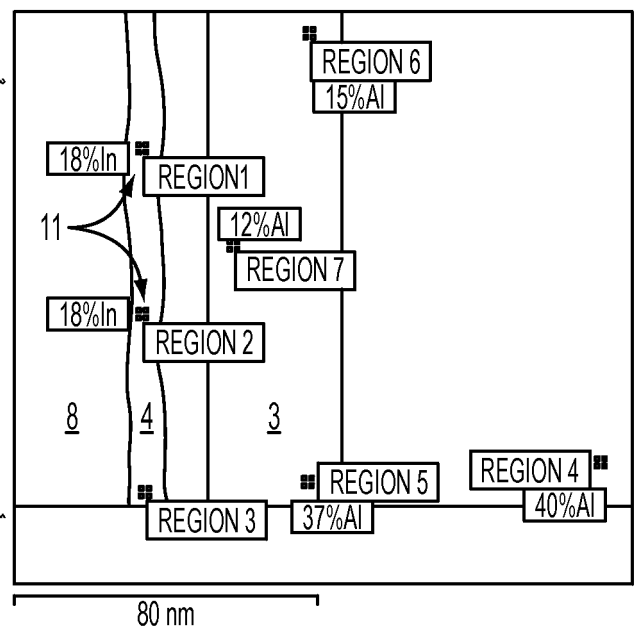


FIG. 7A

FIG. 7B

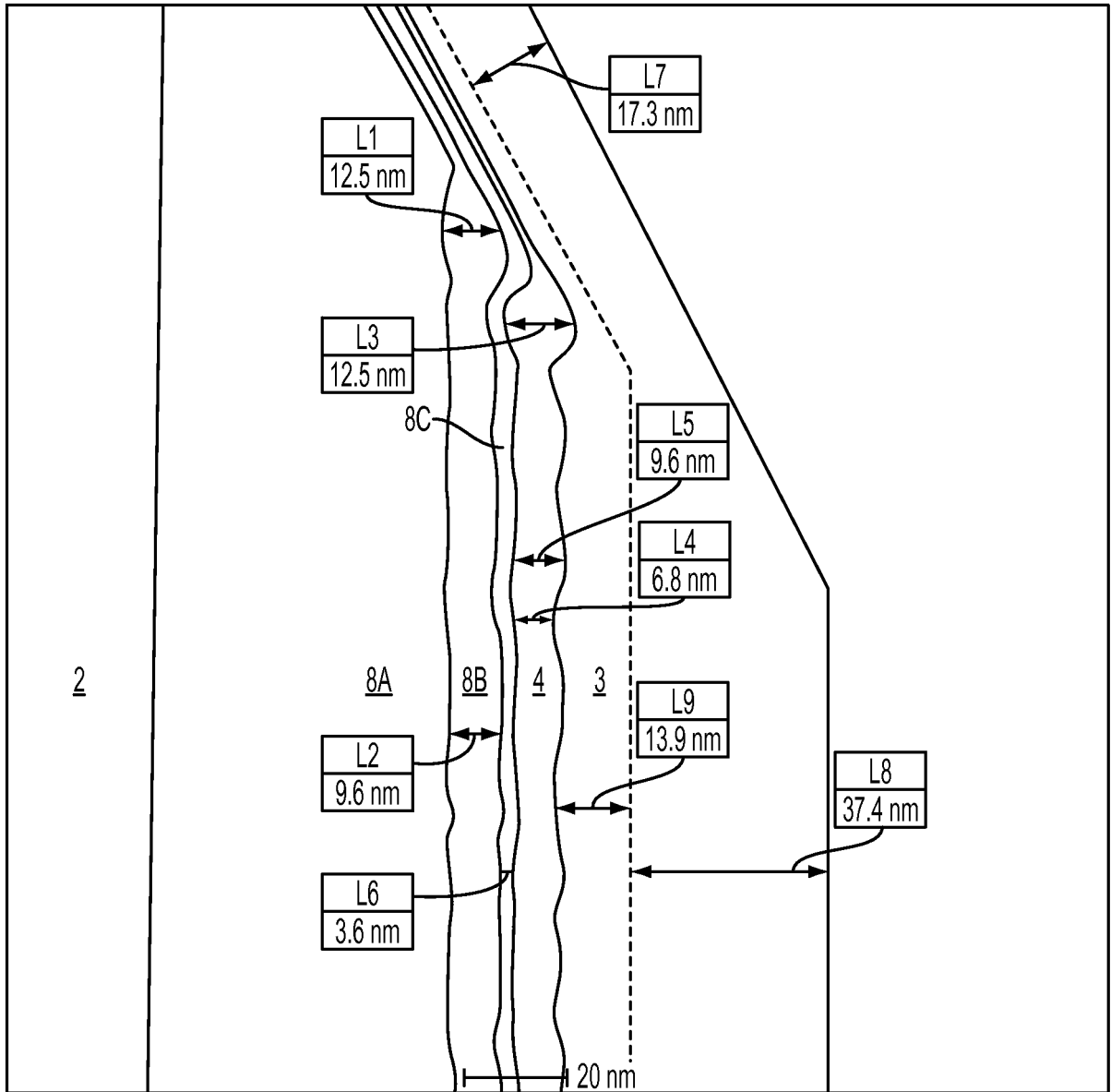


FIG. 8

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2014/070347****A. CLASSIFICATION OF SUBJECT MATTER****H01L 33/20(2010.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/20; H01L 21/20; B82B 1/00; B82B 3/00; H01L 33/18; H01L 21/335; H01L 33/00; H01L 33/44; F21Y 101/02; H01L 29/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: nanowire, core, shell, peak, valley, quantum, LED

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0225526 A1 (STEPHEN D. HERSEE et al.) 06 September 2012 See paragraphs [0034]-[0036], [0043] and figures 1, 4.	1, 3, 31, 33
Y		2, 32
A		4-30, 34-60
Y	US 2010-0276664 A1 (STEPHEN D. HERSEE) 04 November 2010 See paragraphs [0104]-[0114] and figures 10A-10C.	2, 32
A	KR 10-2012-0059064 A (SAMSUNG LED CO., LTD.) 08 June 2012 See paragraphs [0026]-[0035] and figure 1.	1-60
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A	JP 2009-105088 A (PANASONIC ELECTRIC WORKS CO., LTD.) 14 May 2009 See paragraphs [0044]-[0058] and figure 2.	1-60

 Further documents are listed in the continuation of Box C. See patent family annex.

\* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

30 March 2015 (30.03.2015)

Date of mailing of the international search report

**30 March 2015 (30.03.2015)**

Name and mailing address of the ISA/KR

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## INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/070347

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2014/070347**

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